PROCEEDINGS OF SCIENCE

# SPACIROC3: A Front-End Readout ASIC for JEM-EUSO cosmic ray observatory

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Abstract:

The SPACIROC ASIC is designed for the JEM-EUSO fluorescence-imaging telescope on board of the International Space Station. Its goal is the detection of Extreme Air Showers (EAS) above a few $10^{19}$ eV, developing underneath at a distance of about 400 km, in the troposphere. The SPACIROC family is dedicated to readout 64-channel Multi Anode PMT (MAPMT) or similar detectors. The two main features of this ASIC are the photon counting for each input and the charge conversion for each 8-channel sum. In the photon counting mode, the 100% trigger efficiency is achieved for 1/3 photo-electron (pe) input charges and in order to avoid pile-up in case of a large flux of photons, the double pulse resolution is required to be shorter than 10 ns. For the charge measurement, the ASIC should operate in a large dynamic range (1 pe to 100 pe per pixel). The operating conditions of JEM-EUSO require having low power dissipation (1 mW/channel). High-speed performances with low power are obtained thanks to the SiGe technology used for the ASIC.

This ASIC has been submitted in three successive versions: SPACIROC1, which showed global good behavior, has been used to equip the EUSO-BALLON instrument. The second version was a conservative design to improve performances and decrease power consumption. The third version has been designed to improve the double pulse separation and to increase the charge dynamic range thanks to new front end architecture.

The design and performances of the third version of SPACIROC are presented in TIPP2014 paper.

*Technology and Instrumentation in Particle Physics 2014*
*2-6 June, 2014*
*Amsterdam, the Netherlands*

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PoS(TIPP2014)172

## 1.Introduction

The primary purpose of JEM-EUSO mission [1] is the detection of the Extensive Air Showers (EAS) created by the Extreme Energy Cosmic Rays (EECR $>10^{19}$ eV), inside the atmosphere. JEM-EUSO, which is a fluorescence telescope, looking downward, that should be installed on the International Space Station, will detect the fluorescent photons released by the EAS. By observing these phenomena from the upper side of the atmosphere, this telescope will be able to identify the EECR.

SPACIROC [2], which stands for Spatial Photomultiplier Array Counting and Integrating Readout Chip, was designed accordingly to the requirements from the JEM-EUSO consortium. Multi-anode photomultipliers (MAPMT) are proposed to be the sensitive device of the JEM-EUSO observatory focal surface. As JEM-EUSO is intended to track the fluorescent light, this ASIC is required to count the number of photons reaching each pixel of the MAPMTs. The secondary mission of SPACIROC is to measure the intensity of photon flux by performing charge measurement. Three versions of this ASIC were developed using the 0.35 µm SiGe process from AMS. The first version equips the EUSO-BALLOON instrument [3] [4] which is a pathfinder for the satellite mission JEM-EUSO. The final dimensions of the ASIC are 4.6 mm x 4.1 mm (19 mm²) and the third version was submitted to the foundry in November 2013.

## 2.The ASIC specifications and architecture

SPACIROC offers 64 inputs dedicated to the anodes of one MAPMT. For the following, the MAPMT gain is assumed to be $10^6$ so that 1 photoelectron (1 p.e.) corresponds to roughly 160 fC.

### 2.1Specifications

The required specifications for the chip are the following:

- 64 channels with MAPMT gain adjustment.
- Independent photon counting measurement with 100% trigger efficiency for charges greater than 50 fC (~1/3 p.e.).
- Double pulse separation at 100MHz
- Charge measurement :
- 8 internal channels (multiplexed inputs).
- Dynamic range: 0 p.e – 800 p.e.
- Power consumption: ~1 mW/channel.
- Photon counting and charge measurement every Gate Time Unit (GTU=2.5µs)
- 9 data serial outputs.

The circuit design was geared towards low power consumption and radiation hardness for the spaceflight electronics systems. Several design and layout techniques have been applied to SPACIROC in order to increase its tolerance against the Single Event Latchup (SEL) and Single Event Upset (SEU) effects. Figure 1 represents the final layout of the ASIC. The main objective

of the third version is to allow separation of two consecutive MAPMT pulses at 100 MHz while minimizing the power consumption.

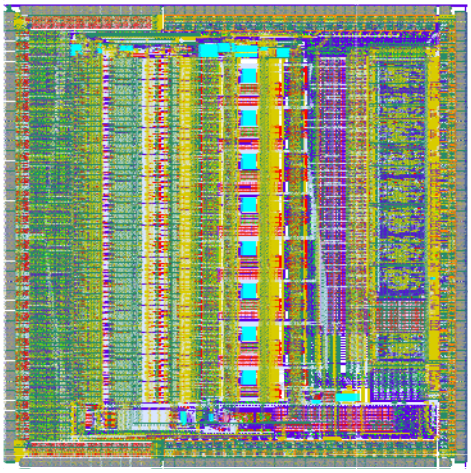

Figure 1 : SPACIROC layout.

### 2.2 Architecture

The general architecture (cf figure 2) of SPACIROC can be divided into 3 main blocks: the Photon Counting, the charge integration and the digital part. However figure 2 doesn't include the auxiliary components of the ASIC such as the bandgap reference, slow control register and signals monitoring.

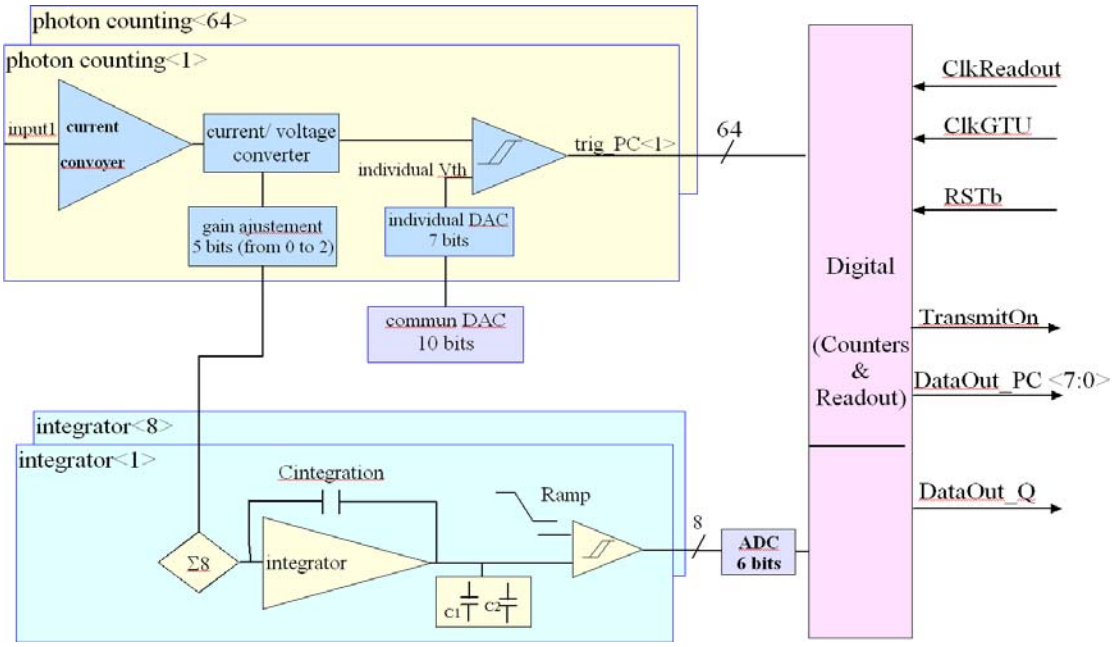


Figure 2: SPACIROC3 general architecture

### 2.2.1 Photon counting

The 64 signals from MAPMT anodes are fed through the fast current preamplifiers. The preamplifier is based on Super Common Base (SCB) structure which has been used in MAROC3 chip [5]. Thanks to the Super Common Base structure, the preamplifier has a reasonably low input impedance (~100 Ohm) while maintaining a low quiescent current. These two characteristics are important for minimising the crosstalk and static power consumption.

A 5 kOhm resistor is used to transform the current from the preamplifier into a voltage pulse thus giving a gain around 1.8 mV/fC. Afterward, the preamplifier outputs are sent to a voltage discriminator in order to transform these signals into trigger pulses. The threshold is used to discriminate the signal of each channel. It is set thanks to a 10-bit common DAC register and 7-bit individual DAC. The MAPMT gain non-uniformity is corrected by an individual threshold per channel. The use of the word “trigger(s)” in the next sections will refer to the Photon triggered pulses at the outputs of the ASIC analog part. The preamplifier and the discriminator are designed to have a fast response and produce a trigger pulse width lower than 10 ns.

### 2.2.2 Charge measurement

SPACIROC3 allows coarse measurements of the input charges while maintaining a simple architecture of the analog and digital parts. The input of the 8 integrators is the sum of 8 consecutive preamplified signals. A 5-bit gain adjustment (from 0 to 2) per channel is available before summing the 8 channels. This feature allows tuning the dynamic range accordingly to the application. For JEM-EUSO, the integrator should work from 0 pe to 100 pe per channel. A 7-bit DAC is implemented to remove the DC current from the 8 preamplifier outputs. The integrator is made of a high gain amplifier with a feedback capacitor and resistor. The main requirement for this part is to achieve charge memorization during more than 25 µs. The integrator amplifier is followed by an analog memory made by two capacitors allowing a “ping –pong” mode to avoid dead time during conversion. The integration is done during one GTU (Gate Time Unit) and the conversion is done by a 6-bit ADC ramp.

### 2.2.3 Digital design

All the data acquisition and readout are done within a defined time slot which is call Gate Time Unit (GTU=2.5 µs). This means that during every cycle of GTU, the present data are acquired and the previous acquired data are sent out to the DAQ system via serial links. Figure 5 illustrates the architecture of the digital block.

The biggest part of the digital block is used for the 64-channel Photon Counting where each channel has a dedicated 8-bit Gray counter. The trigger signals from the Photon Counting Analog part is used to clock these counters. In order to send out the 512-bit Photon Counting data, 8 serial links are used. A parity bit is also available for each serial link to check the data integrity.

The other part of the digital block is used to manage the 6-bit ADC (start_conversion, reset of the integrator, ...) and transmit the ADC data. A serial link is used to send the 48 bits from the ADC and a parity bit is also available for data verification.

The slow control register of SPACIROC was designed carefully in order to minimize area, to reduce the power consumption and to increase the robustness of the system. Flip-flops in critical areas are implemented in Triple Modular Redundancy (TMR) configuration in order to mitigate the effects of SEU.

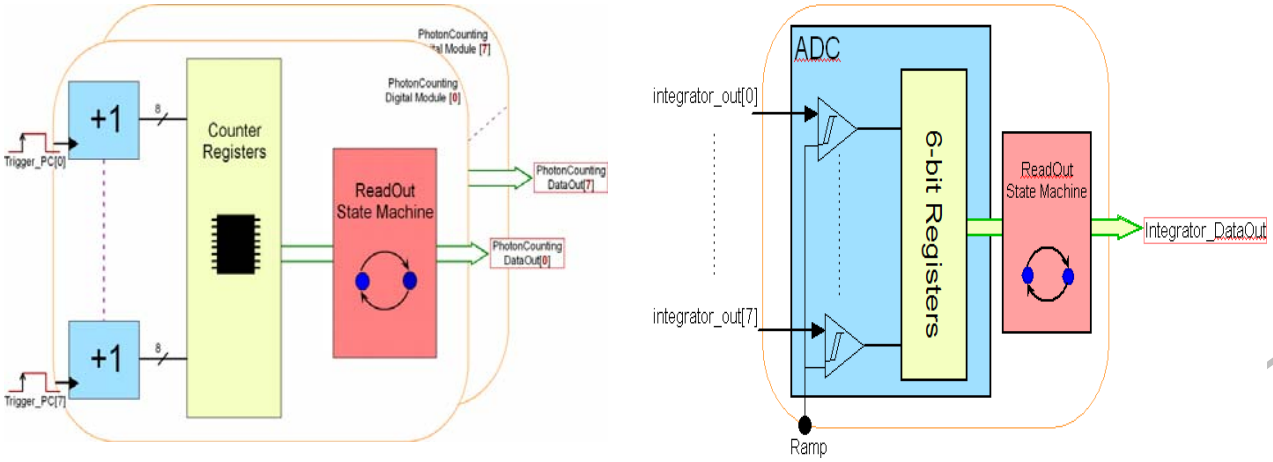


Figure 5: Photon Counting (on the left) and charge (on the right) digital module.

## 3.Measurements

The ASIC was received in March 2014 and extensive tests have been carried out since. A test board (figure 6) and a Labview interface have been developed to perform these tests.

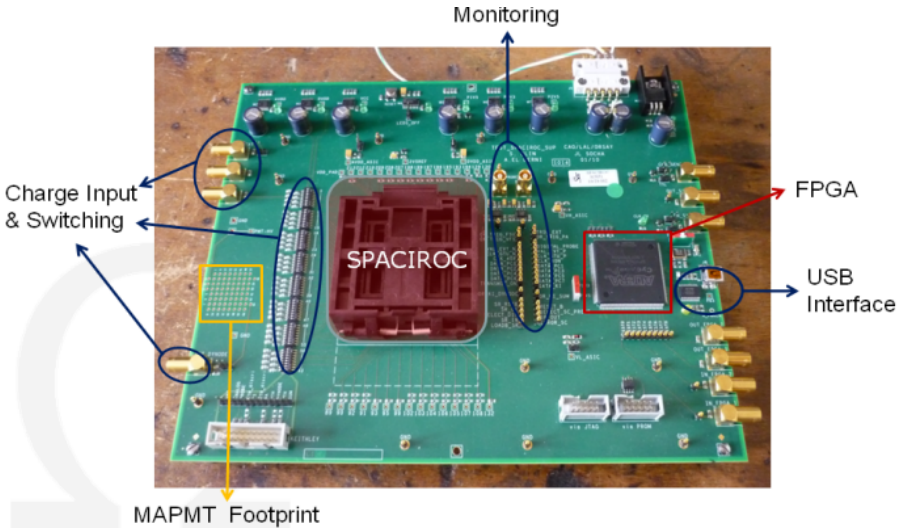


Figure 6: SPACIROC test board

One of the first measurements was to check the DC levels of the ASIC analog part. Below is the figure for the pedestal level preamplifier outputs (figure 7). The speed of the preamplifier can be tuned by slow control parameters.

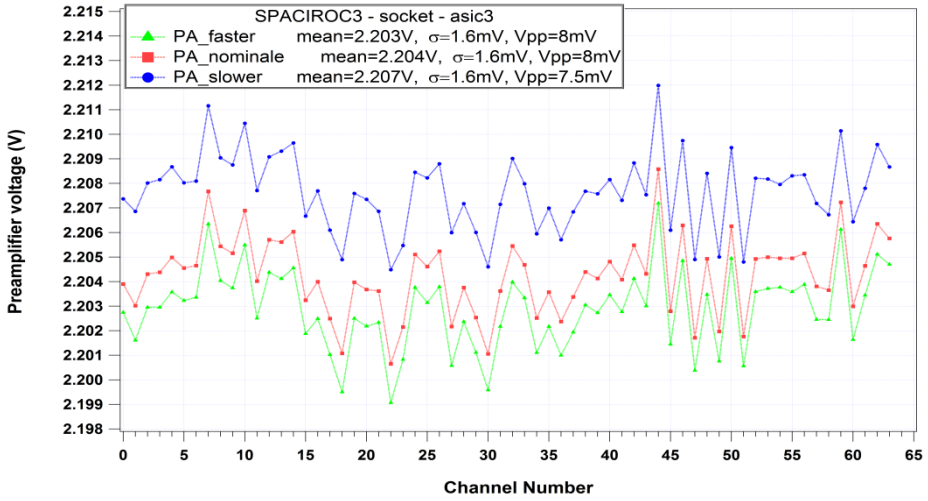


Figure 7: PA pedestals

The overall pedestal dispersions are quite good (~1.6 mV). The RMS noise levels have been verified as well as the analog part. The measured noise levels are acceptable around 600 µV.

In order to set the threshold efficiently, the corresponding voltage (Vdac) has to be linear as a function of the DAC register. The 10-bit DAC voltage can be measured on a dedicated output (figure 8). This common DAC covers the voltage range of 1.4-2.8 V with a nice linearity of ± 0.15%. The range and linearity allow the setting of the common threshold. The LSB of the DAC is less than 1.3 mV. The 7-bit DAC settings add an offset on the threshold per channel. The figure 9 shows the 64 thresholds versus the 10-bit DAC value for different 7-bit DAC values.

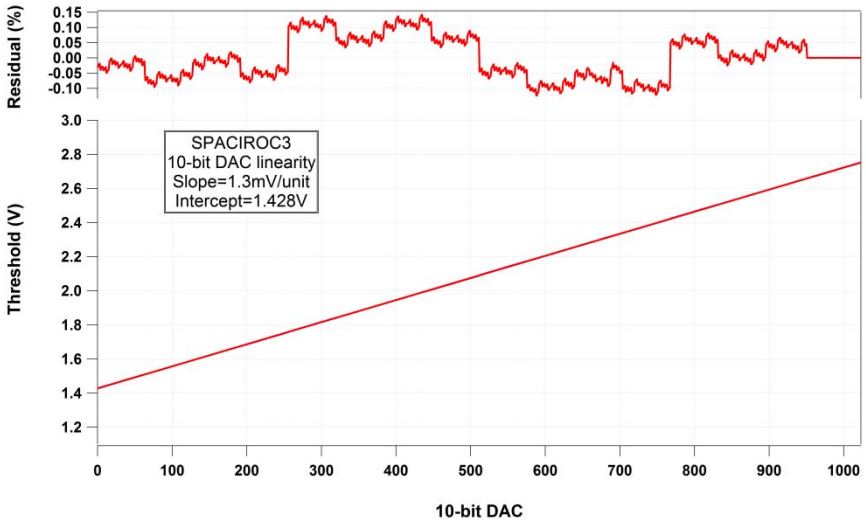


Figure 8: global DAC linearity

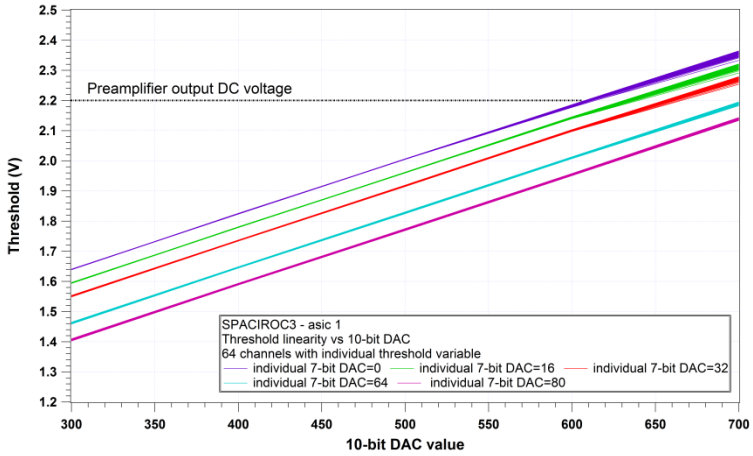


Figure 9: 64 individual DACs

The photo counting is tested by measuring the 50% trigger efficiency point when no signal is injected (pedestal measurements) or while injecting a fixed signal as a function of the threshold. The trigger efficiency is supposed to drop from 100% to 0% (so-called S-curves) in few DAC counts (if the noise is limited). Such measurements were systematically carried out for all the channels. Left part of the figure 10 represents the 64 S-curves with the same 7-bit DAC value for all channels and the right part is the same measurement with an individual 7-bit DAC set per channel.

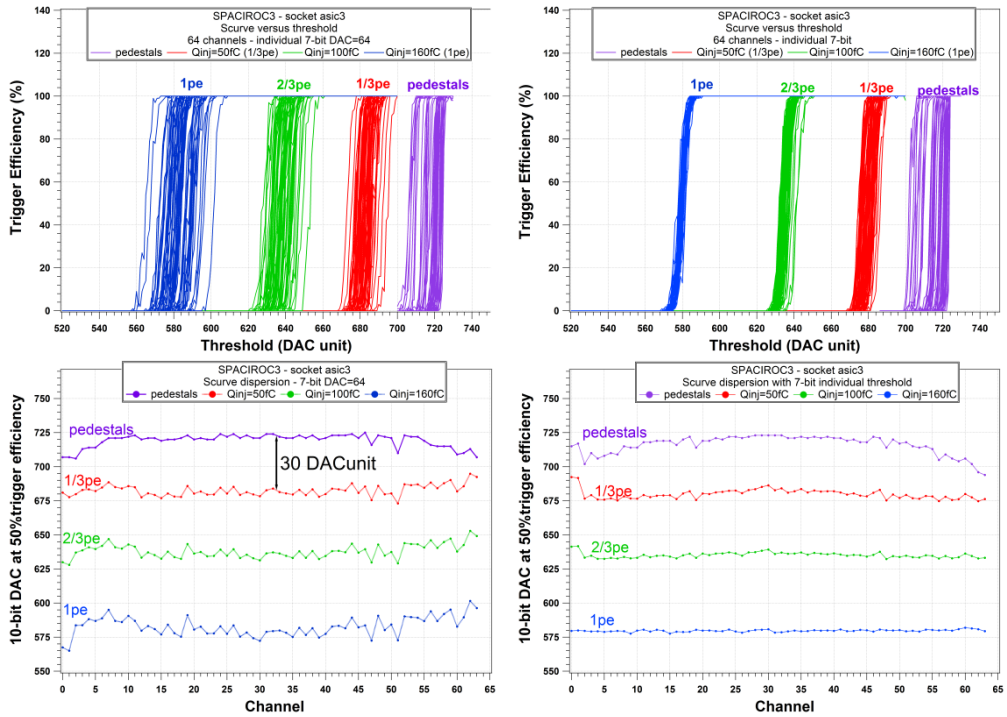


Figure 10: Photon Counting 64-channels S-curves and 50% trigger dispersion (left) S-curves without individual correction, (right) S-curves with individual correction

The 7-bit table was defined to correct the 1 pe dispersion. The S-curve dispersion at 1 pe is 0.7 DAC unit instead of 4 DAC units without adjustment.

To test the double pulse separation, a free running pulses corresponding to 1 pe are sent at different frequencies. The plot (figure 11) shows the data from the counter (acquisition of 200 GTU) as a function of the frequency. The photon counting data are consistent with the GTU multiplied by frequency and show that the ASIC can detect all the pulses contained in one GTU at 100 MHz.

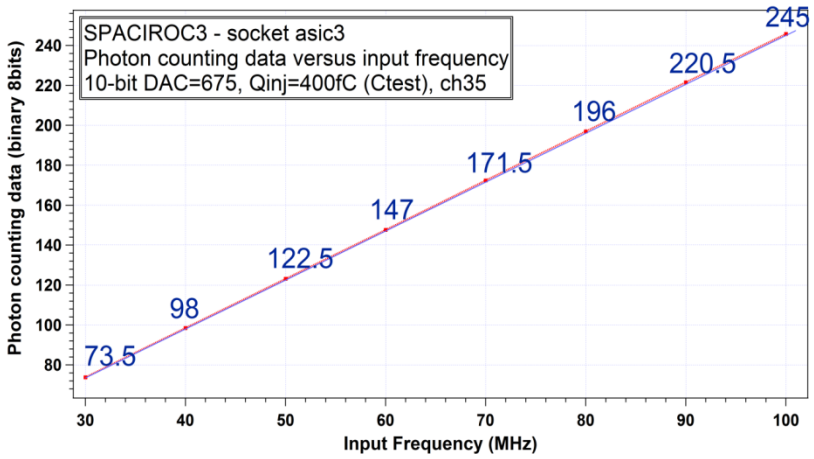


Figure11: Double pulse separation test

The figure 12 gives the linearity of one of the 8 integrators for one slow control configuration. The charge measurement starts after 3 pe/channel instead of 0 pe. It is not an issue for the JEM-EUSO application because the photon counting works very well in this dynamic range. The integrator performances are satisfying and show a good agreement with the post-layout simulations.

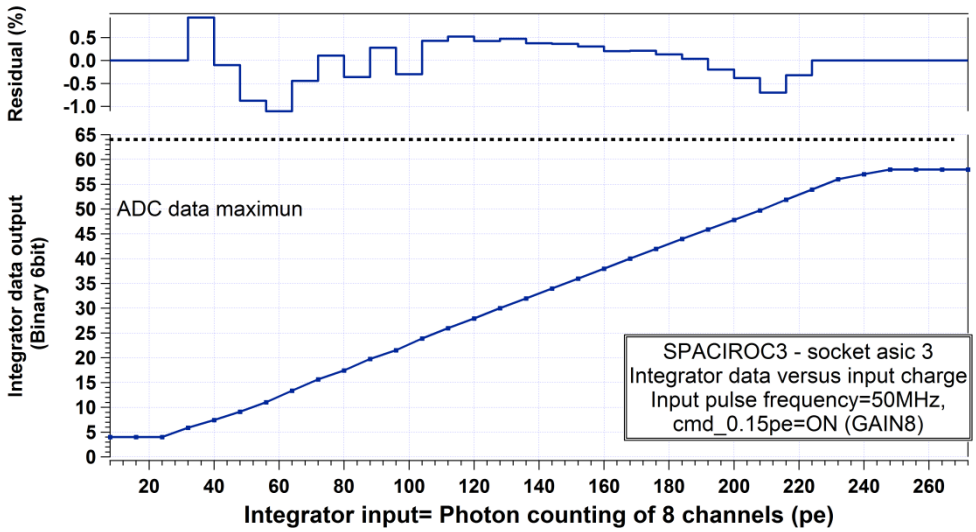


Figure12: Data from the ADC versus the input charge

## 4.Conclusions

This new version SPACIROC was designed to improve the performances and to eliminate the design bugs. The critical points which had to be improved were the power consumption, the double pulse separation resolution and the charge measurements. Intensive tests on SPACIROC3 have demonstrated good overall performances. The ASIC fulfils the requirements for the photon counting and more tests of the integrator are ongoing. Another important aspect of this ASIC is the power consumption. With the recommended settings for JEM-EUSO, the power dissipation of this ASIC is around 0.7 mW/ch. SPACIROC3 fulfils JEM-EUSO experiment requirements. The next step is to perform measurements with the MAPMT and the light inside a black box.

## References

[1] J. H Adams Jr. Et al. *JEM-EUSO collaboration*. Astroparticle Physics 44 (2013) 76-90.

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[5] S. Blin and al., *MAROC, a generic photomultiplier readout chip*, Nuclear Science Symposium Conference Record (NSS/MIC), 2010 IEEE