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Recent Status of Front-end Electronics of DEPFET Pixel Detectors for Belle II Experiment

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The Belle II experiment, which will start after 2015 at the Super-KEKB e^+e^- accelerator in Japan, focuses on the precision measurement of the CP-violation mechanism and on the search for physics beyond the Standard Model. To cope with the designed luminosity of 8×10^{35} cm^{-2}s^{-1} and considerably increased background, a pixel vertex detector (PXD) based on DEPFET sensor technology has been developed as an innermost detector. The PXD consists of two layers of DEPFET modules located at 14 and 22 mm radii from the interaction point. Each module has an active sensor area which is thinned down to 75 μm and the sensor matrices will be steered with three types of ASICs: Switcher, Drain Current Digitizer (DCD) and Data Handling Processor (DHP). Switcher chip is designed to provide steering signals to the pixel matrix of the DEPFET sensor. The DCD chip digitizes the drain currents of the pixels and the DHP chip performs the data reduction and sends the processed data to the backend electronics. All ASICs will be directly bump-bonded to the balcony of the sensor substrate. Its excellent spatial resolution (in the order of several microns) and low material budget are one of the decisive factors determining the choice of this technology for the first time. To meet the performance requirements of the PXD, we have improved the readout ASICs with different technologies. Here we report on the current status of the front-end electronics for the PXD, including the preliminary results of the first full-scale module prototype.

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1. Introduction

The Belle II is planned to be installed at the upgraded KEKB e^+e^- accelerator in Japan, which focuses on the precision measurement of the CP-violation mechanism and on the search for physics beyond the Standard Model via precise tracking of $B^0\bar{B}^0$ decays. The peak luminosity will be 8×10^{35} cm^{-2}s^{-1} and a refurbishment of the detector is currently under way to cope with such high luminosity and 10–20 times higher background than the previous experiment [1].

The Belle II pixel detector (PXD) is the innermost detector based on the DEPFET sensor technology. The PXD consists of two layers of DEPFET modules and will be installed at 14 and 22 mm radii from the interaction point (Figure 1, Left). The active sensor area is thinned down to 75 μm to keep the material budget lower and readout ASICs are bump-bonded on the rim of the sensor substrate whose thickness is about 450 μm for mechanical stability. A spatial resolution of 15 μm can be achieved with a pixel size of 50×75 μm^2, and the readout time of 20 μs for an entire frame enables to suppress pixel occupancies of less than 3%. As the readout electronics of the DEPFET sensor, three kinds of dedicated ASICs will be used: Switcher, Drain Current Digitizer (DCD) and Data Handling Processor (DHP). Switcher chip is designed to provide steering signals to the pixel matrix of the DEPFET sensor. The DCD chip digitizes the drain currents the pixels and the DHP chip performs the data reduction and sends the data to the backend electronics. In the following sections, we explain more details of DEPFET sensor principle and the readout ASICs.

2. Belle II Pixel Detector & Readout Front-ends

2.1 DEPFET Sensor Principle

A DEPFET pixel is a p-MOS transistor situated on a high-ohmic bulk (Figure 1, Right) [2]. Using the sidewards depletion technique [3], the bulk silicon is depleted in a way such that a potential minimum for electrons can be created in the region under the transistor's channel. An additional n^+ implantation deposited right below the gate of the transistor generates an extra positive space charge. This implantation together with the sidewards depletion creates a global spatial potential minimum for electrons in the pixel's surround neighborhood. The deep-n implantation is called 'the internal gate' and the presence of trapped electrons in this internal gate modulates the drain current of the transistor. The p-MOS provides in-pixel pre amplification without additional parasitic capacitances. To remove electrons from the internal gate, a short and high positive voltage pulse is applied to the clear contact which is embedded in an additional deep p-well. Via the punch-through mechanism, an electrically favorable path is created between the clear and the internal gate, hence, the electrons directly drift from the internal gate to the clear contact.

3. The Drain Current Digitizer (DCD) chip

The currents generated by a selected DEPFET row are read out by the DCD chips placed at the bottom of each half-module matrix. Each DCD has 256 analog inputs. The currently working DCD chip is denominated 'DCDB', and implemented in UMC 0.18μm CMOS technology using special radiation hard design techniques. Photomicrograph of the DCDB chip that is produced with solder bumps is shown in Figure 2. The chip occupies 3.2 mm $\times$ 5 mm area.

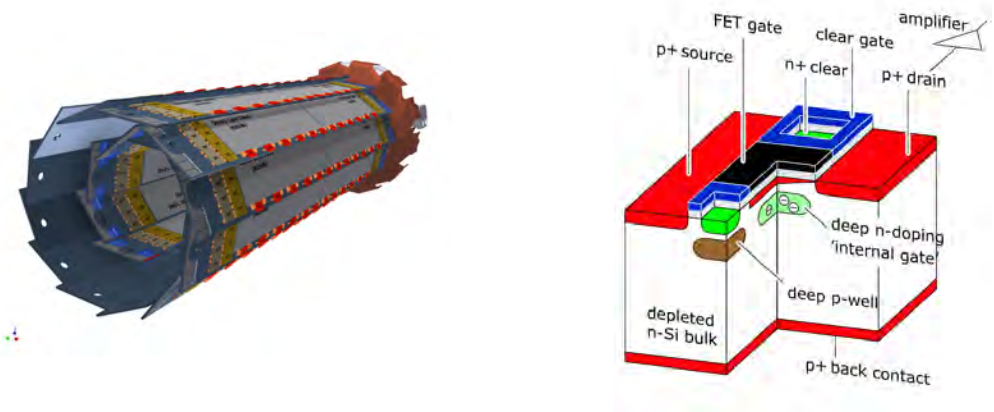

Figure 1: (Left) Geometry of the Belle II PXD which consists of two layers of DEPFET sensor modules. (Right) Cross-section of a DEPFET sensor consisting of a p-channel FET on a sideward depleted silicon bulk.

DCD has 256 analog channels and each channel houses an input stage and ADC. The analog input stage performs various tasks: it keeps the column line potential constant, which is necessary to achieve fast readout, compensates for DEPFET pedestal current variation, amplifies the signal and provides shaping for noise reduction. The analog signal is digitized by ADCs which are based on current-memory cells [4]. While the cyclic ADC has been used in the first two prototype chips, the pipeline architecture has been chosen in the last prototype to increase the sampling speed. A large synthesized digital block decodes the ADC raw data which are then transmitted to the DHP chips from parallel 8-bit digital outputs at the data rate of 320 Mbps.

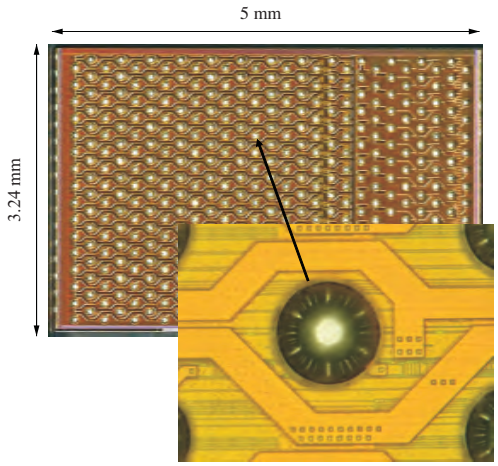

Figure 2: Photomicrograph of the DCDB chip.

4. The Switcher chip

The Switcher steering chips denominated 'SWITCHERB' will be mounted on the longer edge rim of the DEPFET module, the so called balcony. These chips are able to generate fast voltage

pulses ,i.e., 10 ns into a 100 pF load, with an amplitude of up to 50 V to activate DEPFET rows and to clear signal charges. Two variants of SWITCHERB chip have been implemented in two HV CMOS technologies, 0.18 μm and 0.35 μm AMS [5]. Photomicrographs of two SWITCHERB versions are shown in Figure 4. As we can see SWITCHERB in 0.18 μm technology is significantly smaller. Other advantages of this version are faster switching, lower power consumption and higher radiation tolerance.

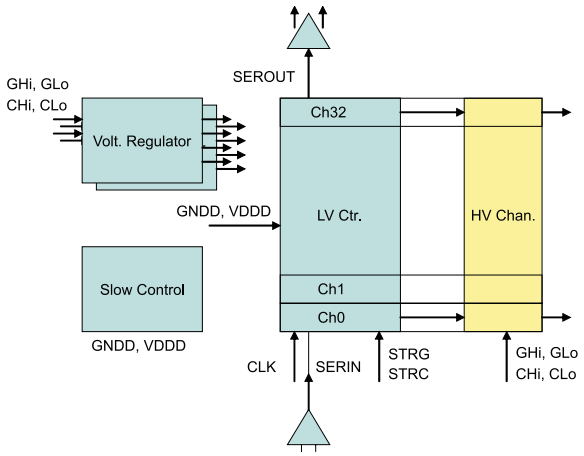

Figure 3: Block diagram of the SWITCHERB chip.

Readout of one DEPFET half-module with 768 pixel rows will require six SWITCHERs, each with 32 channels. The block diagram of the chip is shown in Figure 3. The basic blocks consist of:

- 32 high-voltage channels (level shifters) that generate each two high-voltage signals. These blocks implement fast high-voltage output drivers. Static current consumption in idle state is several μA.
- Low-voltage control block (based on shift register) used to select the high-voltage channels.
- Voltage regulators (two per chip) each generating 4 auxiliary high-voltage supplies out of four externally generated main supply voltages.
- Slow control block based on JTAG.

The outputs of high-voltage channels switch between upper (CHI, GHI) and lower voltages (CLO, GLO), respectively. The voltage swing can be up to 50 V for SWITCHERB in 0.35μm and 20 V SWITCHERB in 0.18 μm technology. The low-voltage control block and the slow control part are supplied by an additional "floating" 1.8 or 3.3 V supply (GNDD, VDDD). Channels are activated one after other by means of a shift register which a part of low-voltage control. It is fed with a single "1" externally through its serial input. This "1" is clocked through the channels. The high-voltage drivers are activated for the selected channel by fast STROBE signals. Several chips can be daisy chained by connecting the serial output to the serial input of the next chip. The chip is bump bonded to the sensor. Fast timing is provided by a few differential control signals.

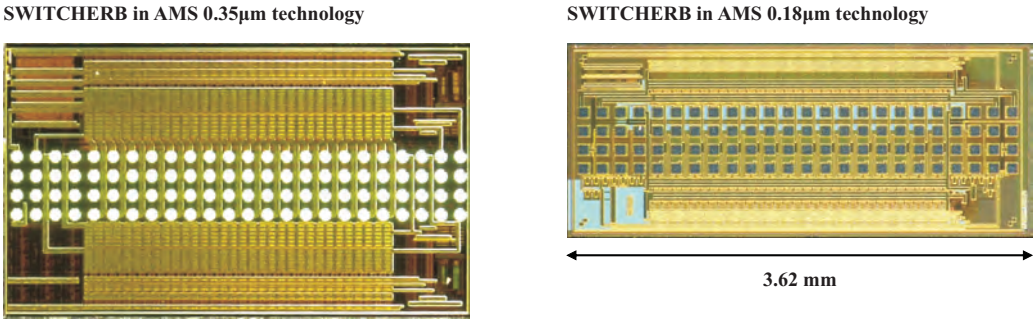

Figure 4: Photomicrograph two SWITCHERB versions. Left picture shows the chip implemented in 0.35 μm AMS technology, right picture shows the chip in 0.18 μm technology.

4.1 The DHP (Data Handling Processor) chip

4.1.1 Data Processing Blocks

The layout of the newest version of the DHP chip is shown in Figure 5 (Left). This chip is denominate 'DHPT 1.0' was implemented in the TSMC 65 nm CMOS technology, while the previous chip implemented in the IBM 90 nm CMOS ('DHP 0.2') is used for the following full-scale module prototype testing. The main task of the chip is data reduction. The block diagram is shown in Figure 5 (Right). First, the data from the DCD are deserialized. The 256 input channels of the DCDB chip are organized in 8 double-columns with 32 ADC outputs each. Each column has one 8-bit wide output link. This makes in total 64 outputs connected to DHP inputs. The data transmission runs at 305 MHz clock rate and 32 DCD clock cycles are necessary for each row. The received data is reorganized and written row-by-row into the raw memory data buffer. The buffer has a depth of one frame and is designed as a ring buffer. This ring buffer serves as a programmable delay element for further data processing which starts upon trigger arrival from the outside. The estimated trigger latency is expected to be about 5 μs, corresponding to $\sim$50 rows with 100 ns sampling time and thus the current ring buffer has a maximal depth of 256 rows.

Together with the raw-data buffer, the DHP chip contains the pedestal memory storage of equal size and pedestal currents are subtracted from the raw data. After pedestal subtraction, the subtraction of the common mode (CM) noise is performed. The CM is the noise component, whose amplitude is the same for all values sampled at the same time. This subtraction is done before the zero suppression, where the threshold cut is applied. As an algorithm to estimate the CM noise, the two parse average was chosen: the averaging procedure is executed twice. First a rough estimation of the CM is taken as a simple average ($\tilde{CM}$) of a row. Then the first signal detection step takes place by applying the threshold: if a signal is detected, the signal is removed from the $\tilde{CM}$ estimation. Then the average can be taken again and, within the digitization limit, this gives the unbiased CM and hit signals. The output data is split into blocks of 16-bit words and organized in frames. Each frame starts with a header containing the information about the type of data in the frame. To parse the data, each word has a flag telling what kind of information is packaged. Each generated zero-suppressed data is encapsulated into Aurora frames using a special protocol, where the data is additionally 8b/10b encoded.

4.1.2 Custom Blocks

In the DHP, several custom blocks are implemented. The Phase Lock Loop (PLL) is used to generate the internal clock of 1.53 GHz for data processing from the externally provided clock of 76.32 MHz. The basic topology is inherited from the pixel front-end chip (FE-I4) for the upgraded Atlas pixel detector. The output of the DHP data is sent at the data rate of 1.53 Gbps to the backend electronics. For such a high data rate, Current Mode Logic (CML) output driver was implemented in the chip. This circuit consists of two differential pairs and one of them is used for the pre-emphasis. The basic idea of the pre-emphasis is boosting the high-frequency components and cancel with the low-pass characteristics of the transmission cable. More information about the actual implementation for the PLL and CML driver can be found in [6].

With the exception of the serial link with the CML transmitter, all other signals between the DHP and backend module are driven by custom-made LVDS transmitters and receivers. Programmable current sources are implemented in this custom LVDS driver to reduce the power consumption of the chip. In addition to that, a temperature sensor using the intrinsic diode temperature dependence was implemented to measure the external temperature.

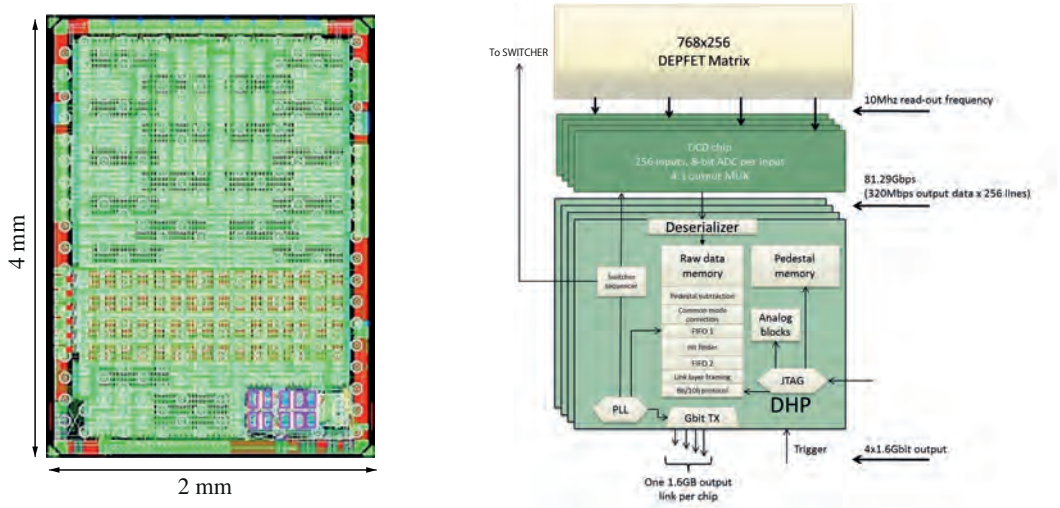

Figure 5: (Left) A layout of the newly developed DHP chip with TSMC 65 nm CMOS. (Right) Block diagram of the DHP chip.

5. Hybrid Module & Test Results

5.1 Full-scale Module Prototype of the PXD

The full-scale module prototype depicted in Figure 6 (Left) has been designed as the first prototype of a PXD module, containing the minimum amounts of all necessary components: one small DEPFET matrix, one SWITCHERB, one DCDB, and one DHP. A custom-made PCB called Hybrid-5 has been designed to host three kinds of ASICs and interconnect their inputs and outputs with the readout system. For a handling issue, a wire bond adapter sits on the PCB which provides interconnection between the bump and wire-bond pads. The backend electronics is emulated in the FPGA board. The Hybrid-5 is controlled from a user's PC via the FPGA board through an

Ethernet cable, and chip configuration is done by a JTAG core. For a user to receive the Hybrid-5 output data, Aurora frames are converted into UDP packets [1] and sent to the control PC. The control firmware is written using HDL language with a use of the Microblaze soft-core processor allowing executive C/C++ programs. This hybrid solution combines the flexibility of a software written code and the speed performance of the hardware modules (see [7] for detailed description).

5.2 Laser scan and IR-source irradiation

A laser scan was performed to determine the correspondence between the physical pixel position and the internal coordinates of the DHP chip after zero-suppression. In the measurement, the small DEPFET matrix with 32×64 pixels was connected to the DCDB chip. Each pixel has a size of 50×75μm^2, corresponding to the total area of 1.6×4.8 mm^2. Figure 6 (Right) shows the matrix image. Since the matrix was illuminated from the back-side, the non-transparent metallization area can be seen in a blue rectangle. In the right figure, a precision scan of the 4×6 pixels is shown. Thanks to the sub-pixel precision with a step size of 10 μm, the high and low sensitivity areas of the matrix can be observed. From the figure, the position dependent of the cluster signal is estimated as ∼10%.

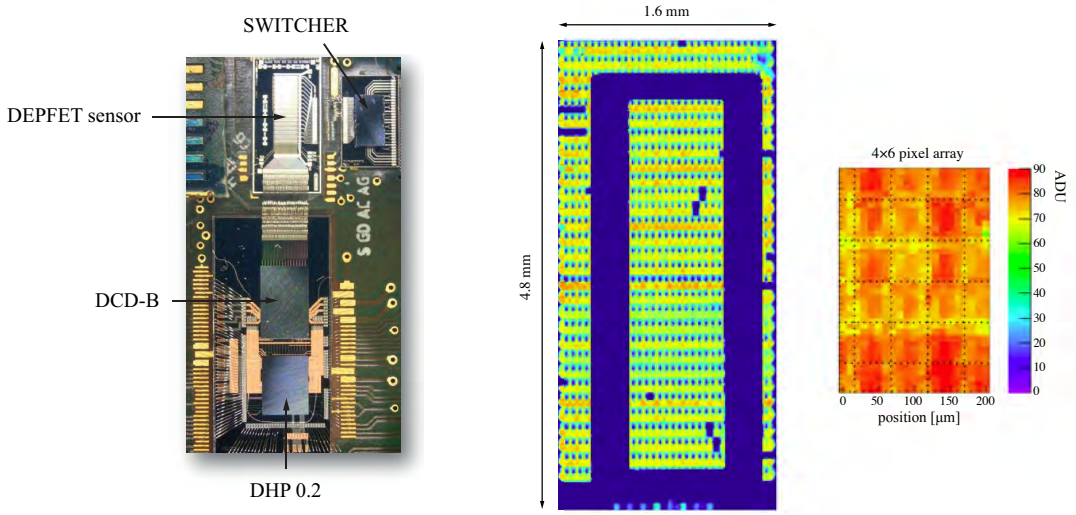

Figure 6: (Left) A picture of the full-scale module prototype, including a small DEPFET matrix, one SWITCHER, one DCDB, and one DHP0.2. (Right) The matrix image of the laser scan from the back-side. The metallization area can be seen as a blue rectangle. Right picture shows a precise homogeneity scan result of the 4×6 pixel area with a step of 10 μm.

5.3 Test beam

The test beam measurement was performed at DESY in May 2013 to prove the performance of Hybrid-5 with its full processing chain. The test setup was mounted using the DATURA EUDAQ telescope with six reference planes for tracking reconstruction. The Hybrid-5 was the device under test and was situated in the center of the telescope. Two scintillators were installed in front and

[1] User Datagram Protocol, a simple transmission protocol belonging to the standard Internet protocol family.

behind the telescope. Upon simultaneous event detection by all reference planes and scintillators, the Trigger Logic Unit (TLU) issues a trigger for the device under test. This allows for a precise track reconstruction to measure the detector efficiency and spatial resolution. Figure 7 (Right) shows the example of the first ten million events recorded by the system. From the expected energy deposition, the conversion gain of the sensor is estimated as $g_q = 450\ \mathrm{pA/e^-}$.

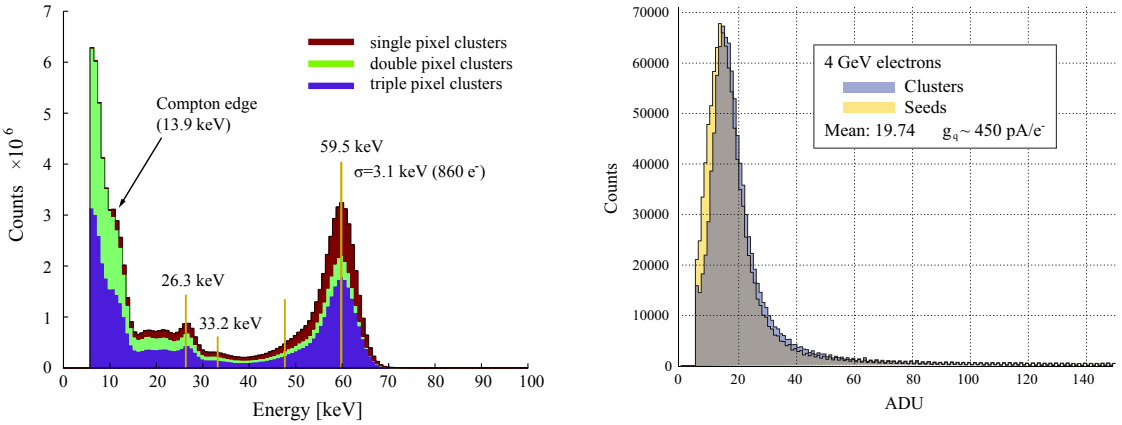

Figure 7: (Left) Spectrum of ^{241}Am obtained with the trigger-less mode. (Right) Histogram of the signals from 4 GeV electrons.

6. Conclusion & Outlook

The Belle-II pixel detector (PXD) has been developed based on DEPFET technology. The PXD requires three types of steering front-end electronics. The architectures and functionalities have been proven in the previous lab testing for the Switcher and DCD chips. The development of the DHP chip is currently imperative. The full size DHP chip has been designed in 65 nm CMOS technology and the chip is currently under testing. This chip is expected to be the production chip version, suitable for assembly on PXD modules. Measurements in the labs and beam test revealed a successful operation of the entire sensor and electronics system. Based on all the test carried out with the latest prototype design, the production of the final sensors for the Belle II experiment have already started and the first ones are expected to be ready in the end of 2014.

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