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A fast, low-power, multichannel 6-bit ADC ASIC with data serialisation

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The multichannel 6-bit ADC ASIC with data serialisation was designed in view of readout systems in future HEP experiments. The first prototype was designed and fabricated in CMOS 130 nm technology. The main components are: 8 channels of fast, very low power (∼0.35 mW per channel) 6-bit SAR ADCs, data serialisation circuitry based on ultra-low power internal PLL, and fast SLVS I/O differential interface. The nominal ADC sampling frequency is 40 MHz but the operation up to 80 MHz is possible. The ultra-low power (<1 mW) PLL was designed to generate clock in a wide frequency range of 20 MHz–1.6 GHz. The SLVS interface was designed for data rates above 1 GHz.

Various modes of data serialisation were implemented, the main three are: test mode – with 6 bits from the selected ADC sent to six SLVS differential outputs; partial serialisation – when output bits of each ADC are serialised, with frequency multiplied six times by PLL, into one dedicated SLVS output; full serialisation – when output of all bits (6) of all ADCs (8) are serialised into single SLVS output. It was verified that all modes are fully functional.

Preliminary measurements showed that the ADC performance, the ENOB in particular, does not depend on the channel or readout mode and is always above 5.75.

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1. Introduction

Future particle physics experiments will require more functionality in the readout systems of particle detectors. In particular, front-end electronics is expected to perform more signal processing than it is usually done in present readout systems. A natural solution to this aim is to comprise signal digitisation in each front-end channel and add the required digital signal processing in the front-end Application Specific Integrated Circuit (ASIC). Such solution greatly increases the complexity of the front-end ASIC since it requires a few additional highly efficient blocks: a multichannel Analog to Digital Converter (ADC) for signal digitisation; a serialisation circuitry to limit the number of output pads at the cost of higher frequency of signal transmission; and a Phase-Locked Loop (PLL) for high frequency clock generation. To fulfil the stringent requirements of present and future readout systems the ADC: should be fast enough to sample subsequent events, e.g. at LHC experiments 40 MS/s would be typically required; should occupy small area to fit into the pitch/size of front-end ASIC; and should consume very low power to not increase largely the power consumption of front-end ASIC. The requirement of very low power consumption applies also to the PLL and serialisation circuitry.

In this paper we show the design and measurement results of the first prototype of an ASIC comprising eight ADC channels, a PLL and a serialisation circuitry. A preamplifier-shaper blocks are not yet added to this prototype for two reasons. First, the precise testing of ADC performance requires direct access to ADC input pads. Second, the functionality of the developed digitisation-serialisation blocks is independent of the preamplifier-shaper type and may be used in combination with any analogue front-end. In the developed systems we decided to use 6-bit Successive Approximation Register (SAR) ADC since we have already developed such high performing block for the LHCb Upgrade tracking system [1]. We also used the PLL block developed recently and described in [2].

2. ASIC architecture and main blocks

The multichannel ADC ASIC with fast serialisation was designed in 130 nm CMOS technology. Its general architecture is presented in figure 1, where the layout of prototype ASIC is shown. The prototype contains: 8 channels of 6-bit SAR ADC, the digital readout circuitry (multiplexer and serialiser), the PLL for generation of high frequency readout clock, the Scalable Low-Voltage Signaling (SLVS) I/O circuitry, and staggered input and output pads. There is also a command decoder (not marked in figure 1) controlling the operation of the entire ASIC.

The SAR ADC architecture and the performance of a single ADC channel was already presented in details elsewhere [1, 3]. Here we give only a brief summary. The ADC is fully differential, uses capacitive segmented Digital to Analog Converter (DAC) network, and works in Merged Capacitor Switching (MCS) [4] scheme. These choices were motivated mainly by the requirement of low power consumption. To lower the power even more and to completely eliminate static power a dynamic comparator is used and an asynchronous control logic is implemented. With such solution no other means are needed to provide power pulsing feature, which is required by many high energy physics applications. Single channel performance was measured in detail, giving Effective

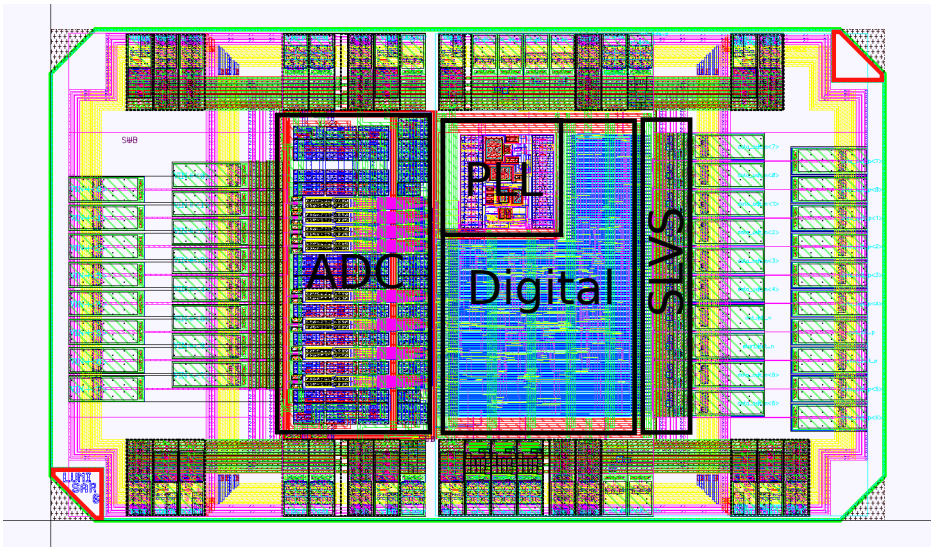

Figure 1: Layout of the ASIC, die size 2340x1380 μm

Number Of Bits (ENOB) of 5.85 together with power consumption of 0.35 mW at 40 MS/s. The sampling frequency can be increased up to 80 MS/s keeping the ENOB higher than 5.8.

The PLL block was designed as general purpose PLL [2]. It works in a very wide output frequency range from 20 MHz up to 1.6 GHz. So wide range is possible because the internal Voltage Controlled Oscillator (VCO) has 16 gain modes, which can be changed automatically or manually. The jitter was measured to be between 15-70 ps, and it is planned to be improved in next prototype. Power consumption at 1 GHz is 0.6 mW. The PLL may be configured to use four different division factors in the feedback loop: 6, 8, 10, and 16. Two of them i.e. 6 and 8 are used in the readout modes described in the next section.

It may be observed in figure 1 that four ADC channels are placed close to each other (40 μm pitch) while other four in twice larger distance (80 μm pitch) with additional decoupling in between. This was done in order to study the effect of pitch/decoupling on crosstalk.

3. Multichannel ADC readout modes

The block diagram of a readout circuitry is shown in figure 2. The readout can operate in three different modes: test, partial serialisation and full serialisation. In the test mode only one ADC sends its output bits to six SLVS output drivers. In the partial serialisation mode each ADC has its own serial output while in the full serialisation mode all ADCs send the data into one SLVS output. To perform serialisation at least two clocks are needed: the slow one before and the fast one after the data serialisation. The required clock frequencies can be obtained in two ways: either by dividing fast clock or by multiplication of slow one (see figure 2, left). Both possibilities are implemented in the prototype ASIC. In the first case a fast clock is delivered to the ASIC and then divided, while in the second case the slow external clock is multiplied by the PLL.

In the test mode only one SAR ADC can be read at a time. No serialiser is used and 6 bits of a selected ADC are sent out through the six SLVS outputs with a frequency of slow external clock

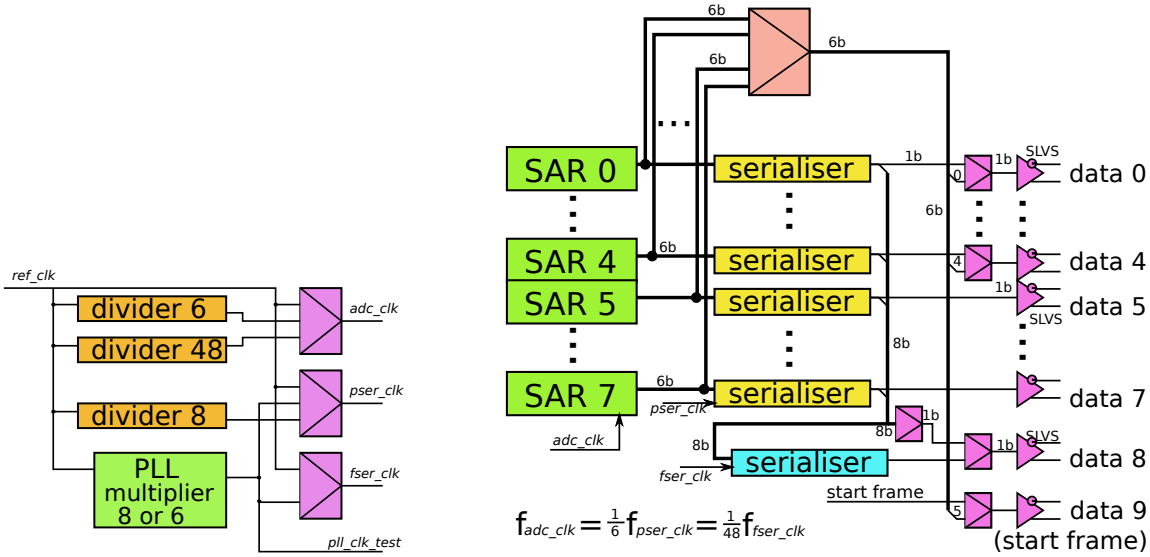

Figure 2: ASIC readout: clock generator (left) and readout block diagram (right)

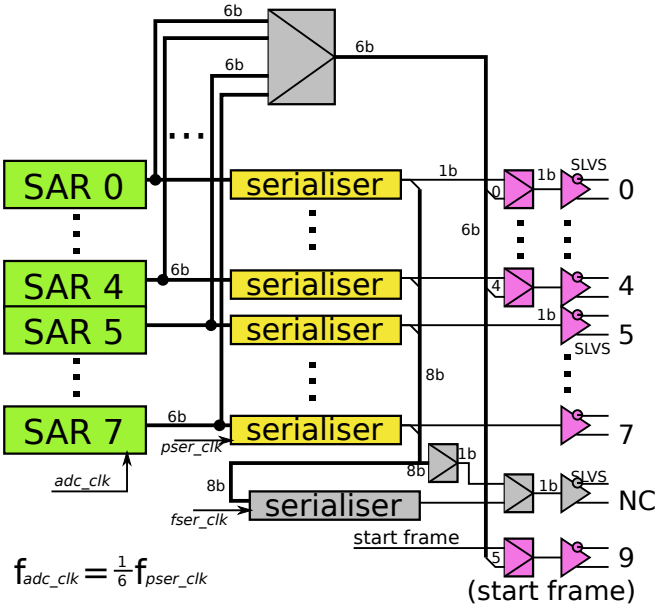

Figure 3: Readout configuration in partial serialisation mode (inactive elements in grey)

(the same which is used for sampling). All measurements presented in [1, 3] were done in this mode.

The configuration of readout in the partial serialisation mode is shown in figure 3. Each ADC channel has its own serial SLVS output and eight ADC channels are readout in parallel. As a consequence, this mode needs two clock frequencies: the slow for sampling and the fast (six times faster) for readout. Two alternative clock generation schemes are available in this mode as shown in figure 4. In the left diagram a scheme with division of fast external clock is shown. High frequency external clock, which is a readout clock, is delivered to the ASIC and divided by six to obtain the

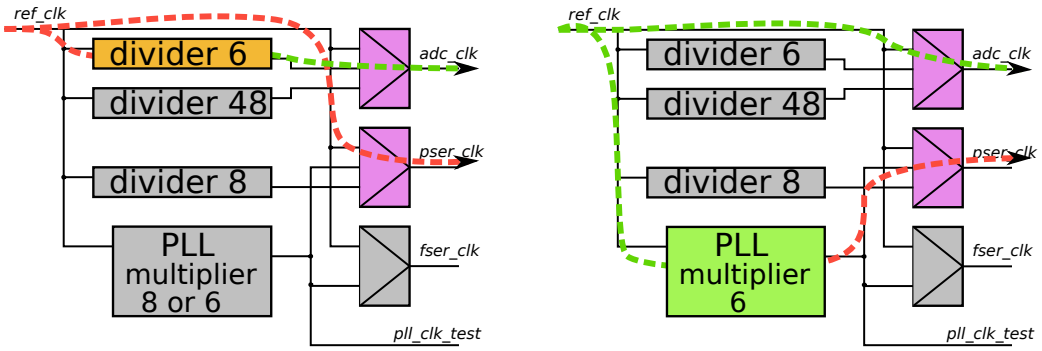

Figure 4: Clock generation in partial serialisation mode (inactive elements in grey): readout clock applied externally (left), generated by the PLL (right)

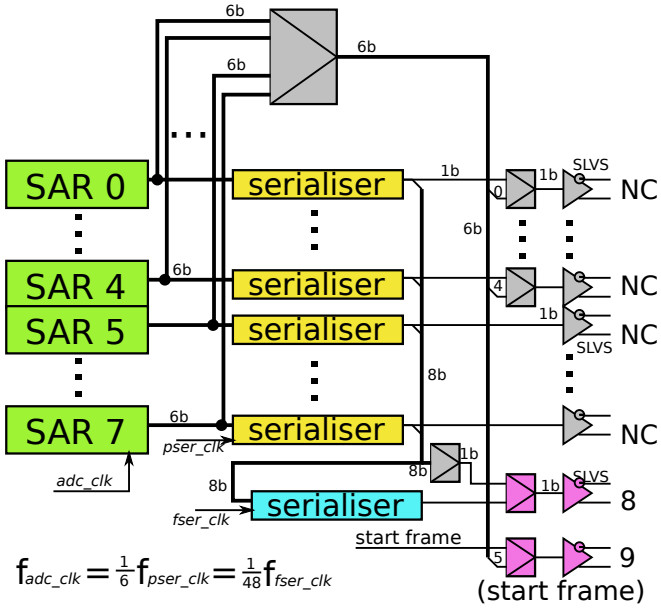

Figure 5: Readout configuration in full serialisation mode (first level of serialisation in yellow, second level in cyan, inactive elements in grey)

sampling clock. In the right diagram the sampling clock delivered externally is multiplied six times by the PLL to get the fast readout clock.

The most complicated readout mode is the full serialisation mode. In this mode, shown in figure 5, all channels are read out via a single SLVS output. The full serialisation mode uses two levels of serialisation. As a consequence three clock frequencies are needed: a sampling clock, a first serialisation level clock and a readout clock. Two configurations of clock generation circuit for the full serialisation mode are shown in figure 6. Similarly as in the partial serialisation mode there are two possibilities: to deliver the fastest clock to the ASIC (left diagram in figure 6) or to create it with PLL (right diagram in figure 6). However, in the configuration with PLL the medium frequency clock is delivered externally and multiplied by eight in PLL to obtain the fast readout clock. The external clock is also divided by six to obtain the slow sampling clock.

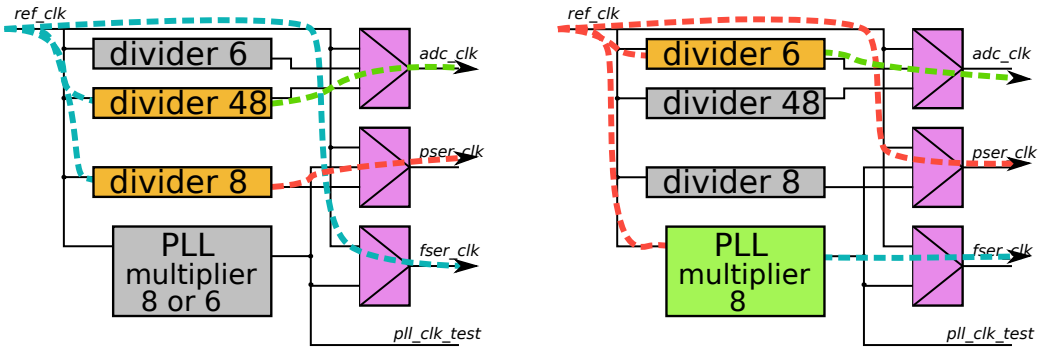

Figure 6: Clock generation in full serialisation mode (inactive elements in grey): readout clock applied externally (left), generated by the PLL (right)

4. Measurements results

A dedicated Field Programmable Gate Array (FPGA) based test setup was developed for multichannel ADC measurements. Differential clock and sinusoidal input signals were delivered to the ASIC from the Agilent 81150A generator. Digital SLVS ADC outputs were readout by the FPGA. To measure dynamic performance a Fast Fourier Transform (FFT) spectrum was calculated for each ADC. To satisfy precision requirements, 512 samples were used as FFT input. The Signal-to-Noise And Distortion ratio (SINAD) was calculated and converted to the ENOB. During the measurements all eight ADC channels were always read, but because of limitation in the present setup the sinusoidal input was sent only to two channels at the same time. Typically channels 1 and 6 were used in order to have one channel with 40 μm pitch, one with 80 μm pitch, and to avoid boundary channels. The tests were performed in two ranges of sampling frequency: up to 7 MHz (for partial and full serialisation modes) and up to 50 MHz (for partial serialisation only).

The scan over input frequency measured at 6.8 MHz sampling frequency for all four possible readout modes and clock configurations is shown in figure 7. In all cases the results are almost identical, what means that the ADC performance is not affected by the readout mode or clock configuration.

In the next measurements the ENOB uniformity over ADC channels was verified. The ENOB obtained in the partial serialisation mode at 45 MHz sampling and Nyquist input frequency is shown in figure 8. Excellent and uniform ENOB over all channels is seen. Following this measurement, the maximum ADC sampling frequency was measured in the partial serialisation mode for each clock configuration. It was verified that with the fast external clock ADCs work well up to 55 MHz sampling frequency and with the PLL they work up to 60 MHz. Since we know, from the test mode measurements, that single ADC works well up to 80 MHz, the maximum sampling frequency obtained in the partial serialisation mode is limited not by ADCs but by the digital readout. From the obtained results it may be concluded that the maximum readout frequency is between 330–360 MHz. However, we should admit that for certain sampling frequencies beyond 40 MHz (readout beyond 240 MHz) communication problems appeared for some of the channels.

One of the main requests in a multichannel system is to eliminate crosstalk effects. We have done first estimation of crosstalk effects sending the full range sinusoidal signal to selected channel and measuring the standard deviation of samples recorded on neighbour channels. The results of

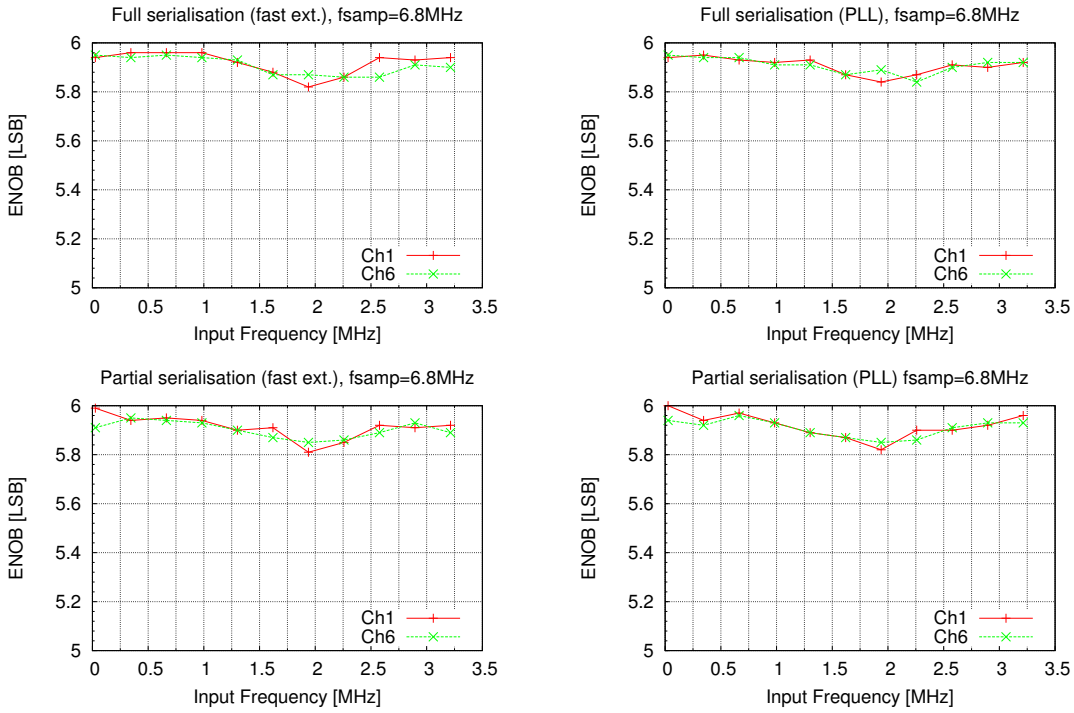

Figure 7: ENOB vs input frequency, at 6.8 MHz sampling frequency, in partial and full serialisation modes, with fast external clock (left column) and with the PLL (right column)

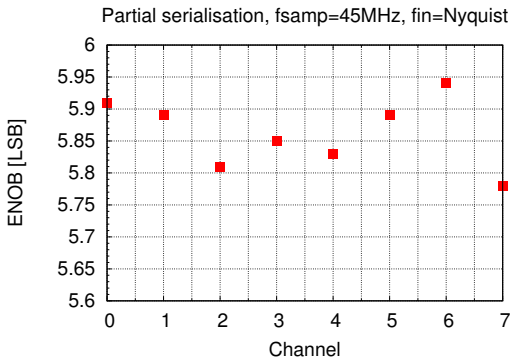

Figure 8: Channels uniformity; ENOB measured using pairs of channels (present setup limitation): (0,7), (1,6), (2,5) and (3,4)

such measurements, performed at 30 MHz sampling frequency are shown in figure 9. We choose 30 MHz in order to disentangle the crosstalk effect from the communication issues seen for some sampling frequencies beyond 40 MHz. In figure 9 we present the situation when signal is sent to channel 1 (40 μm pitch) and to channel 6 (80 μm pitch). It is seen that for channels 4–7 (80 μm pitch) no crosstalk effect is seen. On the contrary, for channels 0–3 (40 μm pitch) small crosstalk, of the order of 0.5 LSB, is observed. More measurements are needed to understand whether it depends on sampling frequency or other parameters, but from the obtained results it is already seen that ADC channel separation and decoupling are very important in a multichannel system.

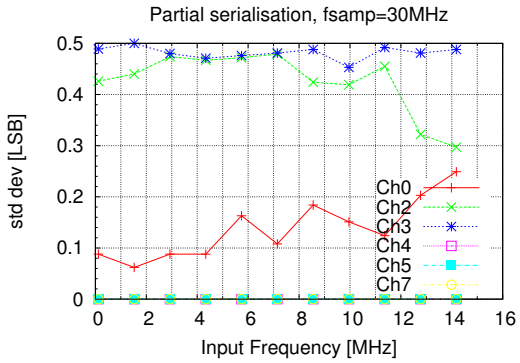

Figure 9: Crosstalk effects at 30 MHz sampling frequency; signal in channels 1 and 6

5. Conclusions

The multichannel ADC ASIC with fast serialisation was designed, fabricated, and preliminary tests were done. All 8 channels of the prototype ASIC were found fully functional and showed excellent resolution with the ENOB above 5.75. All readout modes, the test mode, the partial serialisation mode and the full serialisation mode work very well, without affecting the ADC parameters. The same is true for the configuration of readout clock generated by the internal PLL or delivered externally. The digital readout works up to 330–360 MHz, limiting the ADC sampling frequency to about 60 MHz, in partial serialisation mode. First measurements of possible crosstalk effects were performed, showing that for distant channels with good decoupling no crosstalk is observed. Detail studies of crosstalk, power consumption of the whole ASIC, etc., are foreseen in the near future.

6. Acknowledgments

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