Design and development of the Power Converter Board within the Digital Optical Module in KM3NeT

E. Anassontzis

Faculty of Physics, National Kapodistrian University of Athens, Greece
E-mail: eanason@phys.uoa.gr

A. Belias

Institute of Nuclear and Particle Physics, NCSR Demokritos, Athens, Greece
E-mail: belias@inp.demokritos.gr

E. Kappos

Institute of Nuclear and Particle Physics, NCSR Demokritos, Athens, Greece
E-mail: ekappos@otenet.gr

K. Manolopoulos[*]

Institute of Nuclear and Particle Physics, NCSR Demokritos, Athens, Greece
E-mail: kmanolo@inp.demokritos.gr

P. Rapidis

Institute of Nuclear and Particle Physics, NCSR Demokritos, Athens, Greece
E-mail: rapidis@inp.demokritos.gr

on behalf of the KM3NeT collaboration

KM3NeT is a deep-sea neutrino telescope of very large scale (several km^3) to be deployed and operated in the Mediterranean Sea. Neutrino-induced charged particles are detected by measuring their Cherenkov light in sea-water, using Photomultiplier Tubes inside transparent, pressure resistant spherical enclosures. The aim is to instrument several km^3 of sea volume with tens of thousands of optical sensors, connected to the shore through electro-optical cables up to 100km. The KM3NeT collaboration has successfully developed an optical sensor, the Digital Optical Module, by placing 31, 3-inch Photomultiplier Tubes in a 17-inch glass sphere along with the readout electronics. Each Digital Optical Module is supplied power through a high voltage (400VDC) line, converted to low voltage (12VDC) in a breakout box before entering the Digital Optical Module. The Power Converter Board, situated inside the Digital Optical Module, is used to produce seven voltage rails as required by the Digital Optical Module electronic modules. This paper summarizes the design considerations and implementation of the Power Converter Board and the results of the trial runs so far.

[*]Speaker.

1. Introduction

The main objective of the KM3NeT collaboration [1] is the design, construction and operation of a deep-sea research infrastructure in the Mediterranean Sea, including a very large volume neutrino telescope based on the optical Cherenkov technique (Fig. 1). To detect the Cherenkov light generated by neutrino-induced charged particles in the deep-sea, we use Digital Optical Modules (DOMs) [2], each consisting of photomultiplier tubes (PMTs) inside a pressure resistant glass sphere. Immersed in the deep sea, the Digital Optical Modules will operate under central control from the shore, and all digitized data from each DOM will be sent to shore. Each DOM will be linked to the shore through a photonic network with different throughput requirements for the upstream (DOM-to-shore) and downstream (Shore-to-DOM) data transmission. In this paper, we describe the functionality, the design and the implementation of the Power Converter Board (PB) that is located inside each DOM.
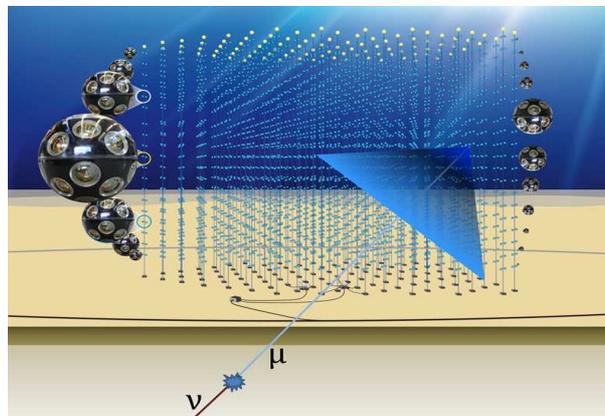
Figure 1: An artistic impression of the KM3NeT.

2. KM3NeT Power Architecture

Each DOM is powered by an electro-optical cable carrying power and optical communications. DOMs are arranged in vertical columns called Detection Units (DUs) consisting of 18 DOMs each. The telescope consists of a grid of such DUs (Fig. 1). Each DU is connected via a 100m deep-sea cable to a central junction box which receives power via a long distance high-voltage cable to shore. To minimize ohmic losses in the power cables and reduce copper diameter, 400VDC was chosen as the voltage for the deep-sea power bus from the DUs to the junction box. The 400VDC bus is converted to an intermediate 12VDC bus before entering each DOM. The 400VDC/12VDC power converter for each DOM is housed in an external oil-filled, pressure balanced enclosure, connected to the DOM by a short 60cm cable. The external converters isolate galvanically the DOMs from the 400VDC cable network providing safety against failure and flooding of any DOM to the other units in the network. The intermediate 12VDC bus voltage provides optimal conversion efficiency between the 400VDC external bus and the internal DOM power rails ranging from 1V to 5V.

3. DOM Power Architecture

The DOM sphere contains several electronic modules such as a Central Logic Board (CLB) built around a high performance FPGA, electronics for the 31 Photomultiplier Tube bases, optical communications as well as several instrumentation modules including an acoustic piezo-sensor for the DOM positioning system, compasses and tilt-meters to monitor the orientation of PMTs, temperature and humidity sensors, and an LED beacon for timing calibration. The PB receives power from the 12VDC intermediate bus voltage and produces six low-voltage power rails for the FPGA and the peripheral modules mentioned above and one programmable high-voltage rail for the LED beacon. Non-isolated point-of-load (POL) DC-DC converters are used for the six step-down rails, and a step-up discrete regulator for the step-up LED beacon rail.

The DOM mechanical design, where 31 PMTs are fitted within the limited space of a 17 inch diameter sphere (Fig. 2), imposes strict constraints on the form factor of the PB as well as the other modules. As a result the PB must be disk-shaped, 130mm in diameter, with a 26mmx26mm opening in its center (Fig. 3). The bottom side of the board is clear of components so that a thermal interface pad can be fitted between it and the aluminum frame where it is attached. The frame at that point is shaped as a solid spherical cap, making full contact with the inner surface of the DOM glass sphere. This maximizes the heat flow to the surrounding sea water where the ambient temperature is constant at around $14°C$, forming a heat sink for the thermal losses of the POL converters. This advantage, resulting from the fact that all POL converters are located on the same board instead of being close to their loads, more than offsets the minor power distribution losses over longer distances within the DOM. The FPGA board plugs into the PB by means of three board-to-board connectors. Two of these connectors are used for the power rails and the third for the 12VDC bus input, the LED beacon rail and diagnostic signals.

Figure 2: The KM3NeT Digital Optical Module (DOM).

4. Power Converter Board

The most important criteria in the design of a multi-rail power converter are its unit cost, conversion efficiency, reliability, size constraints, dynamic response, output ripple and noise level, power sequencing, RF emissions, acoustic noise, and heat dissipation. In addition, initial development costs in terms of design effort and the time needed to produce the first working prototypes
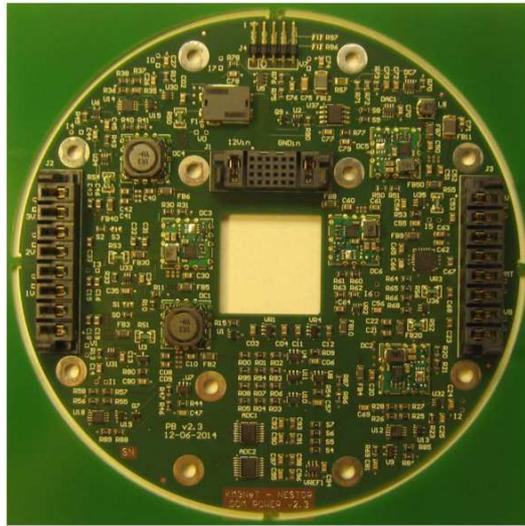
Figure 3: The DOM Power Converter Board.

are often very important. In our case, cost and power conversion efficiency were very important considerations at the outset, due to the relatively large number of DOMs (of the order of 10,000) planned for the entire telescope. A minor increase in DOM power consumption, compounded by conversion and distribution losses over the long-distance high-voltage lines, translates to a significant increase in on-shore power capacity and total energy cost over the entire service life of the telescope, typically 10 to 15 years for such large scale physics experiments.

The reliability of the electronic components was also of paramount importance due to the inaccessibility of DOMs in the deep sea, the high costs of recovering and replacing any faulty DOMs, and their long service life of at least 10 years. Effective thermal management to minimize temperature rise, de-rating of susceptible components, use of quality assured components, keeping the circuits simple and using the minimum number of components were some of the design objectives set in order to improve reliability. For instance, only ceramic capacitors are used for decoupling, with a de-rating factor of 60% or better. Stress screening and burn-in tests are also envisaged for the final product. To ensure final quality, the design of the PB adheres to the guidelines of the FIDES reliability standard used in KM3NeT (http://www.fides-reliability.org/).

In addition to the above primary considerations, it was desirable to use readily available commercial off-the-shelf components (COTS) in combination with a modular design approach for flexibility in implementing future design changes, arising, for instance, in case of component obsolescence or procurement problems. This precluded the use of complex, highly specialized components such as digital buck PWM controller ICs capable of controlling multiple power stages with a high degree of configurability, sequencing and tracking (e.g. TI UCD9240).

Flexibility in implementing design changes was also important in view of the fact that the load requirements for each rail were likely to change as the detailed design of the various DOM electronic subsystems was progressing in parallel with the PB design and development. For this reason, it was decided to implement two versions of the PB. A pre-production version, to be used only dur-

ing the development phase of the DOM, enhanced with capabilities for measuring in real time the power of each rail, and a production version without such capabilities in order to obtain the maximum power conversion efficiency. The pre-production version could be used as a dynamic power profiling tool for various DOM modules under development, to provide feedback in optimizing the PB design, especially the parameters determining the power conversion efficiencies.
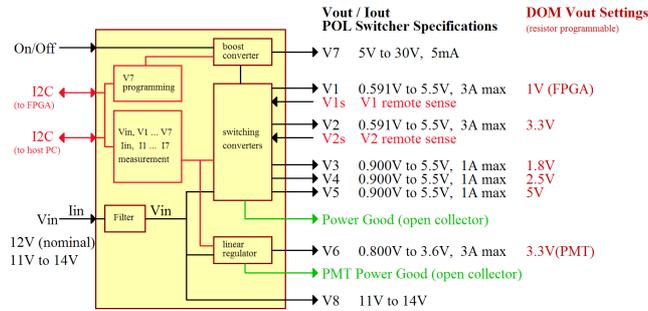

Figure 4: I/O block diagram and rail specifications of the Power Converter Board.
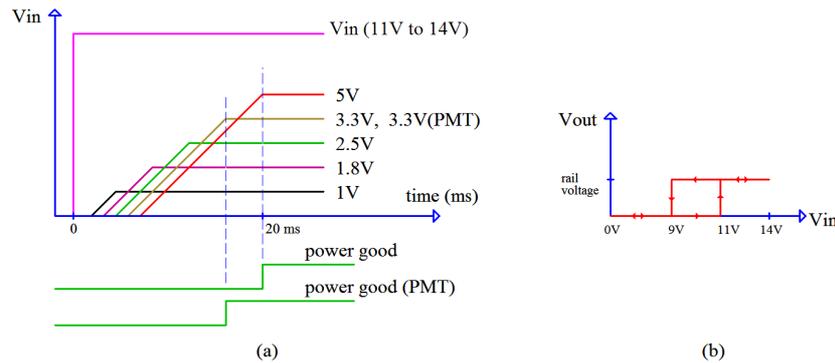

Figure 5: Power sequencing and start-up hysteresis specifications.

4.1 Power Converter Board Specifications

The PB rail voltages were specified at 1V, 1.8V, 2.5V, 3.3V, 3.3V(PMT) and 5V with expected loads ranging from 1W to 2.3W. They are derived from the 12V bus using step-down switching regulators. Due to the low noise and ripple requirement in driving the electronics of the PMTs, the 3.3V(PMT) rail is derived from a linear regulator (TI TPS74401) driven by a switching regulator that converts the 12V bus to an intermediate 3.8V rail in order to minimize the dropout voltage and heating of the 3.3V linear regulator. In addition to the above six step-down rails, a low power step-up rail, digitally programmable via I2C from 5V up to 30V, with a maximum load of 5mA, is also required. An independent on/off control signal is also provided for this 30V rail.

A block diagram of the PB is shown in Fig. 4, along with the maximum driving capabilities and set voltages for each rail. The initial load estimates for the step-down rails were 2.3A, 0.9A, 0.9A, 0.7A, 0.3A(PMT) and 0.4A for each rail respectively. This amounts to a total output power of

11.5W and, assuming a conservative 80% average converter efficiency, 14.3W for the input power drawn from the 12V bus. The output power estimate was later revised as the design of various modules was progressing and is now about 8W.

The power sequencing requirements dictated by the FPGA core and I/O voltages are illustrated in Fig. 5a. Lower rail voltages must be powered-up before higher ones, except for the 30V rail which works independently and is not part of the power sequencing specification. The power-down sequence normally is the reverse of the power-up. However, to simplify the design, this was not implemented. Instead, the rails are left to decay freely to ground potential in whatever order was determined by the amounts of energy stored in the decoupling capacitors. As this energy is very small and decays smoothly (i.e. without any voltage overshoots) and rapidly within 3ms (Fig. 6b), the long term reliability of the FPGA and other ICs will not be affected. As it turned out, this scheme results in the rails powering down (Fig. 6b) in the same sequence as powering up (Fig. 6a). The rising voltages at power-up are strictly monotonic as required by the FPGA.

Two open collector "power-good" outputs are produced by the PB (Figs. 4, 5). One collective "power-good" is asserted when all rails (excluding the PMT) have reached within 10% of their set voltages. A separate "power-good" is used for the PMT, asserted only when the PMT voltage and all lower rails (i.e. 1V, 1.8V, 2.5V) have reached their power good state. To simplify the design and avoid using a sequencer IC, the power-good scheme is implemented using the enable and power-good outputs of the switching regulators in a daisy-chain (i.e. domino-like) configuration, where each regulator is enabled by the power good output of the previous (lower) rail. One advantage of this scheme is that as each regulator takes about 5ms to ramp-up (Fig. 6a) and assert its power-good output, the in-rush current on the 12V bus is drawn one-at-a-time in 5ms intervals, thus avoiding any input voltage droops as can be seen in Fig. 6a. To further reduce the chances of any voltage droops during power-up causing unstable behavior, a hysteresis loop is implemented on the input bus voltage as shown in Fig. 5b. The enable input of the first (1V) regulator in the sequence is activated only when the 12V bus has reached 11V and deactivated on the way down at 9V. At 11V the decoupling capacitors at the input of the regulators are fully charged, ensuring a smooth dynamic response when the enable is asserted by the previous stage.

In the pre-production version of the PB, the I2C interface (Fig. 4) is used to monitor in real time the voltage and current of all rails, including the 12V bus. This can be done either by the FPGA firmware, when the CLB is plugged into the PB, or by PC software, independent of the CLB. A second I2C connector allows the PB to be connected at the same time to a PC via a bespoke USB interface board, for dynamic power profiling and data recording purposes.

4.2 Implementation Issues and Performance

The pre-production version of the PB contains additional ICs such as analog-to-digital converters (ADCs), buffers, current sense resistors and current sense amplifiers. As a result, its efficiency is reduced by about 5.5%, based on datasheet data. Two 12-bit, 12-channel ADCs are used (MAX1239) to measure 18 channels. The conversion data is read out via I2C. An external precision voltage reference is used for high accuracy in ADC conversion. A standard 4-layer PCB is used without any blind or buried vias in order to keep production costs low. Two power connectors and one mixed power/signal connector are used to plug the PB onto the FPGA board (Fig.

3). Decoupling capacitors are used on all switcher inputs and outputs, along with ferrite beads for filtering. An input DC power filter (Murata BNX022-01) is also used at the 12V bus entry point.

A very critical design decision regarding each of the six step-down converters was whether to implement it using discrete devices, i.e. a PWM switching controller IC with external components (inductors, MOSFET current switches, capacitors), or using a modular point-of-load switching regulator where all components are integrated into a monolithic package. Each approach has its own advantages and disadvantages and often it is not possible to predict in advance which is the best choice for a particular design without implementing both in detail.

The discrete approach requires more effort and time to prototype, test and validate a design. It is not flexible regarding changes in the specifications. However, it has the advantage of potentially higher conversion efficiency by fine-tuning the design to the specific load characteristics and optimizing component selection such as MOSFET switches. As a result its thermal performance is better. Significant effort and expertise is needed to optimize PCB layout in the discrete approach and as a result reliability is reduced due to the likelihood of assembly errors, whereas POL modules are subject to higher levels of testing by the manufacturer and their PCB layout is carefully optimized in terms of area, track lengths and RF emissions. Regarding output noise and ripple both approaches are similar in performance. However, with the discrete approach, very careful optimization of the PCB layout tracks is required to minimize parasitic inductances which create very high frequency noise spikes.

The modular POL approach is simpler and faster to implement and results in more compact designs with smaller footprint and simpler PCB layout. They are optimized by the manufacturer regarding size, heat flow and EMI. In addition, their reliability is much higher than what can be expected from a discrete design in terms of initial assembly errors, overloading or response to other fault conditions, and component lifetime failures. Modular designs implement more sophisticated protection mechanisms and are subjected to far more extensive and rigorous tests by the manufacturer than most discrete designs by the typical end user.

An initial attempt for a PB design based on discrete controller ICs (LTC3603, LTC3601) proved unsatisfactory, with high levels of noise and ripple attributed to non-optimal PCB layout and component placement. Subsequently a modular POL approach was adopted. Initially two high-performance modular POLs were short-listed, LTM8031 (1A) and LTM8033 (3A). These are potted in an land-grid-array (LGA) frame, with very low EMI emissions conforming fully to the requirements of EN55022 Class B, and switching frequency from 200kHz to 2.4MHz. However their unit price was high, about EUR 13.00 and EUR 15.82 each in quantities of 100. After initial evaluation, these were rejected mainly on grounds of unit cost. Finally two POL modules from Murata were selected, the OKL-T/1-W12 (1A) and OKL-T/3-W12 (3A). These are open frame LGA modules with fixed switching frequencies of 800kHz and 600kHz respectively and unit prices of EUR 2.18 and EUR 4.35 each in quantities of 100.

The current PB design is based on the Murata devices mentioned above. The additional features offered by the LT devices did not justify the significant extra cost. However, the 1A Murata device has no integrated power-good output, therefore an external circuit was implemented using a dual comparator and a gate, which has an additional EUR 0.48 unit cost for each switcher. Regarding reliability, for the 3A POL Murata quotes 10,011,000 hours MTBF by the Telecordia method (4a), and 5,549,000 hours MTBF by the MIL-HDBK-217N2 method (4b).

Several PB units have been constructed and deployed. The efficiency of the pre-production version is measured to 81.5% and is estimated to increase up to 87% when the current sensing and measurement capability is removed (based on datasheet data). The ripple and noise figures are less than 20mV peak-to-peak, which is satisfactory for our purposes. Our efforts are now concentrated on developing and using the power profiling features to characterize accurately the power consumption of the various modules within DOM. This data can then be used to optimize certain rails, possibly using a discrete controller approach, and also for stress screening and burn-in purposes at the production phase.
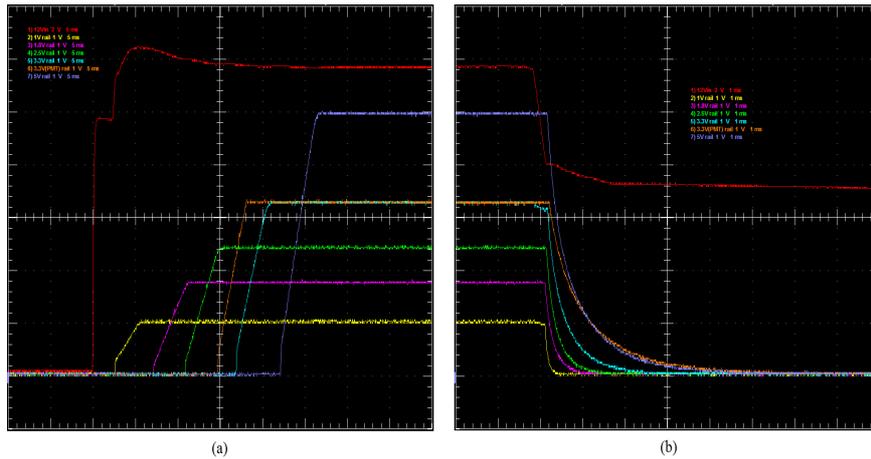
Figure 6: Oscilloscope capture of (a) power-up sequence (scale: 1V/div, 5ms/div), (b) power-down sequence (scale: 1V/div, 1ms/div), under full load.

5. Conclusions

In this paper we presented a flexible multi-rail converter design based on widely available, off-the shelf integrated power modules (modular POL converters), to simplify the design effort and speed up the production of working prototypes. These prototypes are enhanced with measurement and data acquisition instrumentation for the purposes of dynamic load characterization of each power rail. Following system integration, measurements are conducted and the results of load characterization can be used in further redesign of certain rails replacing the modular POL converters by discrete regulators with external magnetics and power transistors, if higher conversion efficiency is required. As it is not possible to predict in advance whether a system based on modular or discrete regulators satisfies better the list of design criteria, both designs must be implemented fully and compared before the final product is delivered to mass production. The results of load characterization can also be used for testing, stress screening or burn-in in the production phases of the project.

References

[1] KM3NeT Consortium, www.km3net.org

[2] P. Kooijman et al. "A new generation optical module for deep-sea neutrino telescopes," in *Nucl. Instr. and Meth A* **626-627**, 139–141 (2011).