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Development and test of a versatile DAQ system based on the ATCA standard

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A DAQ system based on classic electronics (Scalable Readout System-SRS) has been developed inside the Micro Pattern Gaseous Detector (MPGD) community in the recent years and is now being improved for large scale applications using the Advanced Telecommunications Computing Architecture (ATCA) platform. We present the development and test of a readout system which consists of an ATCA crate with high-speed backplane, front-end cards based on custom ATCA blades and custom readout units. The flexibility and modularity of the system makes it a powerful tool to be used in simple setups like cosmic stands or test beams, as well as allowing for the integration into a more complex DAQ framework. It will be used for Micromegas detector certification but also for the readout of a Micromegas prototype in the ATLAS experiment. The certification includes small or medium-size labs and test beam setup as well a 32-64 k channels test facility for the certification of the Micromegas detector for the ATLAS Muon system upgrade. The integration of such a system into the complex ATLAS Online TDAQ will allow to readout a Micromegas prototype (4096 channels) during the upcoming LHC run period.

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1. Introduction

The Scalable Readout System (SRS) is a collective effort within the RD51 [1] collaboration started in 2009 initially for the R&D of the MPGD technologies and the associated readout electronics. It is a general purpose multichannel readout solution for a wide range of detector types and complexities in different experimental environments [2].

The latest years in a process of technology transfer to industry, the classical Eurocrate-based SRS system started to be translated into an industrial ATCA [3] format in order to achieve higher integration density, higher data bandwidth and robustness for full-scale experiment size, having the same scalability capability as the classic SRS.

In the following section a brief overview of the classic SRS and its individual components will be presented. In section 3 the new ATCA-SRS system and the status of the implementation of its components will be given, while last section will go through the current and planned activities in the Muon ATLAS MicroMegas Activity (MAMMA) community at CERN.

2. The classic SRS

Figure 1 shows a schematic view of the SRS DAQ system. With the SRS system different front-end hybrids, with either analog or digital readout, can be connected over a customizable interface to the DAQ system [4]. This interface is implemented via a generic adapter card which is connected with edge-mounted PCIe connectors to the core component of the SRS DAQ system, the Front End Concentrator (FEC) [5] card. The FEC card is the common interface for all applications and contains the high complexity components of the system such as a reconfigurable FPGA with event buffer, I/O for the trigger and clocks and I/O for the adapter card. The adapter card includes all the necessary resources to readout the front-end hybrids on detector, e.g. ADCs in the case

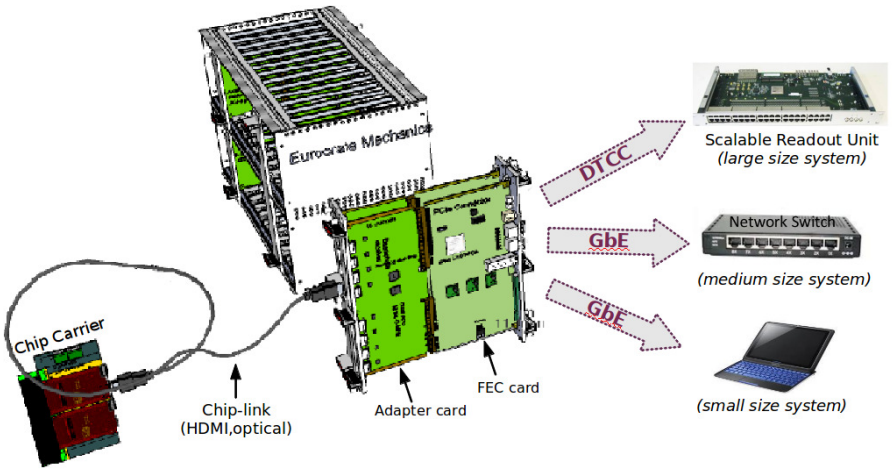


Figure 1: The SRS DAQ system consisting of the FEC card (core DAQ component of the system) and the adapter card.

when analog front-end hybrids are connected. Up to 8 FEC cards together with the adapter cards can be hosted in a standard 6U Eurocrate, reaching up to more than 16,000 detector channels.

Upstream from the adapter cards the components are common for all the DAQ systems. For small and medium size system the FEC cards can be connected via Gigabit Ethernet to a pc or a network switch, while for large size system DTCC (Data, Trigger, Clock and Control) links can be connected to a Scalable Readout Unit (SRU).

The DTCC link [6] has low fixed latency for the transmition of trigger primitives and TTC (Time, Trigger and Control) information using bidirectional channels, hence all the FEC cards can achieve a perfect synchronization without any data interference.

The SRU [7] is a readout concentrator which aggregates both event and trigger data from up to 40 FECs with 1 Gbps DTCC links. It hosts an FPGA that can perform event building, therefore the SRU can also act as a Read Out Driver (ROD) to maintain data acquisition compatibility. Event data is buffered, formatted, optionally compressed and re-transmitted via SFP+ ports. The latest version of the SRU hosts a Xilinx Virtex-6 FPGA, 3 SFP+ ports with up to 5 Gbps each and a 10 GbE output. For LHC applications, the SRU has a TTCrx ASIC receiver in order to pick up LHC clock and triggers via the TTC network of the LHC experiments.

Overall, the scalable architecture is based on high-speed point-to-point links with no buses thus providing more bandwidth and flexibility for longer distances between all the DAQ components.

3. The ATCA SRS

The ATCA technology was adopted in 2013 by many experiments as a modern standard originated from the telecommunication industry based on high bandwidth point-to-point connections between the boards (no use of data bus) and is about to replace some of the VME off-detector equipment in the LHC experiments.

Figure 2: The 14 slots ATCA crate with one ATCA board

One of the latest activities of the RD51 collaboration is the development of the classic SRS system in the ATCA format. The ATCA-SRS system provides high integration of the electronics components and higher channel density by reducing the cost per front-end channel. With this system more than 65,000 detector channels can be integrated per readout crate, about 4 times more than the classic SRS implementation. The fabric channels of the ATCA backplane can reach more than 10Gbps providing high data bandwidth.

3.1 ATCA SRS board overview

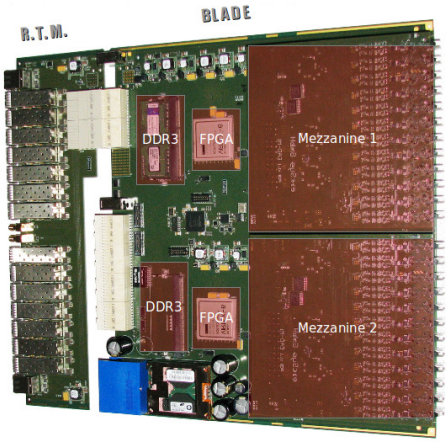


Figure 3: The ATCA-SRS board with the Rear Transition Module (RTM) and the Blade Main Board

The ATCA-SRS board (Figure 3) consists of two modules, the Blade main board with functionality equivalent of two FEC cards and the Rear Transition Module (RTM).

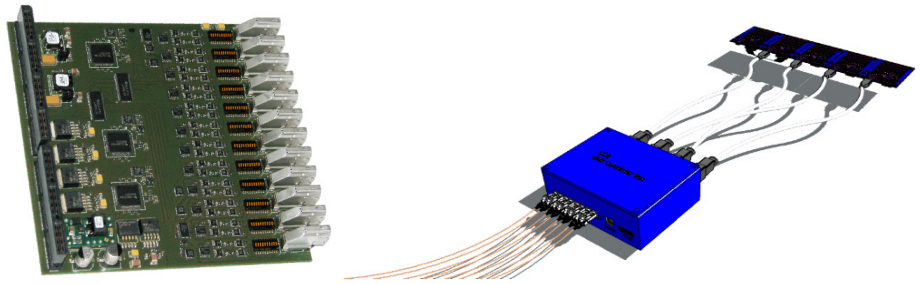
The blade main board hosts 2 x Xilinx Virtex-6 FPGAs, 2 x DDR 3 memories up to 4GB each and 2 x Mezzanine ports (with Samtec QTE/QSE connector) that work independently. The mezzanine cards are replacing the adapter cards of the classic SRS system. The 2 FPGAs can be

also interconnected in order to increase the logic resources between them. In this case only one DTCC output can be used sharing its speed between the two mezzanines.

The RTM is an I/O extension card with 2 x 7 SFP+ ports up to 5 Gbps at the moment, 2 x DTCC input ports with Rj45 connector and 2 x NIM input ports.

The ATCA-FEC is 3 times more logic resources, 5 times more memory and 2 times more performance (speed) in comparison with the FEC-SRS.

3.2 Readout of different front-end hybrids using the ATCA-SRS



(a) (b)

Figure 4: (a) The ADC HDMI mezzanine card for the ATCA-SRS board, (b) The optical converter (OC) box

Figure 4(a) depicts the ADC HDMI mezzanine card (with a size of 145 x 146 mm^2), that integrates the capability of the classic SRS-ADC adapter card. This mezzanine card hosts 12 x HDMI ports for a total of 24 x ADC channels and can be used to readout analog front-end hybrids, e.g. the APV25 [1][8] hybrid. Clock and trigger information to the front-end hybrids are distributed through the HDMI cables.

In order to readout front-end hybrids with digital output, as a function of the readout cable that it is used, e.g. the VMM2 [2] [9], three solutions are proposed:

- The HDMI output can be connected to a Digital-HDMI mezzanine card that is under designed at Horia Hulubei National Institute of Physics and Nuclear Engineering (IFIN-HH), Romania. In this case the hybrids are attached directly to the ATCA-SRS crate for laboratory or beam test conditions where the back-end electronics are not subject of intense magnetic field or radiation environment.

[1]The APV25 chip was developed initially as a front-end amplifier for the CMS silicon strip tracker and it is extensively used by the MAMMA collaboration for testing several Micromegas prototypes. It is a 128 channel charge sensitive amplifier chip with an analog pipeline buffer that has a depth of 192 cells for each input channel. The APV25 front-end hybrid has a discharge protection for gaseous detectors and it can be powered via HDMI cable.

[2]The Micromegas detectors that will be used in the ATLAS upgrade system for the LHC Phase-I upgrade will be readout by new series of front-end chips with digital output, the VMM. A second version of this series, the VMM2, will be used to readout the Micromegas prototype that will be installed during the 2014 summer in one of the two ATLAS Muon Small Wheels. The VMM2 chip has 64 channels and provides charge and timing information together with the address of the first event in real time for trigger information and time-over-threshold measurements with zero suppression for all the strips per event. A preliminary version of the VMM2 hybrid will have HDMI digital output while the final version will have optical output, each with discharge protection.

- The HDMI output can pass through an optical converter (OC) box (Figure 4(b)) and the optical output can be connected to the SFP+ ports in the RTM card of the ATCA-SRS board. This solution increases the reach of the output links, while the OC box is designed to stand strong magnetic fields and moderate radiation environments. The OC box is under design at CERN and Universitat Politècnica de València (UPV), Spain.
- The optical output of the OC box can be connected to an optical (SFP+) mezzanine card which is under design at IFIN-HH. This solution is a variant of the second one where the fibers coming from the front-end are plugged into an optical mezzanine, liberating the RTM for the use of 10Gb Ethernet or other links for DAQ.

4. Example of the possible SRS DAQ system

In MAMMA community the classic SRS and now the ATCA-SRS system is used as a data acquisition system for Micromegas detector certification at small or medium-sized setup in the RD51 lab at CERN and test beam setup. For this purpose, a dedicated DAQ software, called MMDAQ, has been developed inside the community in order to readout Micromegas chambers with the SRS system.

A DAQ system based on the ATCA technology will also be used to readout the Micromegas prototype [10] that will be installed this summer (2014) in one of the two ATLAS Muon Small Wheels. This prototype represents one multilayer of the detector which will be used for the ATLAS Muon Upgrade in the LHC Phase-I, the New Small Wheels.

4.1 MMDAQ: A Micromegas software for the ATCA-SRS system

The MMDAQ is a very flexible software since during its design no assumptions were taken on the electronics type or readout configuration. In this sense, any combination of different data sources can be used from different front-end hybrids using the FEC-SRS or the ATCA-FEC through a switch or an SRU.

It is a C++ multi-threaded program with dynamic dispatch that can perform event building according to the trigger number or the SRS time stamp. It is based on the server-client model using inter-process communication with sockets. The server initializes itself, opens all the necessary threads in the start up and waits for the client request in order to configure (start or stop) the run, to perform event building and to move the data to a storage. During data buffering a lock mechanism is enabled until all data is transmitted. The client can be a detached Graphical User Interface (GUI) or a terminal that transmits all the commands to the server.

Figure 5 shows the MMDAQ GUI through which the DAQ system can be fully configured. There are two run options: one for physics and one to measure the pedestals. Online monitoring is available to check main detector and electronics properties at channel level during the run, using the ROOT framework. An offline monitoring based on the online GUI infrastructure has been developed and it allows for fast offline check.

4.2 Integration of a Micromegas quadruplet into the ATLAS DAQ system

A Micromegas quadruplet prototype with an active area of 0.5 m^2 per plane has been built at CERN and will be installed on the present ATLAS Muon Small Wheel during the 2014 summer.

The quadruplet has 4096 channels in total and will be readout by the preliminary version of the VMM2 hybrids with the HDMI output. An OC box that is tolerant to radiation and intense magnetic fields will be used and the optical output will be connected to the SFP+ ports in the RTM card of the ATCA-SRS board or to an optical mezzanine.

This prototype will be readout using the ATLAS TDAQ chain, joining the ATLAS detector at Run II [3]. A standard SRU will act as a ROD in order to transmit the data after generating valid event fragments to the high-level Read Out System (ROS) [11] using the standard S-Link [12]. The SRU will be synchronized with the LHC bunch crossing clock (40.08 MHz) and will receive the Level-1 trigger signals from the Central Trigger Processor (CTP) through the TTCrx receiver ASIC. The Run Control System will be used for configuration and system control. A dedicated Micromegas segment has been implemented using the ATLAS TDAQ Software in order to be attached to the main ATLAS DAQ partition.

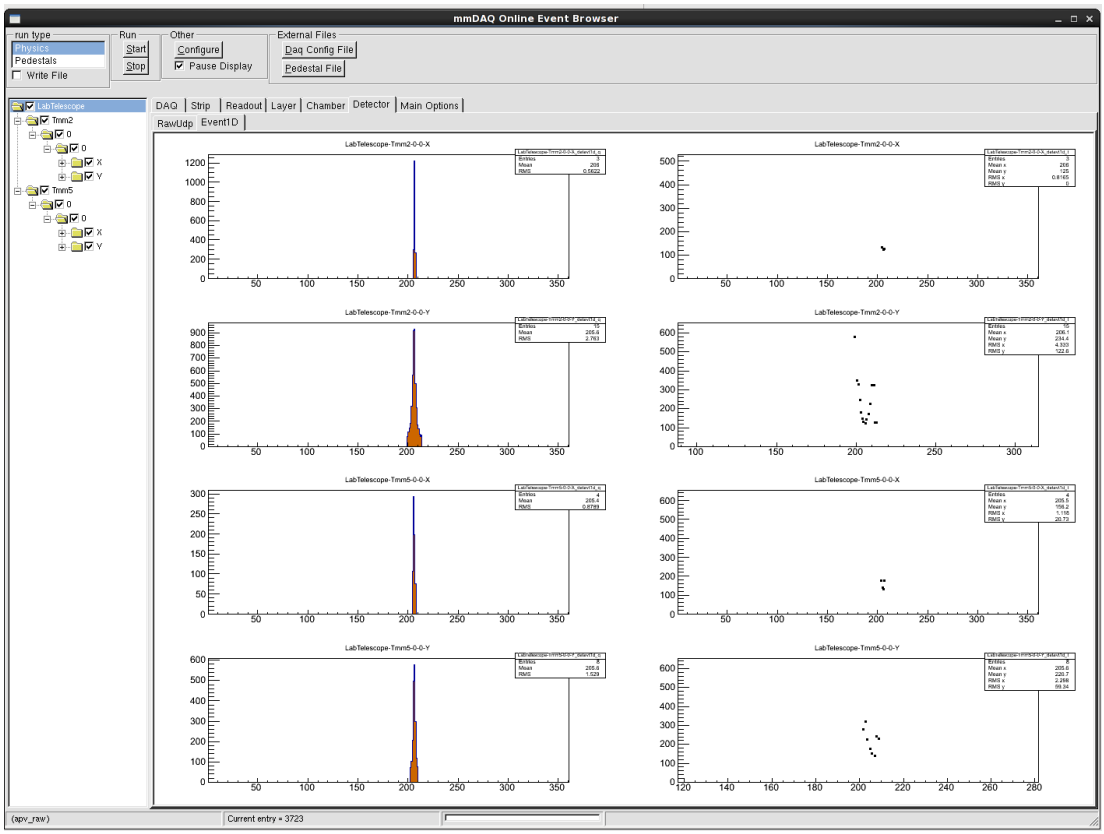


Figure 5: The MMDAQ Online Event Browser. The left side of the display histograms shows the maximum integrated charge and the strip position, while the right side displays the time corresponding to the bin with the maximum charge for every Micromegas strip detected cosmic muons.

Acknowledgments

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[3] Run II is the period 2015-2017 after the scheduled Long Shutdown 1 (LS1) at CERN

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References

[1] S.D.Pinto, *Micropattern gas detector technologies and applications, the work of the RD51 collaboration*, *IEEE Nuclear Science Symposium 2010 Conference Record* 5873870 (2010) [physics.ins-det/1011.5529]

[2] S.Martoiu et al., *Development of the scalable readout system for micro-pattern gas detectors and other applications*, *JINST* **8** C03015 (2013)

[3] *The official AdvancedTCA website:* http://www.picmg.org/v2internal/resourcepage2.cfm?id=2

[4] S.Martoiu et al., *Front-end electronics for the Scalable Readout System of RD51*, *Nuclear Science Symposium and Medical Imaging Conference (NSS/MIC), IEEE* (2011), doi:10.1109/NSSMIC.2011.6154414

[5] J.Toledo et al., *The Front-End Concentrator card for the RD51 Scalable Readout System*, *JINST* **6** C11028 (2011)

[6] A.Tarazona et al., *A point-to-point link for data, trigger, clock and control over copper or fibre* , *JINST* **9** T06004 (2014)

[7] A.Zibell, *Development of a read out driver for ATLAS micromegas based on the Scalable Readout System*, *JINST* **9** C01038 (2014)

[8] M.Raymond et al., *The APV25 0.25 μm CMOS readout chip for the CMS tracker*, *IEEE Nucl. Sci. Symp. Conf. Rec* **2** (2000), 9/113

[9] G. De Gironimo, *Trends in front-end ASICs for particle physics*, in proceedings of *TIPP 2014 Third International Conference on Technology and Instrumentation In Particle Physics*, Amsterdam, Netherlands 2-6 June 2014

[10] P. Iengo, *Construction of a large-size four plane micromegas detector*, in proceedings of *TIPP 2014 Third International Conference on Technology and Instrumentation In Particle Physics*, Amsterdam, Netherlands 2-6 June 2014

[11] G.Crone et al., *The ATLAS ReadOut System : performance with first data and perspective for the future*, *Nucl.Instrum.Meth. A623* (2010) pp. 534-536

[12] H. C. van der Bij et al., *S-LINK, a data link interface specification for the LHC era*, *IEEE Trans. Nucl. Sci.* (1997) vol. 44, no. 3, pp. 398-402