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Triroc: 64-channel SiPM read-out ASIC for PET/PET-ToF application

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Triroc is the latest addition to SiPM readout ASICs family developed at Weeroc, a start-up company from the Omega microelectronics group of IN2P3/CNRS. This chip developed under the framework TRIMAGE European project which is aimed for building a cost effective tri-modal PET/MR/EEG brain scan. To ensure the flexibility and compatibility with any SiPM in the market, the ASIC is designed to be capable of accepting negative and positive polarity input signals.

This 64-channel ASIC, is suitable for SiPM readout which requires high accuracy timing and charge measurements. Targeted applications would be PET prototyping with time-of-flight capability. Main features of Triroc includes high dynamic range ADC up to 2500 photoelectrons and TDC fine time binning of 40 ps. Triroc requires very minimal external components which means it is a good contender for compact multichannel PET prototyping. Triroc is designed by using AMS 0.35µm SiGe technology and submitted in March 2014. The detail design of this chip will be presented.

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1. Introduction

Triroc is a 64-channel silicon photomultiplier (SiPM) readout ASIC targeted for Time-of-Flight Positron Emission Tomograpy (TOF-PET) application. This chip is developed for TRIMAGE [1] European project, which is aimed for building a cost effective tri-modal PET/MR/EEG brain scanner. The sketch of the brain scanner is shown in the following figures.

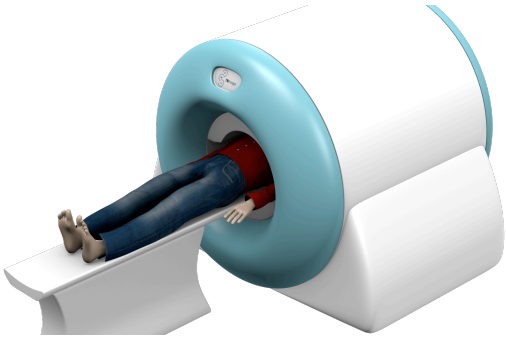


Figure 1 : Illustration of TRIMAGE brain scanner.

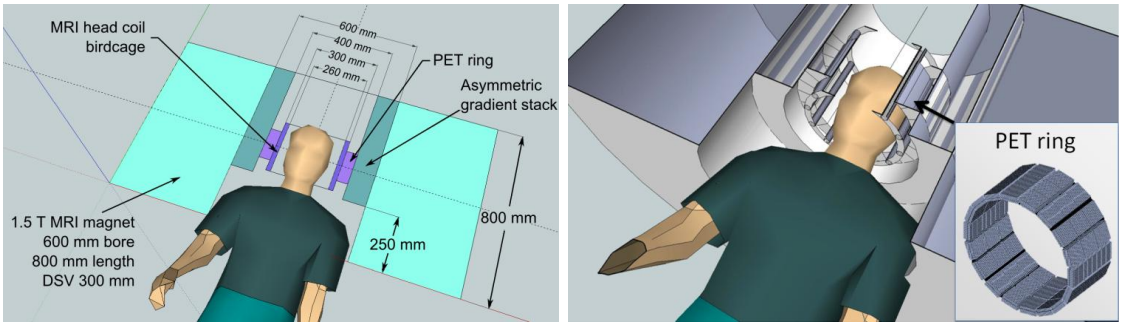


Figure 2 : TRIMAGE brain scanner cut off view and PET ring location.

The PET ring (Figure 2) of TRIMAGE brain scanner is assembled from 54 smaller units called gamma camera module. An illustration of the gamma camera module within the PET ring is shown in Figure 3.

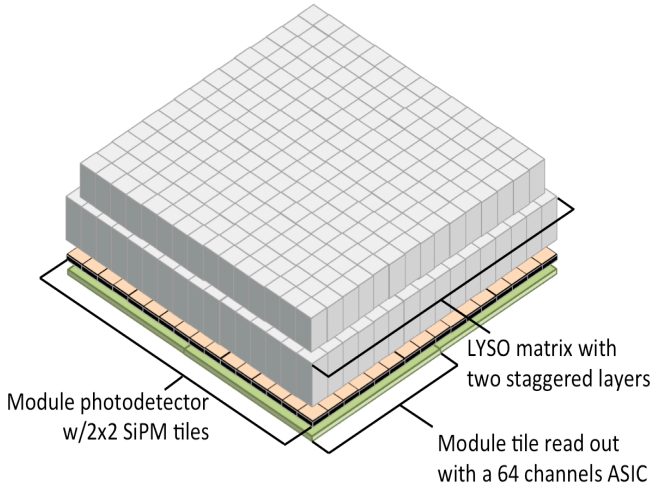


Figure 3 : PET ring gamma camera .

A gamma camera module consists of a front end board with SiPM arrays along with LYSO crystals on one side and readout ASICs on the other sides. The total channel number to be read out is 4x64 = 256 channels.

TRIMAGE is a consortium of 11 public institutions and private companies in Europe. Weeroc is involved in the Work Package 3 of this project that involves the design and optimization of the PET system. Specifically, Weeroc will design the readout ASIC of the SiPM arrays and also deliver the front end boards which house the readout chips.

Currently at Weeroc and Omega, three ASICs are available for reading out SIPM : Citiroc, Petiroc and Petiroc2. These ASICs are limited to 32 channels, can accept only one type of polarity input and contain limited signal processing capability. Therefore Triroc has been designed in order to cater higher input channel (up to 64 channels) and to accept both positive and negative polarity inputs. Additionally this chip includes more functionality in the digital part such as ADC, TDC and noise rejection function, which are specifically targeted for compact TOF-PET system prototyping. As of 2014, there are very few ASICs available from other laboratory or company that integrates high channel number and charge and/or time conversion for the input signal. However it is worth mentioning ASICs such as PET4[2] and TOFPET[3] which was designed for TOF-PET application. TOFPET ASIC is quite similar to Triroc in term of features and input channel. The differences between the two ASICs reside on the pre-amplifier bandwidth and charge measurements conversion. Triroc incorporates gigahertz pre-amplifier coupled with fast discriminator for swift first photon triggering and more precise Wilkinson ADC for the charge measurement. Comparing to 36–channel PETA4 ASIC, Triroc has the advantage on the input channel number. However PETA4 ASIC has the upper hand on the signal processing speed by taking advantages of the smaller transistor technology node (180nm) compared to 350nm used for Triroc.

2. ASIC Architecture

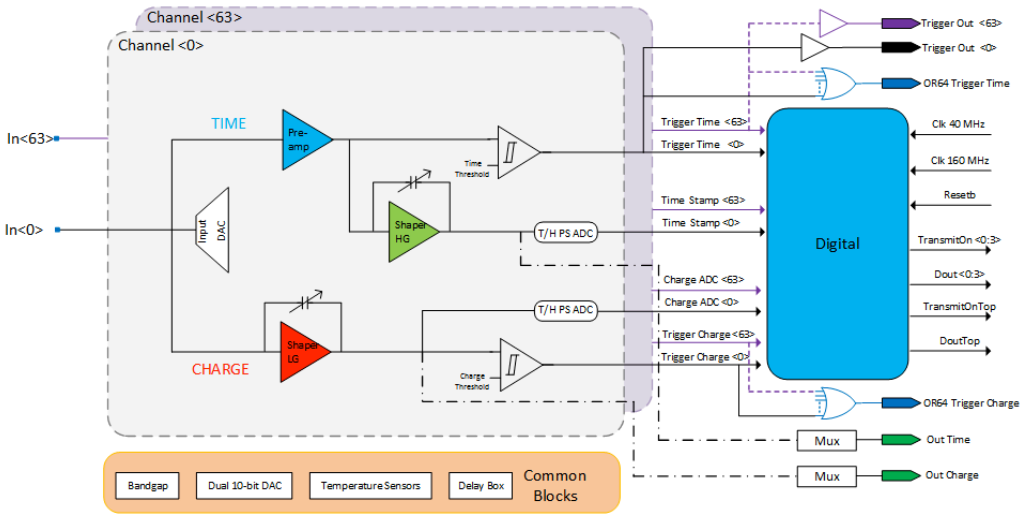


Figure 4 : Triroc ASIC block diagram.

From the block diagram in Figure 4, one could identify different function in this chip. The analog section of the chip is divided in to 2 main blocks : the first one for time measurement and the second one for charge measurements. Afterwards the outputs the analog blocks are sent to digital part that will initiate the analog to digital conversion, events time stamping and also the data readout. The design of both analog and digital parts will be detailed in next sections.

3. Analog Design

The architecture of the analog part is shown in Figure 5.

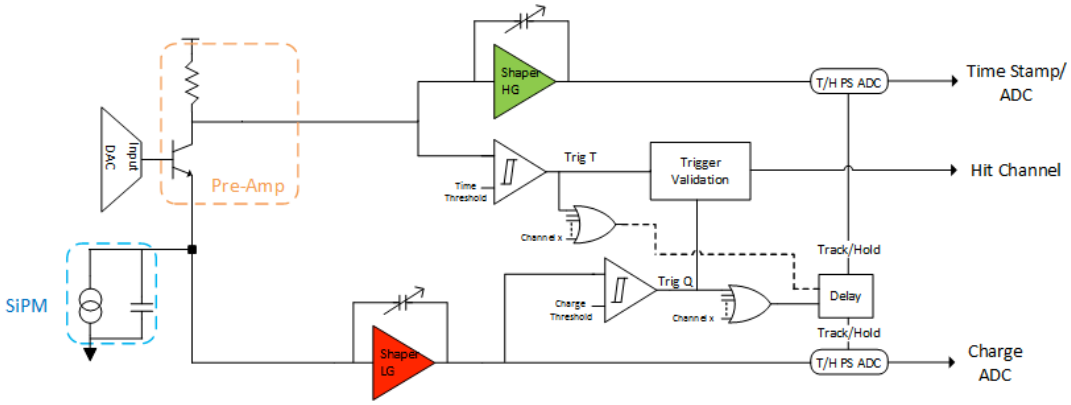


Figure 5 : Triroc ASIC analog architecture.

The low-noise, DC-coupled front-end amplifier of this ASIC accepts both negative and positive input signals thus making it suitable for reading out any SiPM in the market. Moreover, individual input DC level adjustment is available for correcting the non-uniformity of SiPM gain.

In each ASIC channel, the incoming signals will be sent into two different paths: for energy and time measurements. A variable gain semi-gaussien shaper is used for shaping the input signal in energy measurements. The energy conversion is handled by a 10-bit Wilkinson ADC. This ADC is a proven design and it is expected to be linear up to 2500 photoelectrons (p.e). Additionally, Charge Trigger is available and can be used for events validation at required energy such as 511 keV.

Signal from high-speed input pre-amplifier is fed into a discriminator in order to provide a fast trigger (Time Trigger) for time measurements. A TDC module with coarse and 40 ps fine time is used to time-stamp this trigger.

4. Digital design

The digitized data are collected by the digital part, which is also capable to validate 511 keV events and reject noise. Running at 80 Mhz, data will be transmitted through 5-bit parallel links. 4-bit link is dedicated for channel specific data such as coarse time, fine time and charge measurements. Finally the last bit of the parallel links is allocated for global coarse time of the ASIC. Other features available are for examples zero suppress readout and TDC data compression. In all, the ASIC should be able to process up to 50k events per second.

5. Simulations

Simulations results are presented in this section. Preliminary measurement results of the analog part are reported in next section.

5.1 Input DAC

In each analog channel, an input DAC is available so that users could adjust the overvoltage of SiPM. Eventually the SiPM gain non-uniformity can be corrected by applying appropriate input DAC value for each channel. The architecture of the DAC is based on current steering topology. The simulation of this DAC is shown in Figure 6.

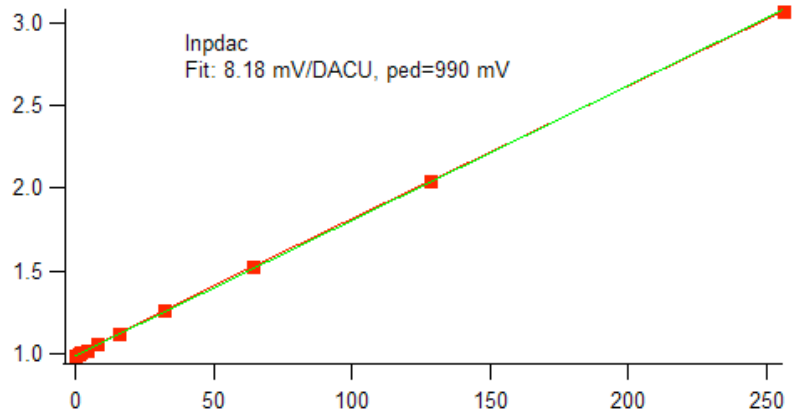


Figure 6 : Input DAC linearity simulation.

The characteristics of the input DAC are shown in the following table :

Bit	8
Range	1-3 V
LSB	8.18 mV

Table 1 ; Input DAC characteristics

5.2 Trigger Threshold DAC

For setting the threshold of the two triggers, Time and Charge Triggers, a 10 bits DAC with dual outputs is implemented internally. Just like the input stage DAC, trigger threshold DAC is also based on current steering architecture. The outputs of this DAC are common for 64 channels. The simulations of the DAC outputs are shown in Figure 7.

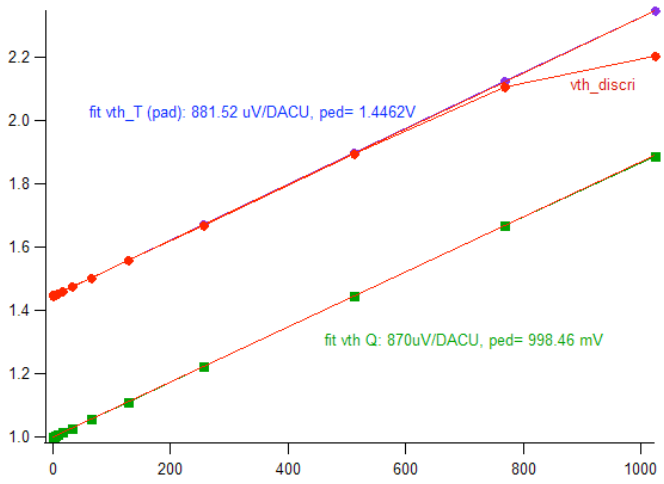


Figure 7 : Top plot: Time Trigger DAC, Bottom plot : Charge Trigger DAC.

The summary of the 10 bits DAC dual outputs are shown in the following table:

	Time Trigger	Charge Trigger
Bit	10	10
Range	1.446 - 2.348 V	0.998 – 1.889 V
LSB	0.89 mV	0.87 mV

Table 2 : Time Trigger and Charge Trigger DAC characteristics.

Since the Time Trigger is required to be precise and uniform all over the 64 channels, a threshold trimming system is also available individually in each channel. Users will be able to correct the time threshold down to 40 mV below its input. For example in the simulations shown in Figure 8, the Time Trigger threshold is set at 1.67 V.

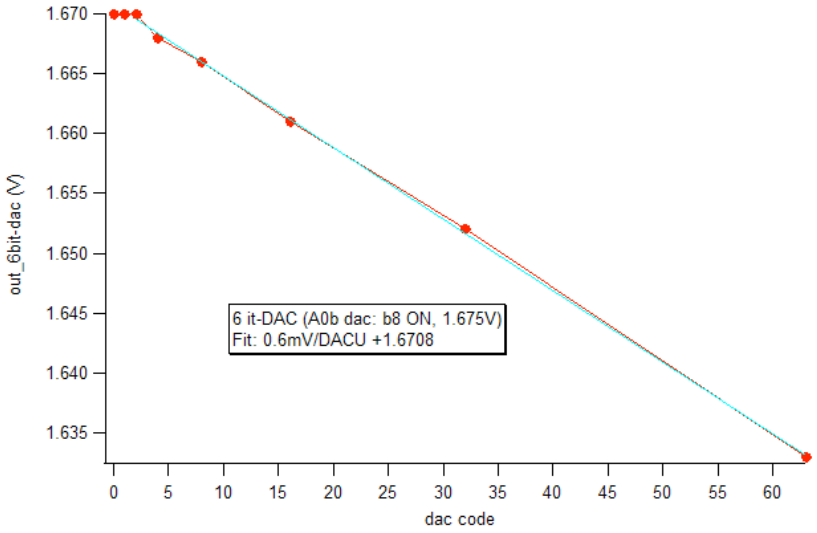


Figure 8 : Time Trigger Threshold trimming simulations.

The characteristics of the threshold trimming are listed in Table 3.

Bit	6
Range	Input – 40 mV
LSB	0.6 mV

Table 3 : Time Trigger threshold trimming performance

5.3 Pre-Amplifier

The pre-amplifier in this ASIC is based on common base amplifier design. It has designed in order to maximize the bandwidth for accepting fast inputs while maintaining low power consumption. Coupled with a fast discriminator, this pre-amplifier is used to generate the trigger for time stamp the events.

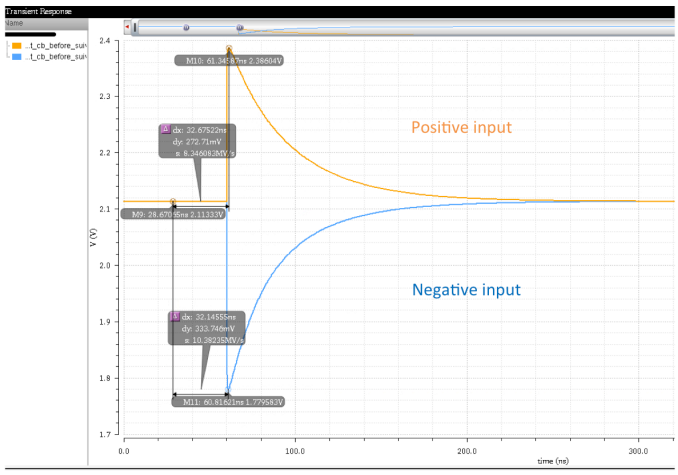


Figure 9 : Pre-amplifier simulations for 20 p.e inputs charges.

As shown in Figure 9, the pre-amplifier is capable to accept negative and positive polarity inputs. The linearity of the preamplifier is shown in the following figure.

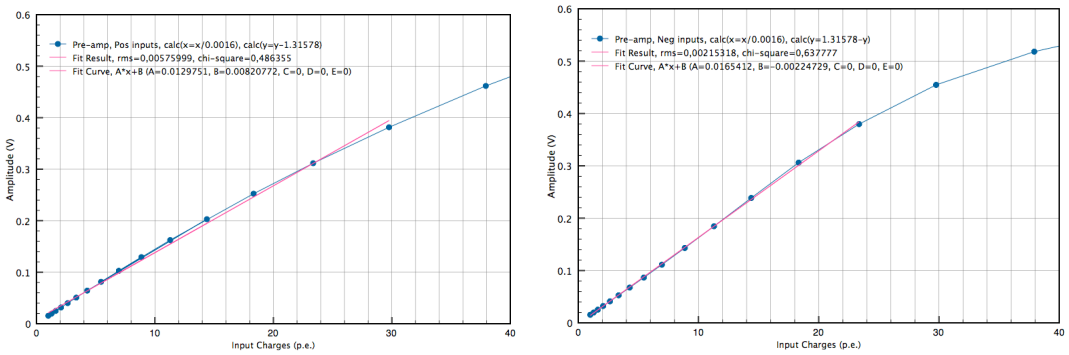


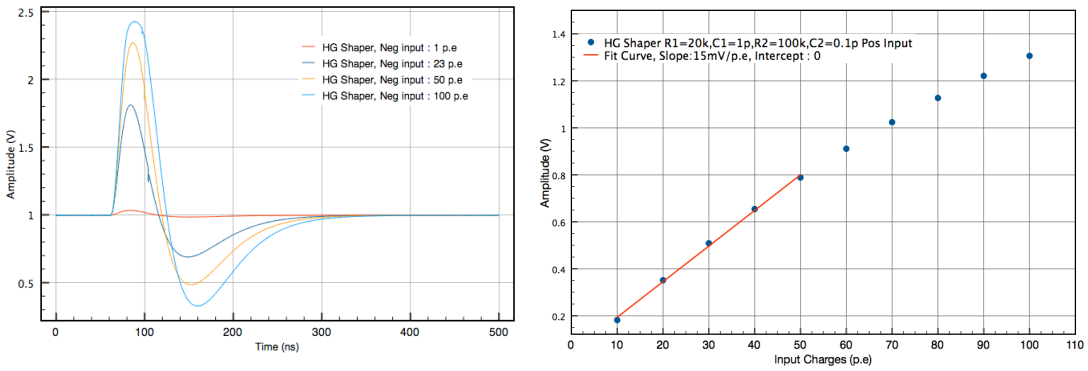
Figure 10 : Left : Linearity for positive inputs. Right : Linearity for negative inputs.

As shown in Figure 10, the pre-amplifier is linear up to 30 p.e for both input polarity. This dynamic range is more than enough for the pre-amplifier as for the timing path, Time Trigger just need to trigger on the first arrival photoelectron.

For the time stamp, the coarse time is handled by the digital part of this ASIC. On the other hand, the fine time is done via a time-to-amplitude converter (TAC) and Wilkinson ADC. Both TAC and ADC are proven designs that have been used in previous chips such as Petiroc2 [4].

5.4 High Gain Shaper

Although the pre-amplifier is primary used for time measurement, it has a secondary function for charge measurement at lower range. The energy measured with the pre-amplifier is typically lower than 100 p.e. For this purpose a high gain shaper is connected to the preamplifier for shaping the input signal. The shaper used here just a typical CR-RC2 architecture with variable shaping time and gain. By default the gain is set at 10 and the shaping time is set at 20 ns. Otherwise the shaping time can be adjusted from 10 ns to 160 ns. The simulations of the shaper are shown in Figure 11. As shown in Figure 11 (b), the linearity of this shaper is up to 100 p.e.



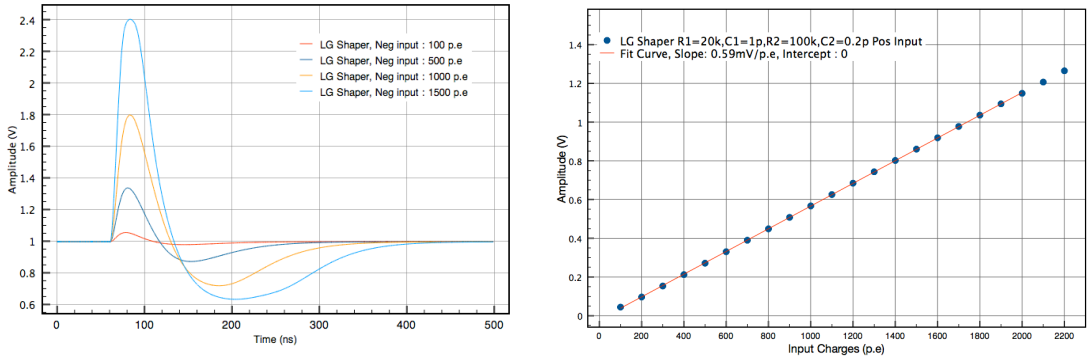
(a) (b)

Figure 11 : (a) High Gain Shaper simulations. Input : 1-100 p.e (b) High Gain Shaper linearity

In order to digitize the signal, either hold/sample module or peak detector system can be used. The Analog-to-Digital converter used here is based on Wilkinson architecture that has been used in other chips designed at Weeroc and Omega.

5.5 Low Gain Shaper

The Low Gain Shaper shares the same architecture as the High Gain Shaper. However the gain is lower and the input of the shaper is coming directly from the SiPM. Therefore the overall gain is lower and this shaper can accept higher input charge. By default the gain and shaping time are set at 5 and 20 ns. The simulations of this shaper are shown in Figure 12.



(a) (b)

Figure 12 : Low Gain Shaper simulations. Input : 100-2200 p.e

The linearity of this shaper is shown in Figure 12 (b) and it is linear up to 2000 p.e. Just like High Gain shaper, its output is connected to either a track/hold module or a peak detector system. The conversion is done with Wilkinson ADC similar to the previous shaper.

6. First measurement results

After several delays in test board development and ASIC BGA packaging, the tests have been started in October 2014. Analog measurements have been carried out for the pre-amplifier and the two shapers of the ASIC. The results for the pre-amplifier are shown in the Figure 13.

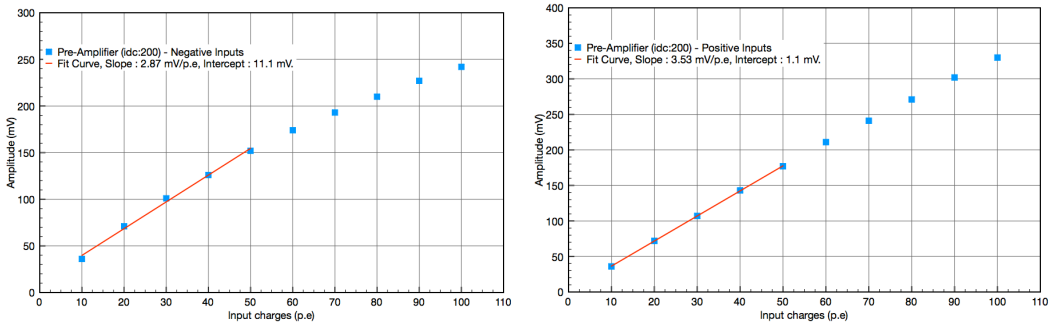


Figure 13 : Pre-amplifier gain and linearity for negative and positive inputs.

The pre-amplifier is linear at least up to 50 photoelectrons. The measured gain is expected to be lower (~50%) than simulation results since the pre-amplifier output is not buffered for analog measurements. The real gain and minimum input charge will be extracted using s-curves or trigger efficiency tests.

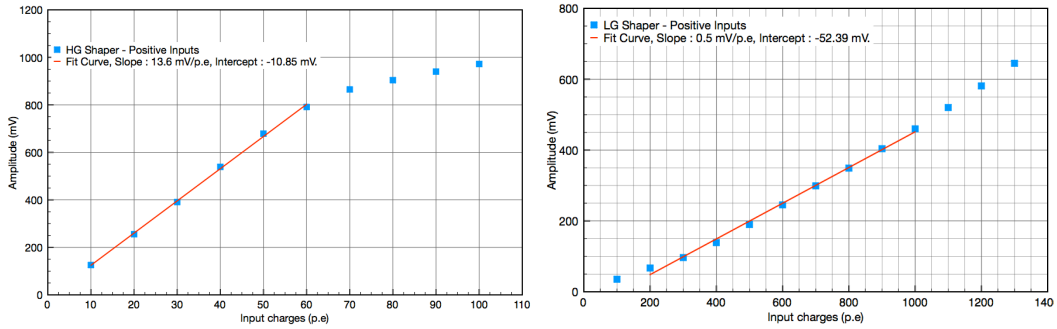


Figure 14 : High Gain Shaper (left) and Low Gain Shaper linearity (right).

The shaper outputs are measured by setting default slow control configuration for each block. The gain for High Gain Shaper is 13.6 mV/photoelectron compared to 15 mV/photoelectron of simulation results. For Low Gain shaper, the measured gain is 0.5 mV/photoelectron compared to 0.59 mV/photoelectron from simulations. The dynamic range of the shaper will be determined by using internal ADC since the analog measurement is limited by the signal monitoring buffer of the ASIC as shown in Figure 14. Other measurements such as for time and charge measurement are still on going. These are only early results of the ASIC characterisation and other performances results will be released later.

7. Conclusion

Triroc ASIC has been submitted successfully in March 2014. The technology chosen for this ASIC is AMS 0.35µm SiGe BiCMOS. Unfortunately ASIC characterisation phase has to be pushed back to September 2014 due to various delays in ASIC packaging and test board development. This ASIC will be packaged in 353 FBGA with dimensions of 12x12x1 mm. A small packaging is required since the front ASIC board shall include four readout ASICs in 5.5x5.5mm area. The work on the front end boards started in September 2014 in parallel with the ASIC characterisation phase.

8. Acknowledgment

This work is supported by European Union Seventh Programme under the grant agreement n° 601621.

References

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