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AGIPD, the electronics for a high speed X-ray imager at the Eu-XFEL

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The AGIPD (Adaptive Gain Integrated Pixel Detector) X-ray imaging camera will be operated at the X-ray Free Electron Laser, Eu-XFEL, under construction in Hamburg, Germany. Key parameters are 1 million 200 μm square pixels, single 12.4 keV photon detection and a dynamic range to 10 000/pixel/image. The developed sensors, ASICs, PCB-electronics and FPGA firmware acquire individual images per bunch at 27 000 bunches/s, packed into 10 bunch-trains/s with a bunch separation of 222 ns. Bunch-trains are handled by 352 analogue storage cells within each pixel of the ASIC and written during the 0.6msec train delivery. Therefore AGIPD can store 3520 images/s from the delivered 27 000 bunches/s. Random addressing provides reusability of each cell after an image has been declared as low-quality, so that good images can be selected. Digitization is performed between trains (99.4 msec).

In the paper all functional blocks are introduced. The details concentrate on the DAQ-chain PCB-electronics and the slow control. A dense area of 1024 ADC-channels, each with a pickup-noise filtering and sampling of up to 50 MS/s/ADC and a serial output of 700 Mbit/s/ADC.FPGAs operate the ASICs synchronized to the bunch structure and collect the bit streams from 64 ADCs/FPGA. Pre-sorted data is transmitted on 10 GbE links out of the camera head using the time between trains. The control and monitoring of the camera with 600 A current consumption is based on a micro-controller and I^2C bus with an addressing architecture allowing many devices and identical modules. The high currents require planned return paths at the system level. First experimental experience with the constructed components will be presented.

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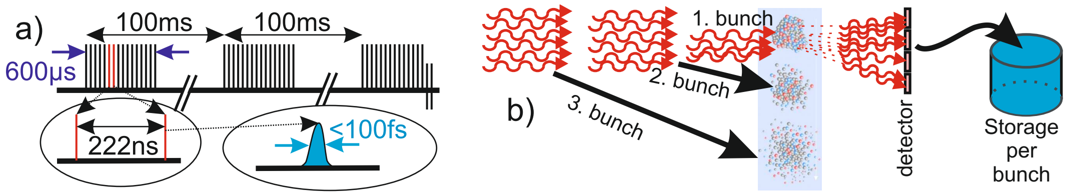

Figure 1: XFEL-experiments: (a) bunch structure of Eu-XFEL, (b) Principle of recording bunch-by-bunch

1. Free electron lasers (FEL): Chances, challenges and AGIPD's parameters

Free electron lasers generate intense very short X-ray bunches. The European free electron laser (EU-XFEL)[1][2] is under construction in Hamburg, Germany, until 2016 aiming for 27 000 bunches/s. With a 2.1 km long superconducting accelerator electrons will be accelerated to an energy of $E_e = 17.5$GeV and sent into undulator magnets with geometrical parameters to generate X-rays with a wavelength of ≈ 0.1 nm, the size of atoms. Since the wavelength for lasing in alternative magnetic fields scales with $1/E_e^2$ [3] the long accelerator is needed.

Lasing will generate very short, intense pulses of coherent X-rays with 10^{12} photons within 100 fs[2]. At XFELs it is feasible to study objects, which get even modified by a few X-ray photons. FELs provide enough photons within a single bunch to image the structure. But in the time afterwards fragments move and the photons get scattered on them. Therefore detectors are required which can record the signals from each bunch as separated data sets. Due to thermal losses, when applying accelerating RF-fields in the cavities, the Eu-XFEL delivers the high rate of bunches in trains (see figure 1). During 600 μs 2700 bunches are delivered with a time separation of 222 ns (4.5 MHz), so called trains. They repeat every 100 ms. This high bunch rate demands specially developed detectors.

The AGIPD (**a**daptive **g**ain **i**ntegrating **p**ixel **d**etector) consortium develops a 2 dimensional camera[4] to catch the small angle scattered photons. The images are recorded with 1 Megapixel, 1024×1024 pixels, each with a size of 200 μm×200 μm. The readout chain is optimized for 12.4 keV photons. The dynamic range will cover identification of zero and low number of photons and will provide for high signals up to 10 000/pixel a resolution better than the fluctuation described by Poisson statistics $\sqrt{number\ of\ photons}$. Out of the delivered 2700 bunches 352 images can be recorded. A possible overwriting of storage cells during the train will allow to keep the bunches identified as good by external detectors. Since most of the pixels will contain signals for each scattering and the information is contained in the details no generic algorithm can be applied to compress the signal and data stream further than the description of the dynamic range. Therefore the full signal bandwidth passes through the whole chain until entering high level computing equipment.

2. Concept of AGIPD for a two dimensional camera

The fast bunch-to-bunch timing, the large dynamic range and the mechanical optimization of the active camera head requires specialized developments of all components through the signal chain. In the following section the individual components will be described. The signal chain

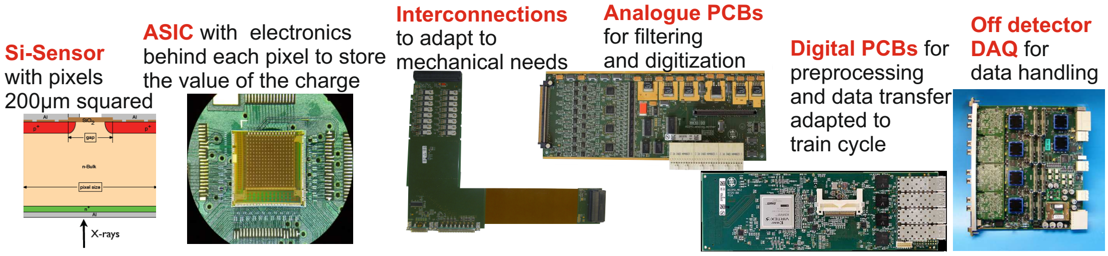

Figure 2: Electronic chain from sensor to off detector-head data handling

(see figure 2) starts with a silicon pixel sensor. During the train each pixel generates a signal rate of 4.5 MS/s and for 1 Mega-pixel a mean sample rate of 3.7GS/s is transfered through the chain. This requires a dedicated ASIC. The mechanical constraints can be fulfilled with interconnecting printed circuit boards (PCB) before the signals get digitized and preprocessed within the detector head. Final processing and storage is done outside the detector head.

The mechanical concept, figure 3, keeps the X-rays in vacuum until the surface of the detector. Minimizing the distance of the detector to the sample and leaving space for small angle downstream detectors defines the design of the vacuum chamber and the complex positioning of the PCBs as wings. The analogue and digital PCBs are located in air allowing an easier cooling and compacter design of these PCBs populated with many different heat producing components. The interconnection between the focal plane and the analogue PCBs allows an adjustment of the central hole by moving the focal plane as quadrants, which is a group of four modules. With a PCB the many signals are fed out of the vacuum.

3. Functional blocks of the electronics

With 500 μm thick n-type Si-sensors[5] 90% of the 12.4 keV X-rays are detected. A specific challenge is the high ionization density, 4×10^6 electron-hole-pairs, generated by 15 000 X-ray photons within a single pixel[6]. AGIPD has chosen a sensor design of 200 μm square pixels, which needs 500 V as bias to keep the charge cloud at the size of a pixel.

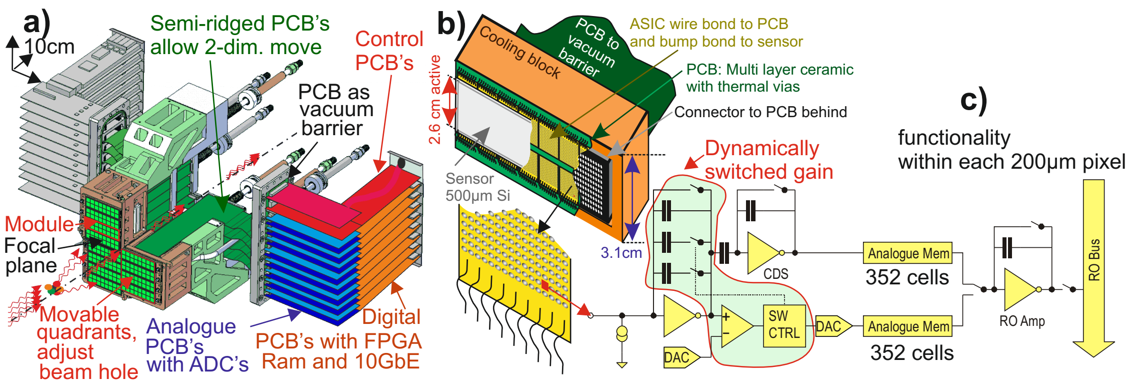

Figure 3: Mechanical concepts of AGIPD as (a) whole detector-head and (b) of the focal plane design; (c) the electronics functionality to fit in the pixel area of the ASIC

Each pixel is bump bonded to an ASIC [7]. The functionality per pixel is shown in figure 3. For each bunch the arriving charge is integrated into a dynamically increased feedback capacitor, providing three gain states. This function gives the detector its name AGIPD: Adaptive Gain Integrating Pixel Detector. The analogue output and the selected gain state are stored in capacitors. The used storage cell is set per bunch via a control interface allowing random access, which gets later relevant for keeping the best scatterings. Since all that functionality is required for each pixel, it is only possible to realise 352 storage cells, which is less than the 2700 bunches/train. After the train all the stored values are multiplexed to four differential output lines of the ASIC with 33MS/s. Each ASIC with 64×64 pixels is controlled by just three 3 LVDS lines. This minimized connectivity is necessary due to the available space for connectors through the whole signal chain.

The focal plane, figure 3, is constructed out of modules. Each module has 512×128 pixels on a single sensor. 16 ASICs are bump bonded to the sensor and wire-bonded to a multilayer ceramic PCB. Electrical vias and the ceramic itself transfer the heat and signals to the back side, on which the available space is shared between a 500-pin dense connector and a copper block to cool the sensor and the ASICs to -15 to -20^{0}C.

The interconnection from the backside of the focal plane to the analogue boards has to provide the feasibility to position the focal plane close to the sample preparation by sticking out of the flanges needed for the vacuum enclosure. Also the movement of the quadrants for adjusting the beam hole but fixed vacuum-flanges, one for two quadrants, has to be realized. Therefore the many differential signals, 560 per $^1/_2$ -Mega pixel, and a few control signals are routed from the focal plane to the vacuum flange with a pre-bended long semi-ridged PCB allowing a two-dimensional movement. For the vacuum feed-through a thick multilayer-PCB is designed. With SMD-connectors on both sides the connection density is provided without mechanical interference. Using micro- and plugged vias avoids any through going holes and maintains the vacuum tightness.

The analogue electronics, figure 4, provides on PCBs plugged into the vacuum barrier a dense electronics for 512 analogue channels per $^1/_2$-Mega pixel, each with a signal stream designed for 50 MS/s. With two PCB's per module each of the 64 analogue channel gets on one side of a PCB an 8 mm wide strip. On that a filter with a single amplifier, capacitors and coils is installed to reduce

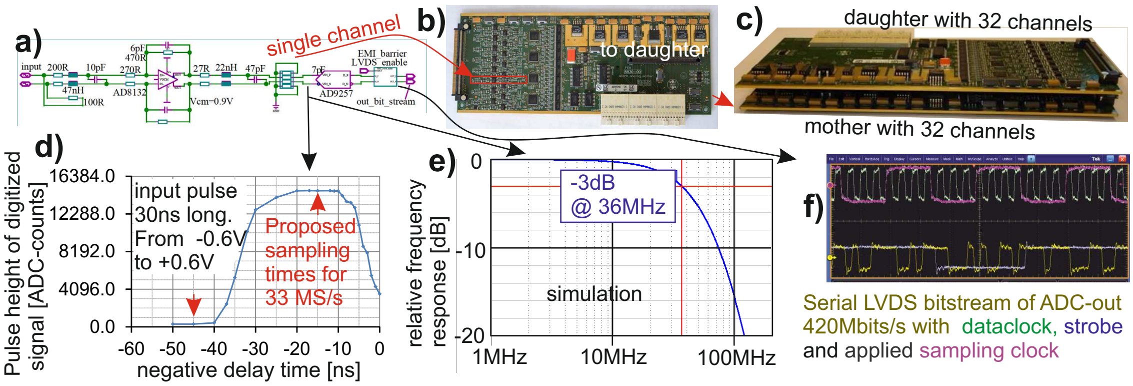

Figure 4: Analogue electronics: (a) basic circuit for each channel, (b) PCB for 32 channels, 16 channels each side, (c) combination of two boards for 64 channels of a module (d) pulse shape of filter measured with the own ADC, (e) simulated frequency response, and (f) digital bit output stream to the digital PCB.

the noise picked up along the interconnecting boards and to adapt voltage levels to the needs of the ADC. For the ADCs commercial 14 bit 8-channel chips with serial data outputs as frequently used for medical imaging are chosen. The 64 data streams up to 700 Mbit/s and its synchronizing signals (clock and strobe) are fed through resistors and a dedicated LVDS-buffer to keep the ADCs protected from noise from high power digital electronics.

The subsequent digital electronics[8] is mounted under 90^0 and receives on the 64 parallel lines per module a data stream of 45 Gbit/s. For all the data handling tasks a FPGA, XILINX VIRTEX5, is used. It will have to receive the data stream, reduce the ADC-value for the gain to a two bit combination with the information of the three gain states (00, 01, 10) and of ambiguous identification (11), and to combine it with the 14-bit value of the integrator output to a 16-bit word per image and pixel adequate for IT-instrumentation. This needs to write data per train first to memory and read it during the next train period again with a bandwidth of the output stream for a 10 Gigabit-Ethernet (GbE). The required memory access for parallel read and write is provided by DDR2 memory with 500 M-access/s and a width of 128 parallel data-bits. While the read and write procedures the data can be sorted to small geometrical patterns. Each of the 16 modules has its own 10 GbE output link via an optical fiber to the off-detector head electronics with UDP as protocol and a payload around 50 %. The realization is done with an active multi project mezzanine card providing four high speed links plugged onto a project specific carrier. Even with the mechanical constraints a good behavior of all 16 high speed 3.125 Gb/s- lines from FPGA to physical interfaces is reached. No bit transfer errors are observed within hours of checks on the fibers leaving the detector head.

4. System aspects

The detector head consumes ≈600 A of low voltage power. Within that environment signals have to be handled with 3000 electrons/12keV-photon, with signal transfers on the geometrical scale of PCBs for 14bit resolution and a frequency range kept open from DC to 36 MHz. Therefore a grounding and EMI-concept (electromagnetic interference), figure 5, is designed to minimize the common usage of ground as reference and current return. Also the goal is to minimize the coupling

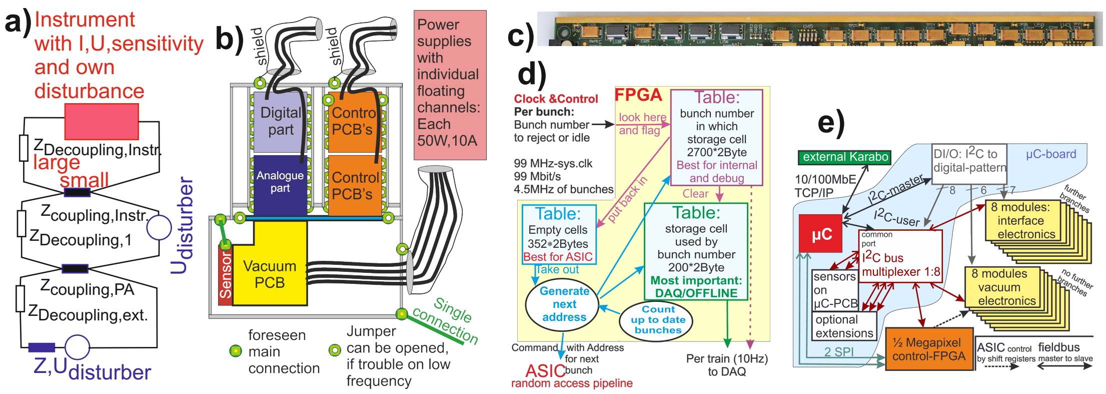

Figure 5: System aspects: (a) General idea of EMI-zoning (b) AGIPD's supply and ground for different functional blocks, (c) PCB edge for induced current-return, (d) rejecting bunches and (e) Slow control

impedances between different functional blocks by defining good entrance points for required and induced currents. It follows an EMI-zoning idea described in [9]. Therefore the whole signal chain from ASIC through the analogue part and the digital part is kept differential with decoupling at the different entrance points and planned current balancing. Each functional block gets from external supplies a floating power channel with ferrite-filters at the entrance points and currents guided back from the point of usage. The groups are adjusted to make usage of commercial low-ripple multi-channel power-systems with around 50 W or 10 A per channel. That still leaves everything floating and the common grounding point can be freely chosen at the most sensitive point, the focal plane. As default option many additional ground connections to the chassis will be installed providing for higher frequency currents induced into the surrounding chassis a return path to the source. That default option relies on the fact, that the low frequency components are kept under control by the floating supply system and generally not using ground as current return. But the option to open the grounding connections is provided and would allow the optimization for low frequency disturbances on the price of an increased sensitivity to higher frequencies. To avoid sensitivity to currents in the external metal and grounding system only a single connection area for all metal connections will be defined, reducing also the current induced by AGIPD into foreign systems.

The control signals distributed within the detector-head are either differential LVDS or low current with limited risetimes, I^2C with specifications >20 ns [10]. The required higher speed SPI-buses operated during data taking are transformed to LVDS and adequate rise times before they are transfered from PCB to PCB.

On system level the shortage of 352 storage cells within each pixel for 2700 bunches/train is handled. The ASICs allow a random access to the analogue storage cells. Within the control system of XFEL each bunch gets a consecutive number within the train. For each $^1/_2$-Mega pixel an FPGA receives telegrams from an external bunch qualification system [11]. With a telegram of 22 bits any earlier bunch can be declared as low quality. This decision is performed on fast sensing the quality of the bunch and the scattering. First ideas are now introduced at LCLS for image selection based on easily accessible signals before CPU-extensive offline processing of images[12]. With a book keeping in three tables the FPGA can provide fast access to the required information. From the cell-number sent as memory write-address to the ASIC and the external reject information a full history table (1) represents the storage cell number as function of the bunch number with its full history. From that table (1) the freed cell number can be transfered to the table (2) of free bunches and in the opposite direction the used cell-number is communicated. Transferring the same information to a table (3) representing the bunch number as function of the cell number a table optimized for offline correlation of the images to other accelerator information can be provided.

As third system aspect the control of the detector head is important. In such a high power and complex digital processing system voltages, currents and temperatures need to be monitored, power for functional blocks has to be switched in sequences and firmware has to be downloaded and configured. This system has to consider, that each module just appears with the same electronics but has to be addressed individually and that the number of connector pins is limited. To provide an easy interface for the external control a central micro-controller per $^1/_2$-Mega pixel will be installed. Via a branched I^2C network the micro-controller communicates with every other partner in the detector head. On the I^2C-master bus the final addressee is selected by setting a digital pattern. Afterwards the I^2C-user bus is used to communicate with the final device. That branching will even

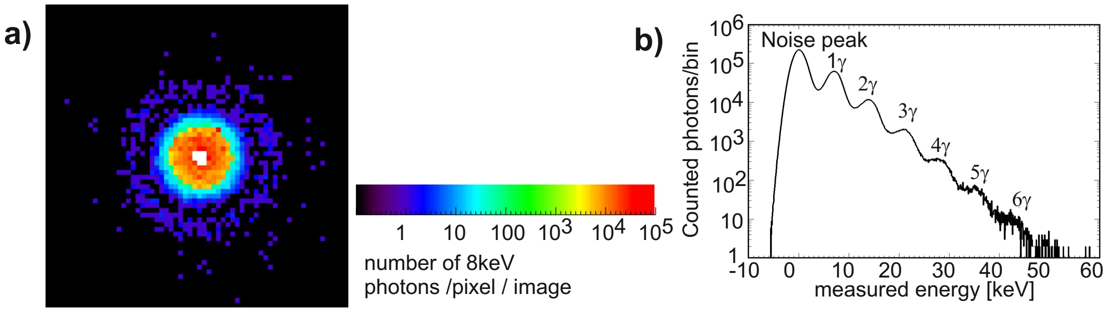

Figure 6: First data at Petra-III: (a) an image demonstrating the dynamic range and (b) Histogram of integrated photons

be repeated at the daisy-chained modules of the interface electronics. Advantages of this concept are the need of only a few lines for connections, the possibility of identical modules, multiple usage of same integrated I^2C devices without limits on the I/O-channel, short I^2C-lines for each segment, the need of different software-drivers for a limited number of devices and minimum coordination of I^2C-addresses and conflicts while the hardware development. But the access speed is slowed down, which can be coped with for the slow control of AGIPD and the software for the branching has to be developed once.

5. Off-detector data handling

Each $^1/_2$-Mega pixel part is controlled by two cables, which are galvanically separated at the driver side. One is for the slow control and firmware-boot via the micro-controller using 10/100 Megabit Ethernet and the reliable protocol TCP/IP. The other transfers the needed train and bunch synchronous information like train start, bunch clock and the reject information. Off detector these signal will be generated within a MTCA.4 system, called clock and control [11].

The image data and the tables from the storage-cell usage and reject are transfered via optical 10 GbE fibers into an off detector DAQ system. In a first stage, a train builder realized in ATCA [13] FPGAs and cross point switches sort the data to full images and trains. In a next stage a PC-farm allows higher level calculations and transfers the data into a storage facility.

6. First data

AGIPD has taken first data with a single ASIC mounted to a sensor[14]. The primary beam of a PETRA-III beam line at DESY was sent to the sensor. Within the images (figure 6) the coverage shows pixel responses to a few 10 000 X-rays with 8 keV energy. The histogram of the pulse heights is an overlay of well separated peaks counting the few 8 keV X-rays. At XFEL the peaks of 12.4 keV photons will even be further apart from each another. In June 2014 first beams have been sent to a full sensor equipped with all ASICs and readout by the full chain of PCBs.

7. Summary and outlook

XFEL's opens new fields of studies on objects at the atomic scale. In particular access to the structure of objects, which are destroyed even by low intensity X-rays will get realistic. The Eu-XFEL will provide 27 000 bunches/s for these studies. To make full use of them requires dedicated developments with new concepts or the adaptation of technologies from other fields of large scale instrumentation.

AGIPD develops a 1 Mega pixel camera for recording images at a bunch rate of 4.5MHz and keeping 352 images per 100 ms of each train for storage. All specialized developments for the whole fast signal chain are available and in first beam tests now. The control PCB's are in development. The logic algorithms, firm- and software developments are ongoing and will include over long time the operating experience.

The Eu-XFEL plans to provide beams from 2016 on and in 2017 first beams to the users[1].

Acknowledgments

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