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Upgraded readout and trigger electronics for the ATLAS liquid argon calorimeters for future LHC running

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The ATLAS Liquid Argon (LAr) calorimeters produce almost 200k signals that must be digitised and processed by the front-end and back-end electronics at every triggered event. Additionally, the front-end electronics sums analog signals to provide coarse-grained energy sums to the first-level (L1) trigger system. The current design was optimised for the nominal LHC luminosity of 10^{34} cm^{-2}s^{-1}. However, in future higher-luminosity phases of LHC operation, the luminosity (and associated pile-up noise) will be 3-7 times higher. An improved spatial granularity of the trigger primitives is therefore proposed, in order to improve the trigger performance at high background rejection rates. For the first upgrade phase in 2018, new LAr Trigger Digitiser Boards are being designed to receive the higher granularity signals, digitise them on-detector and send them via fast optical links to a new digital processing system (DPS). This applies digital filtering and identifies significant energy depositions in each trigger channel. The refined trigger primitives are transmitted to the L1 system, allowing extraction of improved trigger signatures. The concept for the upgraded readout and the components being developed for the new system are described. R&D activities as well as architectural and performance studies are on-going for the design of mixed-signal front-end ASICs, radiation tolerant optical-links, and the high-speed FPGA-based DPS units. These studies also guide the way towards the second upgrade phase, in which all LAr Calorimeter read-out electronics must be replaced due to radiation damage, ageing, and a new ATLAS trigger scheme.

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1. Introduction

The ATLAS detector [1] was designed and built to study proton-proton collisions produced at the LHC at centre-of-mass energies up to 14 TeV and instantaneous luminosities up to 10^{34} $\mathrm{cm}^{-2}\mathrm{s}^{-1}$. The ATLAS Liquid Argon (LAr) calorimeters produce almost 200k signals that must be digitised and processed by the front-end and back-end electronics at every triggered event. The current design of the first-level (L1) trigger system was optimised for the nominal LHC luminosity. However, in future higher-luminosity phases of LHC operation, the luminosity and associated pile-up noise will be 3-7 times higher. In order to improve the trigger performance at high background condition, an improved spatial granularity of the trigger information is proposed for the first upgrade phase in 2018 (Phase-I upgrade) [2].

2. Upgrade strategy

The existing calorimeter trigger information is based on the concept of a "Trigger Tower" that sums the energy deposition across the longitudinal layers of the calorimeters in an area of $\Delta\eta \times \Delta\phi = 0.1 \times 0.1$. The Trigger Tower is created through several stages of on-detector analog electronics.

The new finer granularity scheme is based on so-called "Super Cells", which provide information for each calorimeter layer for the full η range of the calorimeter, as well as finer segmentation ($\Delta\eta \times \Delta\phi = 0.025 \times 0.1$) in the front and middle layers of the EM barrel and end-cap for $|\eta| \leq 2.5$. This scheme is illustrated in Fig. 1. The digitisation precision of the Super Cell signals is improved by at least a factor of four compared to the existing L1 system optimising the quantisation scale and the dynamic range of the digitisers in each η-region and for each layer of the calorimeter to achieve sensitivities at the level of the Super Cell electronic noise or better. The transverse energy deposited in the Super Cells is calculated through optimised algorithm which is similar to the optimal filtering currently used in the LAr Readout Drivers. It provides results close to the energy resolution obtained from the offline reconstruction.

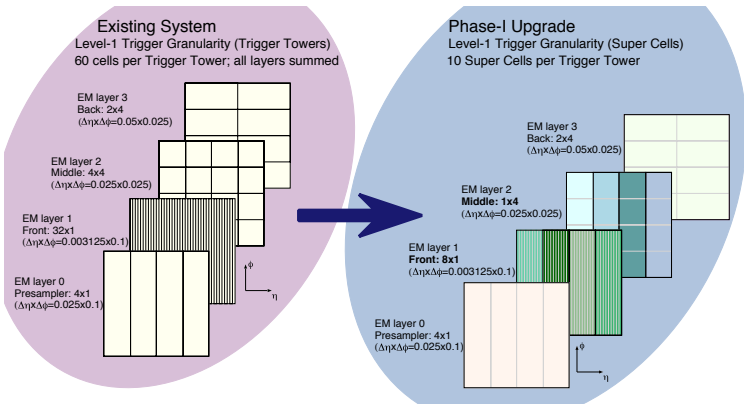
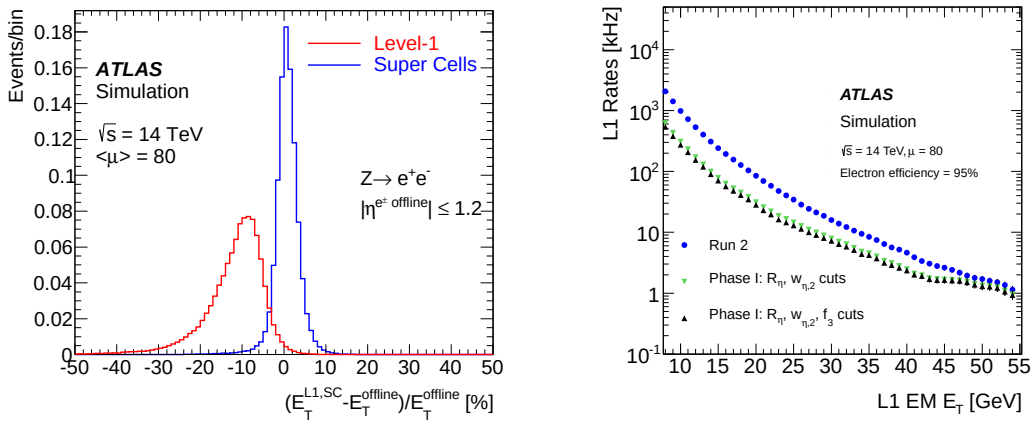


Figure 1: Geometrical representation in η, ϕ space of an EM Trigger Tower in the current system (left) and the Super Cells proposed for the Phase-I upgrade (right).

The high-granularity and high-resolution data provided by the Super Cells will enable the upgraded L1 trigger system to reconstruct electromagnetic clusters with improved precision. Preliminary studies shown in Fig. 2(a) demonstrate the significant improvement in the energy resolution using the Super Cells compared to the existing L1. These upgrades also enable better discrimination of EM showers due to electrons and photons from the background of QCD jets though the use of additional shower shape information. Fig. 2(b) demonstrates a substantial reduction in trigger rates when using these selection criteria, which translates into a possible reduction of the L1 trigger threshold by 7 GeV compared to Run 2 conditions (before Phase-I upgrade).



(a) (b)

Figure 2: (a) The percent difference of electron E_{T} between the existing L1 and offline compared that between the upgraded L1 with Super Cells and offline for simulated $Z \rightarrow e^{+}e^{-}$ events in the LAr EM barrel calorimeter. (b) L1 trigger rates for 95% electron efficiency as a function of the EM E_{T} threshold assuming Run 2 conditions and Run 3 conditions for two sets of selection criteria as measured from a sample of simulated minimum bias events.

To provide high-granularity and high-precision information to upgraded trigger processors, new LAr Trigger Digitiser Boards (LTDB) are installed in the available spare slots of the Front-End crates. Each LTDB will process up to 320 Super Cell signals with a total power consumption smaller than 156 W. Super Cell signals must be digitised at 40 million samples per second by the ADC on the LTDB. This ADC is also required to be radiation tolerant. The ADC word will be 12-bit with a frame clock at 40 MHz.

The digitised signals are processed remotely by the LAr Digital Processing System (LDPS) modules, which convert the samples to calibrated energies in real-time and interface to the trigger processors. The LDPS must receive the digital signal from the 124 LTDBs every 25 ns, and transmit these data to the L1 calorimeter trigger system. It requires the reception of ∼25 Tbps for 34,000 Super Cells and the transmission of ∼41 Tbps over optical fibres. The hardware implementation will be based on the ATCA (Advanced Telecom Computer Architecture) platform that supports the design for high-density, high-speed communication boards. The proposed LDPS is made of up to 31 LAr Digital Processing Blades (LDPBs) housed in three ATCA shelves. Each LDPB consists of one carrier board equipped with four Advance Mezzanine Cards (AMCs), for a total of 124 AMCs.

The AMC is designed around a powerful FPGA with high-speed transceivers that will process the data of up to 320 Super Cells within the latency of 14 bunch crossings.

3. R&D activities

3.1 Mixed signal front-end ASICs (LTDB)

There are two custom ASIC developments for the ADC to meet the requirement of low power consumption as well as radiation tolerance. A commercial off-the-shelf (COTS) ADC is also an option if it meets the electrical and radiation requirements. A 1/4 slice LTDB prototype has been built and is being tested, which has one digital motherboard and two analog mezzanines. The 1/4 slice digital motherboard hosts 10 COTS ADC (the Texas Instruments ADS5272). The analog waveforms can be digitised and read out correctly, and a more detailed test is ongoing now. The test results will feed back to the design of full size LTDB demonstrator which is planned to be installed on detector by mid 2014.

3.2 High speed FPGA-based DPS units based on ATCA (LDPS)

In order to evaluate a possible LDPB layout, one ATCA board with three Altera Stratix IV FPGAs has been designed, built and tested with fibres running up to 8.6 Gbps. The two front FPGAs are connected to 24 transceivers. Tests of the physical links up to 8 Gbps, configuration of two different link speeds for reception (5.1 Gbps) and for transmission (6.4 Gbps), data transmissions and reception at 8 Gbps between two FPGAs on the board, have been successfully performed.

4. Summary and prospect

The Phase-I upgrade project of the ATLAS LAr calorimeter is proposed to enhance the physics reach of the experiment in the high-luminosity environment foreseen in the next ten years. R&D activities as well as architectural and performance studies are on-going for the upgrade of readout electronics. Tests on demonstrator boards are going well and it was decided to install them to the ATLAS readout system for the run starting in 2015.

In the second upgrade phase planned in 2022-2023 (Phase-II upgrade), all LAr calorimeter readout electronics must be replaced due to radiation damage, ageing and a new ATLAS trigger scheme. The new electronics installed at Phase-I upgrade will be used as a Level-0 trigger and the new Level-I trigger will access the full granularity detector information to further enhance discrimination against backgrounds. Therefore, the Phase-I upgrade project is fully compatible with the ATLAS upgraded long-term plans.

References

[1] ATLAS Collaboration, "The ATLAS Experiment at the CERN Large Hadron Collider", *JINST* **3** (2008) S08003.

[2] ATLAS Collaboration, "ATLAS Liquid Argon Calorimeter Phase-I Upgrade Technical Design Report", ATLAS-TDR-022, 2013, `http://cds.cern.ch/record/1602230`.