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A Monolithic Active Pixel Sensor for the upgrade of the ALICE ITS

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Substantial upgrades of the ALICE experiment at the LHC are planned during the LHC Long Shutdown 2 (scheduled 2018-2019), including the full replacement of the Inner Tracking System (ITS) by a new detector based on CMOS Monolithic Active Pixel Sensors (MAPS) [1]. This paper presents the architecture of a first large scale monolithic pixel chip prototype (pALPIDEfs) implemented in the TowerJazz 180 nm CMOS imaging sensor technology [2], which is expected to reach a S/N, power density and readout time beyond the ALICE ITS upgrade requirements.

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1. Introduction

The new ALICE Inner Tracking System [3] will be composed of 7 layers of Monolithic Active Pixel Sensors. A smaller pixel pitch ($\sim 20\mu$m), beam radius (19 mm) to allow the inner layer to be closer to the beam line, and an extremely low material budget ($0.3\%X_0$ for each of the 3 inner layers and $0.8\%X_0$ for each of the 4 outer layers) should improve the overall pointing resolution by at least a factor 3 at $p_T < 0.5$ GeV/c ($\sigma_{r-\varphi} \sim 40$ µm at $p_T = 0.5$ GeV/c). To reach that low material budget, the power density must be limited to 300 mW cm^{-2} in the inner layers and to 100 mW cm^{-2} in the outer layers. The upper limit for the integration time is 30 µs to limit pile-up and keep the tracking efficiency sufficiently high while running with a 100 kHz trigger in Pb-Pb collisions and with a 400 kHz trigger in p-p collisions [3]. While these requirements can be achived by the traditional rolling shutter approach, used in the Mistral, Astral [4] and Cherwell architectures [5], the ALPIDE development tries to reduce power consumption and integration time well below these values, using a binary in-pixel front-end associated with a hit driven readout architecture.

2. Monolithic Pixels Technology

The TowerJazz 180 nm 6-metal CMOS imaging sensor process [2] has been chosen as it is possible to use full CMOS in the pixel due to a deep p-well (fig. 1 left) and different starting materials. The deep p-well [2] shields n-wells containing the PMOS transistors from the epitaxial layer and prevents them from collecting signal charge from the epitaxial layer instead of the n-well of the charge collection electrode. High resistivity epitaxial layers (between 1 kΩ cm and 6 kΩ cm) [10] allow more significant depletion with lower input capacitance and hence better S/N ratios. More depletion and a more important drift component in the charge collection is also known to favor radiation tolerance of the sensor [6]. For this reason it is possible to reverse bias the substrate on the pALPIDE prototypes. Deep submicron CMOS technologies are known to offer significant radiation tolerance due to their thin gate oxide [7]. This was experimentally confirmed also for this technology (with a gate oxide thickness of 4 nm) [8].

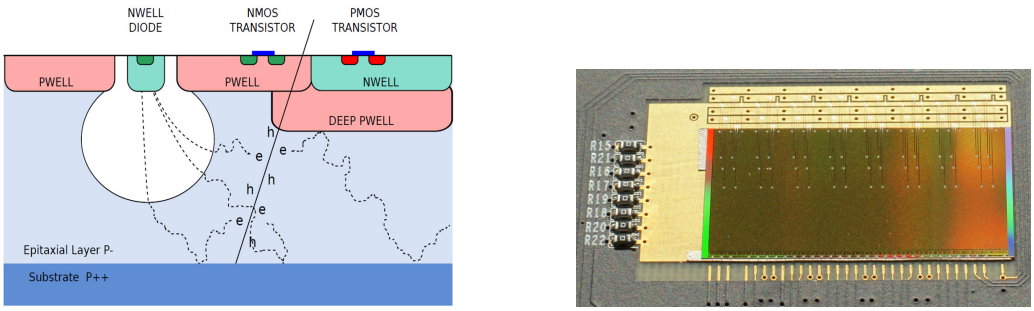

Figure 1: Cross sectional view of the TowerJazz 180 nm technology (left) and pALPIDEfs die picture (right).

3. ALPIDE development

pALPIDEfs[1] is a full scale monolithic pixel chip prototype developed in 2013 and currently under test (fig. 1 right). The die is 3×1.53 cm^2 and contains a pixel matrix of 1024 columns by 512 rows. The pixel size is 28 µm $\times$ 28 µm. The chip is divided in 4 sectors containing pixels with different anode geometries and reset mechanisms for test purposes (fig. 2 left).

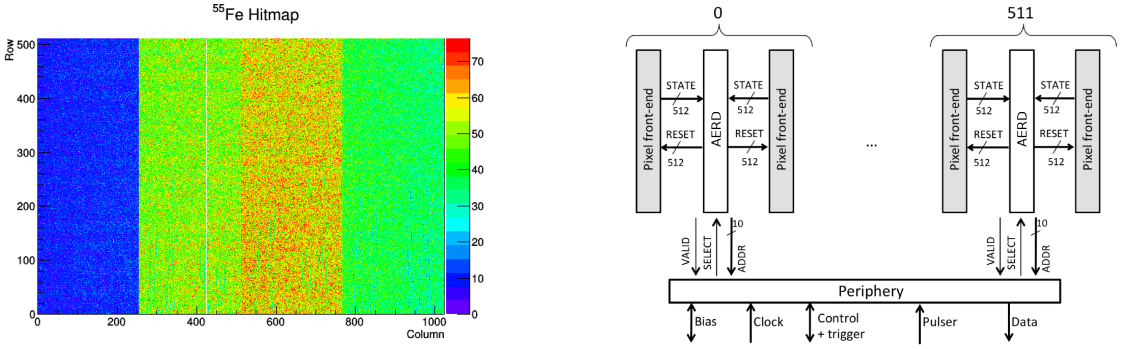

Figure 2: pALPIDEfs hitmap obtained with an iron source that shows the fours sectors with different anode responsitivities (left). pALPIDEfs scheme showing the signals at the interface FE-AERD and AERD-DP (right).

The anode signal is processed by a low-power non-linear current comparator circuit with a bias current of 20 nA and a peaking time of $1-2$ µs [9]. By asserting a global enable signal, which allows the output of each front-end to write to an in-pixel state register, at the peak of the analog output about $1-2$ µs after a potentially interesting event (minimum bias trigger), these events can be selected by the reducing of background and event pile-up.
The availability of binary hit information within the pixel eliminates most of the complications related to the propagation of analog signals to the end of columns and allows the implementation of fast in-matrix data encoding architectures. This is done in pALPIDEfs by means of asynchronous Address-Encoder Reset-Decoder circuits (AERD) each connected to a pair of columns (fig. 2 right). Each AERD is composed of 3 parts: a pixel state fast-OR, an address encoder and a reset decoder. If at least a pixel is hit in a pair of columns, a VALID signal propagates to the digital periphery. Upon VALID receipt, the digital periphery asserts the SELECT signal which enables the generation and propagation of pixel address (10 bit) based on a priority scheme (pixels with lower addresses are read before). Once the digital periphery has read the address, the SELECT signal is deasserted. This produces a reset of the pixel whose address was previously read. The procedure is iterated until all pixels are read in that column pair. To minimize the area of the digital periphery while keeping a reasonably low dead time of the chip ($\sim$ 10% at 100 kHz rate Pb-Pb interactions), the readout of the matrix is organized as follows: groups of 16 double columns (regions) are read in parallel and double columns belonging to the same region are read sequentially. Data in each region is compressed and stored into a multi event buffer (256×16 DPRAM). After the matrix is read, the 32 buffers are read sequentially and the data is transmitted to the off-detector electronics through a dedicated 8-bit output at 40 MHz (total bandwidth 320 Mb/s). This results in a small

[1] ALice PIxel DEtector full scale prototype

digital periphery (height $\sim 450\mu$m, less than 3% of pALPIDEfs height).
Considering the average hit density of the inner layers after LS2 (18.6 hit cm^{-2} evt^{-1}), the average number of hits per region is ~ 2.5. Since the readout time of each pixel is 100 ns and assuming an average cluster size of 4 pixels, the average readout time of the matrix is ~ 1 μs.
The total power density of this prototype is 70 mW cm^{-2} with the main contribution from the digital periphery, where no low-power techniques are implemented yet. The power consumption of each pixel is estimated to be ~ 40 nW, yielding an analog power density lower than 6 mW cm^{-2}. Assuming a 100 kHz trigger rate and a hit density expected in the inner layers of the ITS, the total power consumption of the 512 AERDs of pALPIDEfs is about 3 mW (power density less than 1 mW cm^{-2}).

4. Conclusions

Extensive R&D has been carried out in the last 3 years on MAPS for the ALICE ITS upgrade that lead to a first full scale prototype currently under test. Promising preliminary results are being obtained. New prototypes will be submitted in the short term (2014) to improve the digital power consumption, the AERD readout speed and to study solutions to other system integration aspects.

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