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# ROB performance in a high luminosity scenario

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The first layer of the CMS (Compact Muon Solenoid) DT (Drift Tube) read-out system is built around the ROBs (Read-Out Boards), which are responsible for the time measurement of the chamber signals to allow reconstruction of charged particle tracks with a resolution of 250 $\mu m$ per cell. ROB boards have shown an excellent performance during LHC operation and are expected to continue their operation safely during all LHC Phase 1 up to 2022. Present LHC upgrades for Phase 2 foresee an increase of instantaneous luminosity up to $5 \cdot 10^{34}\ cm^{-2} \cdot s^{-1}$ which will increase significantly the expected hit rate. Moreover, CMS is studying to increase the Level 1 Accept (L1A) latency of the trigger signal from 3.2 $\mu m$ to 20 $\mu m$ to allow including tracking subdetector information into the Level 1 trigger decision and also the $L1A$ frequency from 100 $kHz$ maximum to up to 1 $MHz$, in order to accommodate the increase of trigger rate due to the higher luminosity. ROB operation under such conditions has been studied and tested in the laboratory and results are presented in this paper.

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## 1. Introduction

CMS is a general purpose detector designed to run at the highest luminosity at the LHC collider. The central feature of the CMS apparatus is a superconducting solenoid of $6\ m$ diameter that generates a magnetic field of up to $4\ T$. Such a high field was chosen in order to allow the construction of a compact tracking and calorimetry system on its interior, and still performing good muon tracking on the exterior.

Muons are measured in CMS by means of three different technologies of gaseous detectors, and, among them, drift tubes –DT– are used.

*DT chambers* are responsible, not only for muon detection, but also for precise momentum measurement over a wide range of energies. When a muon or charged particle crosses one of the drift tubes, it ionizes the inner gas filling the chamber volume, and a small current is induced in the anode after a drift. This signal –*hit*– will be amplified and discriminated by the front-end electronics before being sent to the ROBs, which perform a time measurement of the signal with respect to the Level 1 Accept –*L1A*– trigger signal [2]. The position of the charged particle can be related to the time measurement since the drift velocity in the cell volume can be considered constant.

### 1.1 ROB and *HPTDC* description

ROBs are built around a 32-channel *HPTDC* ASIC developed by the CERN EP/MIC group [1]. This device supplies the basic time elements to reconstruct muon tracks, that is, the relative time to a common trigger for every hit produced on chamber wires.

Each ROB houses 4 *HPTDC* [2] that are connected inside the board in a clock synchronous token ring scheme for the read-out of the digital data (see Fig. 1.1). One of the *HPTDC*s is configured as master, controlling the token that authorizes data transmission to a common bus connected to a $240\ Mbps$ serializer.

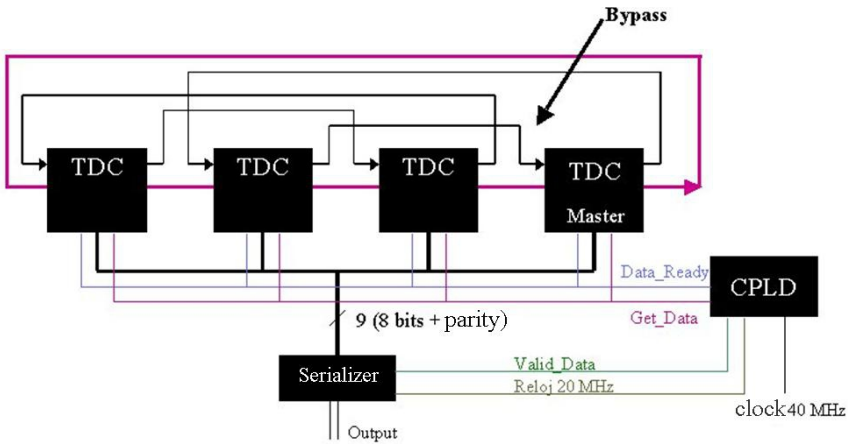


***Figure 1.1:*** *Diagram of the HPTDCs read-out interconnec-tions in the ROB*

The digitized signals from each of the 32 channels are stored in the input *hit registers* and then are driven to the 256-words-deep group memories –Level 1 buffers– common to every 8 channels [1]. The output of these group memories is merged into a common 256 deep memory

once the trigger matching[1] is performed. Until this operation can be done, the pending triggers are stored in a 16-words-deep FIFO.

Depending on the amount of created particles in a collision and the specific configuration used, ROB serial link and *HPTDC* internal shared buffers could be a bottleneck for sending all gathered data, leading to a situation where particle information is lost, due to lack of storage space into the *HPTDC* circuits.

### 1.2 LHC upgrade and ROB occupancy

Background distribution in the detector behaves linearly with luminosity, though geometrically inhomogeneous. Top sectors MB4s[2] are very much affected by single hits, presumably due to neutron background that permeates the cavern.

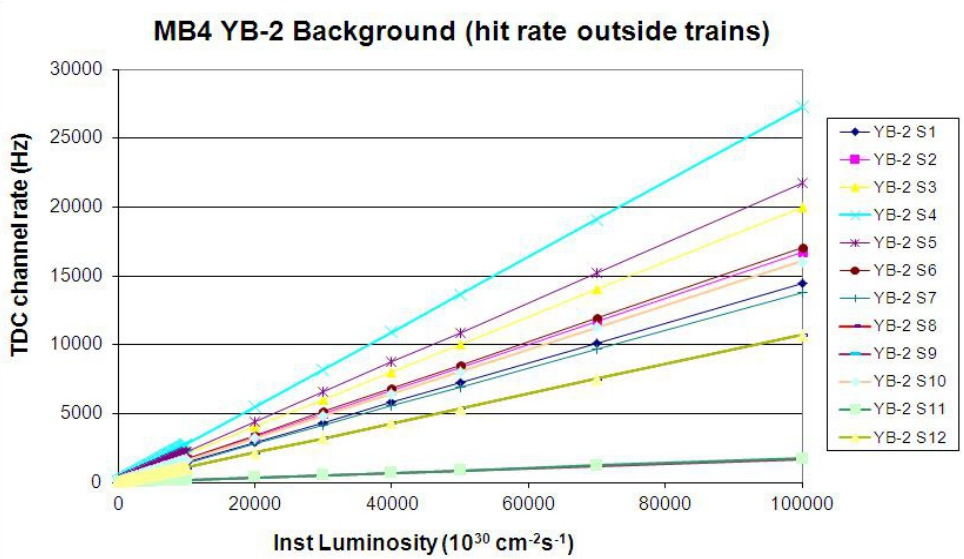


***Figure 1.2:*** *MB4 top chambers extrapolation of the background rates measured in the different chambers for luminosities up to $10^{35}$ $cm^{-2}{\cdot}s^{-1}$. Single or double hits in a time window of 250 ns before the bunch trains are selected, i.e. this is out of time background, likely neutrons*

Extrapolating linearly these measurements to $10^{35}\ cm^{-2} \cdot s^{-1}$of instantaneous luminosity (see Fig. 1.2), we obtain maximum rates of $27\ Hz/cm^2$ which correspond to $27\ kHz/TDC\ channel$ for the worst MB4.

This measurement corresponds to the background rate outside of the bunch trains, so one needs to add the contribution of prompt signals from collisions (measurement inside bunch trains). In case of MB4s of external wheels, the total value of maximum uncorrelated hit rate per *HPTDC* channel can be assumed around $30\ kHz$, during Phase 2.

Contribution from muons, punch through, or track-like signals, should also be considered since these hits are correlated –arrive in the same time window– and their contribution to the number of words being read is large. These can be estimated from the chamber trigger rates, and

[1] This mechanism is enabled, by default, during normal LHC operation.

[2] MB4s are muon chambers located at the CMS outermost iron yoke place. For a deeper description of them look at reference [2]

have been extrapolated for different luminosity levels. In Fig. 2.1 the extrapolated rates to $10^{35}\ cm^{-2} \cdot s^{-1}$ and $14\ TeV$ can be seen for each of the different chambers. In the case of the MB4s, we obtain maximum values of $200\ kHz$ per chamber which, in this case, due to different size, translates into $40\ kHz/ROB$ and $10\ kHz$ track rate per *HPTDC*.

## 2. Test description

The test stand comprise a single ROB board that has been connected to a Control-X and a Patgen boards[1], and powered by an external power supply.

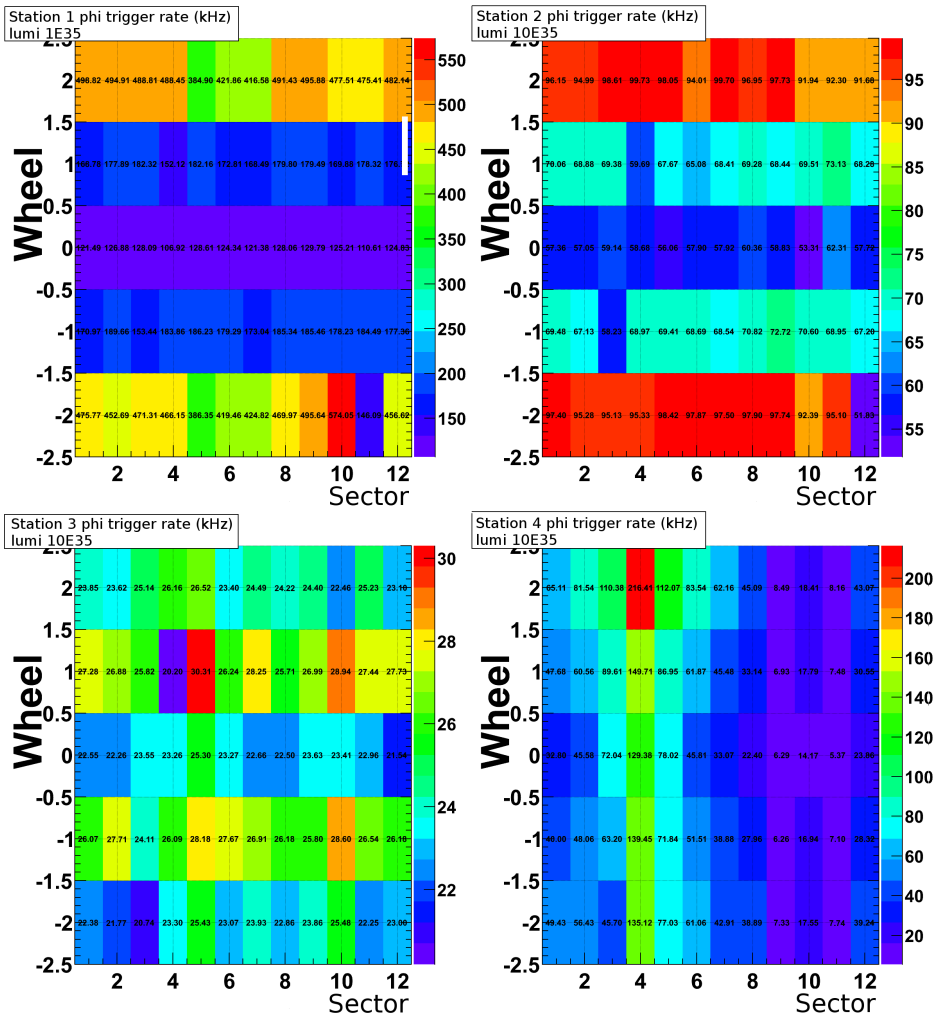


***Figure 2.1:*** *Extrapolation of the trigger rate versus luminosity including the correction to 14 TeV center of mass energy*

The test procedure emulates operation at LHC with signal hits sent through different channels and a Level 1 trigger signal delayed $20\ \mu s$, the expected Phase 2 latency. The goal of the test is to operate the ROB at increasingly high occupancy conditions, and study the limits at which it cannot handle such hit and/or trigger rate levels. ROB processing speed capability depends on two aspects:

[1] Those are two 6-U VME specific boards developed at CIEMAT, ad-hoc, for CMS. Their firmwares have been partially redesigned to cope with the requirements for planned ROB tests.

- the number of hits selected per event which depends on the input signal frequency and on the number of channels that receive hits;
- the frequency of the *L1A* trigger signal which will determine the amount of hits that are validated and, thus, need to be sent to the next level. It is also worth noting that, for each trigger, the ROB sends, by default, a header and a trailer 32-bit word, which will contribute to limit the ROB processing speed.

In order to test systematically the ROB operation, we will control the number of ROB channels enabled, the number of hits validated for each trigger and the frequency of the trigger signal, which will be the same that the hit frequency.

## 3. Experimental results

Tests results, described in previous section, are sumarized in plot in Fig. 3.1, where the total hit number, per event, being processed by the ROB board without error, are represented as triangles. The continuous interpolated curve represents the maximum number of hits that can be processed per event versus the *L1A* trigger rate. We have also verified that the number of hits, at which ROB gives overflow, is independent from the position of any hit inside the configured time window. This was tested by varying the delay between hit and trigger, along the whole time window width, while the system was running.

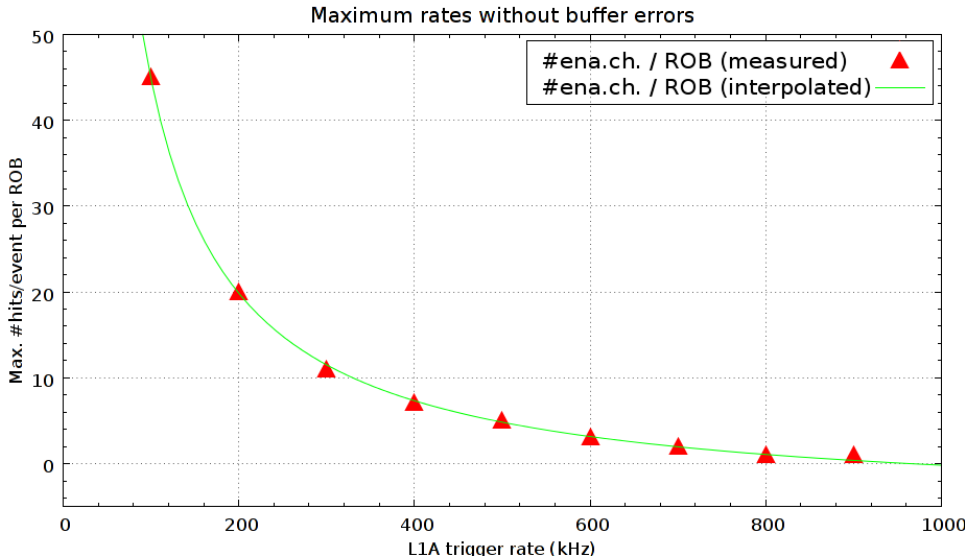


***Figure 3.1:*** *Relationship between the L1A rate and the num-ber of hits processed without error*

It is necessary to note that these values have been obtained in the worst case, because hits have been spread out among all *TDC*s. If only a single *HPTDC* has pending data to be sent, processing is faster, whereas, if many *HPTDC*s have stored information, they need to wait for getting the token before data sending, inserting a delay of around 2 clock cycles per *TDC* into the process.

As it could be observed, there is a decreasing monotonic relationship between the maximum ROB event size processing capability and the hit and *L1A* frequency.

In order to find any correlation between the *TDC*, where hits are being injected, and a possible bottleneck caused by this particular *TDC*, many tests have been repeated maintaining constant the hits rate and the total number of enabled channels, but only alternating the pattern of enabled channels per *HPTDC* and/or channel group.

We have verified, by testing different ROBs in the same conditions, that the errors obtained are identical for the same patterns and frequency of input and trigger signals. The different tests performed, confirm that the round-robin tokenized mechanism [1], used by the *TDC* chain to decide which device can send its data, is the main bottleneck for operating at higher Level 1 trigger rate.

### 3.1 Effect of the Level 1 Accept latency

To study the effect of increasing the latency from few $\mu s$ to 20 $\mu s$ we have performed a test with a fixed trigger rate and two differente latency values: 3.8 $\mu s$ (which is present latency for the ROB boards at CMS) and 20 $\mu s$.

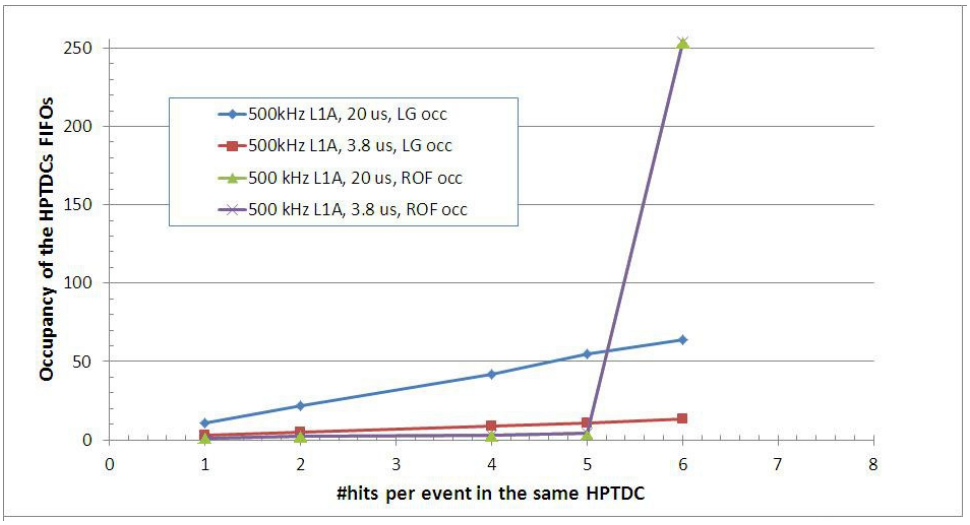


***Figure 3.1.1:*** *FIFOs ocupancy at 500 kHz of L1A accept rate, varying hit rate. 500 kHz ROF 20 µs occupancy is completely overlapped by 500 kHz ROF 3.8 µs line.*

We have measured the occupancy of the L1 buffers (LG) and of the read-out FIFO (ROF) and the results have been plotted in Fig. 3.1.1. As can be seen, the occupancy of the ROF is inde-pendent of the latency programmed, since it depends only on the amount of data that needs to be transmitted through the serial link. However, the LG occupancy increases with higher values of the latency, since it needs to wait longer to perform the event matching. Nevertheless, the buffer size is 256 words, so in both cases with approximately 60 words maximum, we are far from saturating these buffers. In summary, operation of the ROBs with up to 20 $\mu s$ latency is considered safe, independently of the trigger rate used.

### 3.2 Discussion of results

The next step is to calculate which is the equivalent channel rate that will produce the obtained number of hits per event per ROB, in order to obtain the maximum *L1A* rate acceptable for the occupancy levels expected in HL-LHC.

In order to do that, it is not enough to multiply the number of hits by the trigger rate and divide by 128 channels per ROB. Since the background rate is not correlated with the trigger rate, we need to insert a correction factor that takes into account which fraction of the absolute time we will be reading with a time window of $1.25\ \mu s$.

Table 1 shows the maximum uncorrelated hit rate obtained for each *L1A* frequency.

| L1A Rate | # hits / ROB / event | Max. uncorrelated hit rate / channel |
|---|---|---|
| 100 kHz | 45 | 281 kHz |
| 200 kHz | 20 | 125 kHz |
| 300 kHz | 11 | 68 kHz |
| 400 kHz | 7 | 44 kHz |
| 500 kHz | 5 | 31 kHz |
| 600 kHz | 3 | 19 kHz |
| 700 kHz | 2 | 12 kHz |
| 800 kHz | 1 | 6.25 kHz |
| 900 kHz | 1 | 6.2 kHz |

***Table 1:*** *Uncorrelated hit rate vs L1A frequency.*

As it can be seen, in theory we could achieve up to $500\ kHz$ *L1A* rate for the expected MB4 occupancy at $10^{35}\ cm^{-2} \cdot s^{-1}$ with no safety margin. However, we still need to add the contribution of the track rate, which is $10\ kHz$ for the MB4s. This rate will always include 8 hits per ROB, so in reality, a Level 1 Accept rate bigger than $300\ kHz$ is not considered safe.

## 4. Conclusions

This paper has described a group of tests that explores the throughput limits that can be achieved by CERN's CMS experiment read-out –ROB– boards, using *HPTDC*s as digitizer circuits. They show that there is a monotonically decreasing dependency between the maximum read-out capability of a ROB and the *L1A* trigger and hit rates. Throughput limits due to round-robin method, used to coordinate different *HPTDC*s data sending through the board link, has been found one of the major barriers in order to achieve higher read-out data rates. The fact that 4 *HPTDC*s share the same 240 Mbps serial link, imposes critical constrains to the maximum Level 1 Accept rate that can be allowed.

## References

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