PROCEEDINGS OF SCIENCE

Initial Upgrade of the ATLAS Level-1 Calorimeter Trigger

Duc Bao Ta for the ATLAS Collaboration*
Michigan State University
E-mail: xiedebao@googlemail.com

The Level-1 calorimeter trigger (L1Calo) of the ATLAS experiment has been operating well since the start of Large Hadron Collider (LHC) data taking, and played a major role in the Higgs boson discovery. To face the new challenges posed by the upcoming increases of the LHC proton beam energy and luminosity, a series of upgrades is planned for the L1Calo. This paper presents the first L1Calo upgrade program for the initial upgrade phase in 2013-14. The program includes substantial improvements to the analogue and digital signal processing. Two existing digital algorithm processor subsystems will receive substantial hardware and firmware upgrades, allowing topological information to be transmitted and processed. An entirely new subsystem, the L1 topological processor, will receive real-time data from both the upgraded L1Calo and L1 muon trigger to perform trigger algorithms based on entire event topologies. The expected performance improvements are described together with the upgraded hardware and firmware implementations.

ATL-DAQ-PROC-2014-014
24 June 2014

Technology and Instrumentation in Particle Physics 2014,
2-6 June, 2014
Amsterdam, the Netherlands

*Speaker.

PoS(TIPP2014)410

1. Introduction

The ATLAS [1] trigger consists of three levels of event selection systems, Level-1 (L1), Level-2 and the event filter. The last two levels form the high-level trigger. While the high-level trigger is implemented in software algorithms that run on a computer farm, the L1 trigger is implemented in custom-made hardware. The L1 trigger in run-1 can reduce the event rate from the 40 MHz collision rate down to a rate of 75 kHz. The front-end electronics are designed as a pipelined system with a maximum latency of 2.4 μs. Inputs to the L1 central trigger processor (CTP), which takes the trigger decision, are received from the muon trigger system using hits from dedicated muon trigger detectors and the L1 calorimeter trigger system (L1Calo) using reduced-granularity information from the calorimeters. The signatures that can be triggered on by the L1 system are combinations of thresholded multiplicities of high-p_{T} muons, of energy clusters in the electromagnetic calorimeter deposited by electrons/photons and of energy clusters in both the electromagnetic and hadronic calorimeters from hadronic jets or τ leptons. For electron/photons and τ trigger objects isolation from neighbouring energy entries can be required. In addition, configurable thresholds on transverse energy sums can be added to the signatures. The summed multiplicity information from the different objects that passed configurable thresholds are transmitted to the CTP, which will take the decision to accept the event at the first trigger level (L1A). The L1Calo system will be supplemented in run-2 by a new topological trigger processor.

2. New architecture of the Level-1 Calorimeter trigger system for the initial upgrade

The L1Calo consists of three main sub-systems: the Pre-Processor (PP), the Cluster Processor (CP) and the Jet/Energy Processor (JEP) system with their corresponding modules, PPMs, CPMs and JEMs, where each module is assigned to a certain detector region. The muon L1 trigger system is not described further, but more information on this and the L1Calo system can be found in [2]. A sketch of the current architecture can be found on the left side of Figure 1, while the right side shows the new architecture of the L1Calo system for the initial upgrade.

The upgrade of the current architecture was chosen to accommodate the expected higher amount of data from the collisions as the result of higher of centre-of-mass energy and the higher instantaneous luminosity. It was staged into an initial upgrade phase and a phase-1 upgrade stage to take into account the limited amount of time that is available for upgrades during the first long shutdown of the LHC.

2.1 New multi-chip-modules (nMCM)

The analogue input signals from the main electromagnetic and hadronic calorimeters are summed on the calorimeter front-end electronics. The reduced granularity provides so-called projective trigger towers of mostly 0.1×0.1 in size (in units of the pseudorapidity, η, and azimuthal angle around the beam axis, φ). The analogue signals are sent to the PPMs, which are located outside of the detector volume in the service caverns. The PPMs condition and digitise the input signals using the so-called multi-chip modules (MCM) in run-1. The MCMs associate the analogue pulse to a certain LHC bunch-crossing and applies pedestal subtraction, final E_{T} calibration, noise suppression, and turning off problematic channels in one step via look-up tables.

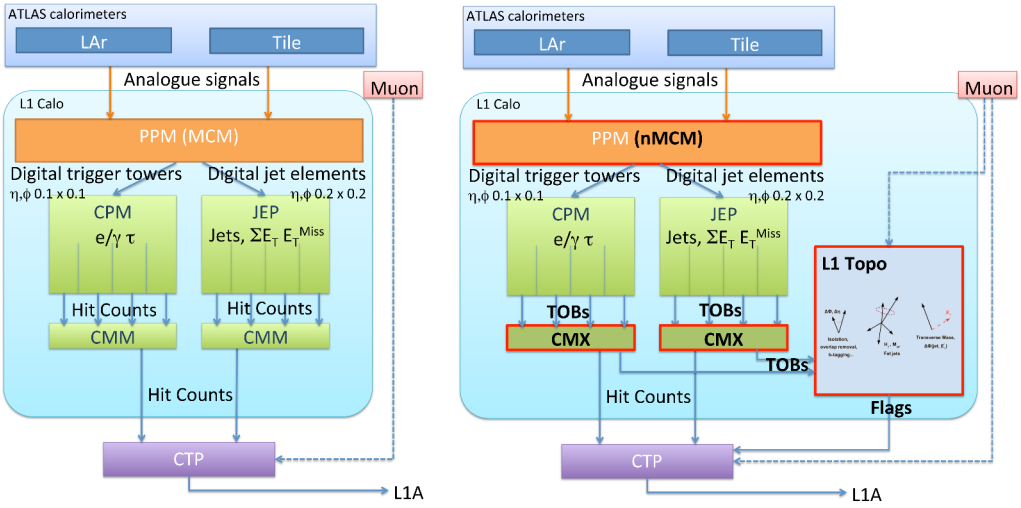

Figure 1: Schematic sketch of the ATLAS Level-1 calorimeter trigger system (L1Calo). On the left side the current system is shown. The right side shows the planned scheme for the initial upgrade.

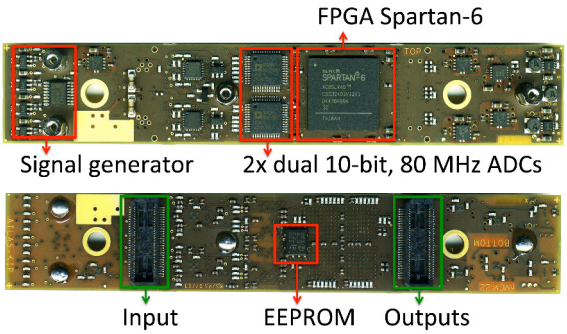

Figure 2: Photograph of the front- and backside of the nMCM. The important components are highlighted as well as the analogue and digital data interfaces.

The nMCM is a plug-compatible device on which the custom ASICs from the MCMs are replaced by one FPGA (Xilinx Spartan-6) for better and flexible signal processing, e.g. the choice and sign of digital filter coefficients, and the possibility of using different types of filter. The four inputs from the calorimeters are digitised to ten-bit precision at 80 MHz in two dual-channel ADCs. The signal processing runs at the LHC clock frequency of 40 MHz, but the saturated-pulse processing uses the full 80 MHz samples. The digital signals are transmitted serially on LVDS links to the CP and JEP subsystems at 480 Mbps, but the serial link to the JEP system can be upgraded to 960 Mbps at the next upgrade stage. The FPGA architecture allows for a second look-up table that would allow more optimized tables for each electromagnetic and hadronic calorimeter energy deposition. The assignment of the bunch crossing ID (BCID) can be improved using the 80 MHz samples from the nMCM, so that the correct BCID can be assigned even to high pulses. Also with the FPGA, fluctuations of the pedestal induced by pile-up can be corrected in an algorithmic or parametric way. The nMCM also features a programmable analogue signal generator used for standalone tests.

2.2 Extended common merger module (CMX)

The digitised information sent by the MCMs/nMCMs is sent in parallel to the digital processor

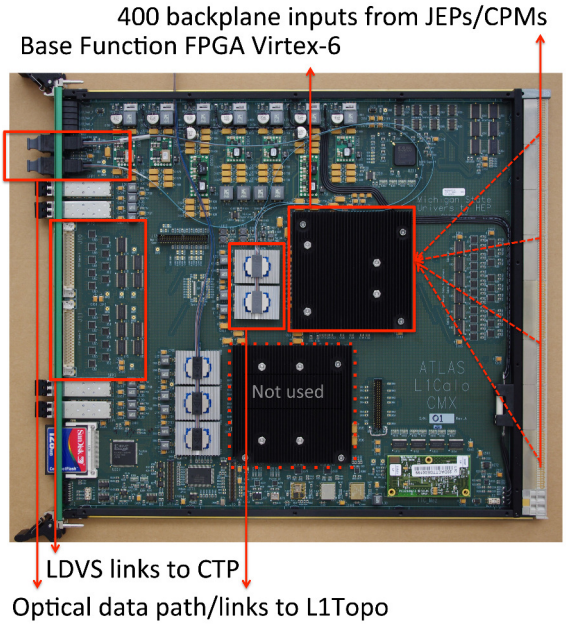

Figure 3: Photograph of the CMX module. The important components are highlighted as well as the data interfaces to the JEMs and CPMs (backplane), to the L1Topo (optical data interfaces at the front panel) and to the CTP (LVDS connectors at the front panel).

subsystems, the CP system and the JEP systems. The CPs use the full trigger tower granularity in the central region to search for small localised clusters typical of electron, photon and τ-lepton candidates. The JEPs operate on jet elements with a granularity of 2×2 sums of the trigger towers to identify jet candidates and to form global transverse energy sums: missing, total and jet-sum transverse energy and missing transverse energy significance. In the run-1 architecture, the energy sums and the multiplicity of trigger objects that passed energy thresholds and isolation criteria are then transmitted to the common merger modules (CMM) that will sum the information from the different detector regions.

The CMX replaces the CMM to enable a four times higher bandwidth (160 Mbps) over the data path within the CP and JEP systems. This higher bandwidth allows the transmission of the location and energy of the trigger objects (TOB) instead of their thresholded multiplicities. Also the aforementioned energy sums will be transmitted to the CMX. The thresholding of TOBs has been moved to the CMX and it can process almost twice as many selection and isolation thresholds for each of the trigger objects compared to the original system. Sums of the multiplicities from different detector regions are still formed before the information is sent to the CTP. Finally, the CMX prepares zero-suppressed TOBs for the L1Topo.

This base functionality of the CMX is realised on a modern FPGA (Xilinx Virtex-6). The TOBs to the L1Topo are transmitted via 24 6.4 Gbps optical fibres. Similar to the CMM, LVDS links to other CMXs and the CTP are provided. The CPM and JEM hardware will remain the same, they will only receive firmware updates to provide their data at the increased bandwidth over the existing crate backplane.

2.3 Topological processor (L1Topo)

To have an additional handle on the L1 trigger rates, a new topological processor was designed to use the topology of the event and the relationship of the TOBs for the trigger decision. This is especially important, since the trigger rates for the same simple energy thresholds of run-1 are

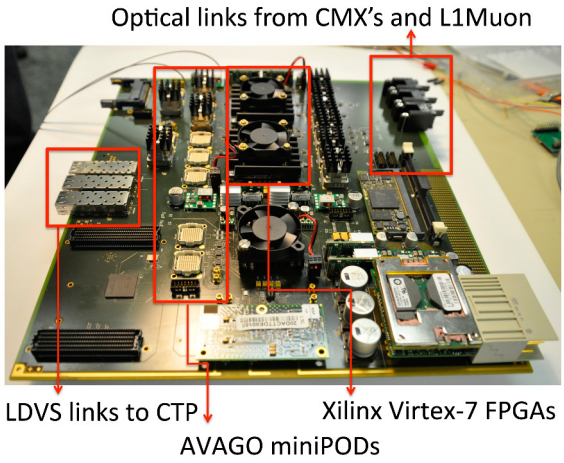

Figure 4: Photograph of the L1Topo module. The important components are highlighted as well as the data interfaces to the CMX and L1 Muon modules (right side) and to the CTP (left side).

expected to increase over the managable limit. Examples are $\Delta\eta$ or $\Delta\varphi$ between two objects or the effective mass, M_{eff}, of the event. For certain topologies, e.g. $H/Z \to \tau\tau$, a $\Delta\eta$ cut reduce the trigger rate by 25% compared to energy threshold triggers. The L1Topo module needs to receive the trigger objects from the L1Calo and L1 muon systems to make the trigger decision based on the correlation between trigger objects. Flags indicating that a certain event topology was fulfilled will be sent to the CTP, which will use these flags to form the L1A.

The L1Topo will be implemented as a single ACTA shelf with two or more L1Topo processors. The data from the L1Calo (CMX) and the L1 muon system is received by fibre cables. The optical signals are routed to 12 Avago MiniPOD optical receivers. The converted electrical signals are fed into the two processing FPGAs (Xilinx Virtex-7) via their on-chip multi-gigabit transceivers (MGT). The baseline link speed of is 6.4 Gbps with standard 8b/10b encoding provides ~5.1 Gbps of payload for each of the 160 inputs to the two main FPGAs.

Many topological trigger algorithms are under study by the physics groups. The firmware is developed in a modular structure, such that the central algorithms are separated from the generic functions such as sorting of the TOBs. Changes of the topological trigger algorithms are planned on a regular basis and it requires firmware updates. The topological trigger has access to 64 jet, 32 muon, 120 e/γ and τ TOBs plus missing transverse energy. The algorithms for the correlations of objects are only limited by the total latency for the L1A.

3. Summary

The ATLAS L1Calo initial upgrade will cope with the challenges of the LHC run-2 at higher energies and luminosity. For the increased pile-up conditions, an improved and more flexible analogue-digital signal processing is being installed. The introduction of a new topological algorithm processor will help to manage the increased trigger rates. The trigger object inputs to this new subsystem will be provided by an upgraded digital processing system which will operate at a four times higher bandwidth. Successfully tested prototypes of the L1Topo and the digital processing system are available and production modules are available for installation and integration. The upgraded system is foreseen to operate for the whole run-2, after which a second, substantial upgrade phase is planned where initially a parallel operation with new L1Calo systems is planned.

References

[1] The ATLAS Collaboration, *The ATLAS Experiment at the CERN Large Hadron Collider*, *JINST* **3** (2008) S08003.

[2] R Achenbach et al, *The ATLAS Level-1 Calorimeter Trigger*, *JINST* **3** (2008) P03001.