PROCEEDINGS OF SCIENCE

Data Acquisition System with data reduction in real-time mode

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The Data acquisition system consists of the signal recorder operating in a real-time mode, the synchronization system providing in-phase operation of multiple channels of the recording system and the communication modules interfacing with an operator PC via the Ethernet 10/100 channel. Recorder based on the ADC with the sampling frequency of 500 MHz and the amplitude resolution of 12 bits. Due to that the digital unit of the recorder is built on a PLD (Programmable Logic Device), the data acquisition system software includes the ability to modify data processing algorithms for the specific diagnostics (interferometry, laser scattering, spectroscopy, refractometry and others) in a real-time mode. The synchronization system consists of two main modules: the timer and the synchronization unit. The accuracy of binding the output data to the trigger pulse is determined by the sampling frequency of data acquisition system recorders.

Technology and Instrumentation in Particle Physics 2014
2-6 June, 2014
Amsterdam, the Netherlands

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PoS(TIPP2014)416

1. Introduction

Nowadays studies performed in the field of plasma physics and controlled nuclear fusion is continuously becoming more complex. They advance new challenges on the diagnostic equipment. It includes specialized digital flow-oriented data processing for the some diagnostics. This solution allows to exclude the interpolation procedures and to obtain the results of the plasma parameters measurements in the real-time mode.

These devices provide information on the current plasma parameters in new applications, e.g., in the discharge control subsystems, which stabilize plasma filament positions in the magnetic trap, support its shape and density, and suppress the magnetic hydrodynamic and kinetic instabilities.

By now, the time of plasma confinement in the magnetic traps has been significant increased. It requires the data acquisition system to store large amounts of the information.

Data acquisition system with data reduction solves these problems. This system was developed for plasma system GOL-3 and GDT (Russia, Novosibirsk) [1].

2. Structure of data acquisition system

Data acquisition (DAQ) system includes folowing elements:

1. The photodetector modules based on avalanche photodiodes S30659E -1060 firm Perkin Elm;
2. The recorder ADC12500 based on high-speed 12-bit ADC with the sampling frequency of 500 MHz.

   As the added elements are used:
3. The module providing the communication between the photodetector modules and PC in the channel Ethernet 10/100;
4. The synchronization module forming the sampling frequency of the ADC modules to ensure their synchronous operation;
5. The timer module, which distributes the triggering and synchronization pulses to all recording subsystems. This ensures the unity of the time scales of the all recording subsystems;
6. Ethernet switch connecting all modules of the system to computer.

The figure 1 shows photo of data acquisition system. Let us consider in more detail some of the DAQ system key elements.

2.1 Recorder ADC12500

The figure 2 shows a functional diagram of the recorder ADC12500 [2, 3]. Each of measuring tracks includes wideband amplifiers with programmable gain, the DAC for offset zero of the input signal, coupling amplifier with differential output and 12-bit ADC (analog digital converter) ADS5463, which fixes the input signal with sampling rate of 500 MHz. The digital part controls

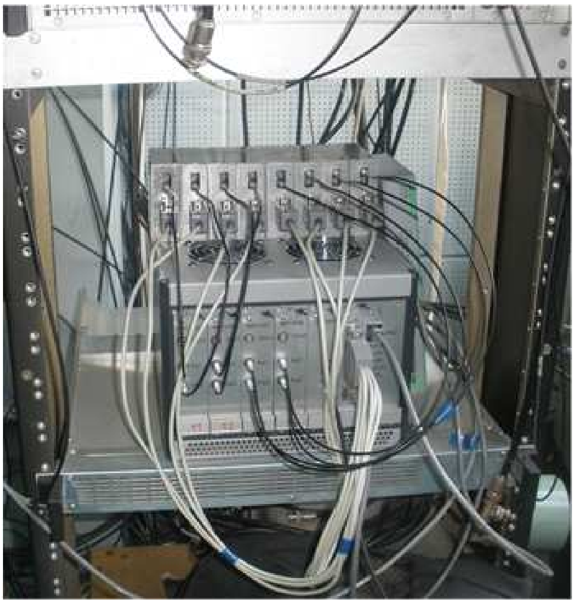

Figure 1: Photo of data acquisition system

the measurement channels, provides data receiving from the ADCs and writes them to the external buffer memory. The digital part is based on the field programmable gate array (FPGA). The recorder includes VCO PLL reducing phase noise of external reference clock, Ethernet-10/100 link controller and additional I/O port. Port can be used to control the external devices. It is used on the GOL-3 and GDT to control the photodetector modules. The feature of the recorder ADC12500 is its software ability to process signals in real time mode. In data acquisition system for Thomson scattering diagnostics on the GOL-3 and GDT, the recorder ADC12500 is used for signal interpolation. In other applications data reduction can be done by form separation of pulses (neutron diagnostics [4]), calculation of the phase shift (interferometry) or by formation of the energy spectrum (spectroscopy) [5]. It is independent file that can be easily connected to the main project.

The ability to process data in real time is implemented using buffer storage A67P0636AE.

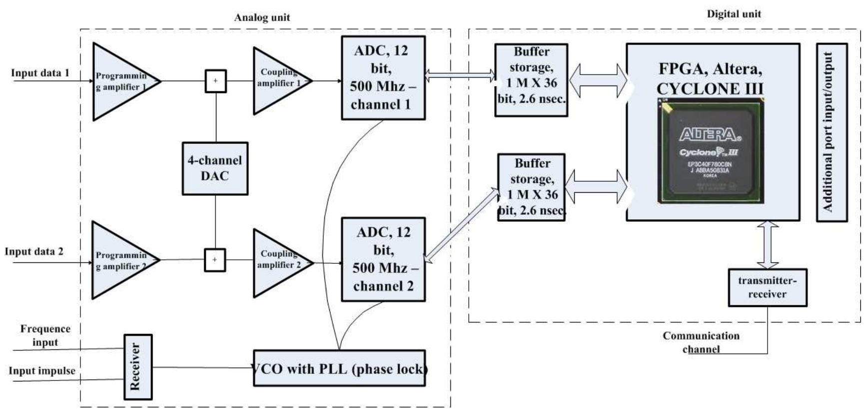

Figure 2: Functional curcuit of data acquisition system

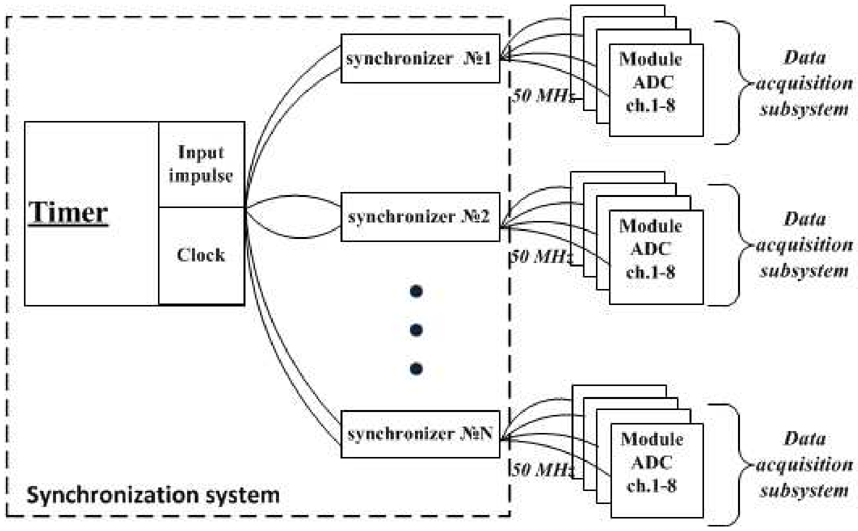

Figure 3: Functional curcuit of syncronization system

This crystal can record 36-bit data at speeds of 166 MSPS.

The recorder modules have the following characteristics: the bandwidth is 0–150 MHz, setting time at the accuracy $\sim$8 ns and the noise voltage (root-mean square) referred to the ADC input $\sim$150 μV.

2.2 Syncronization system

The figure 3 shows a functional diagram of the synchronization system. The system has a hierarchical structure and consists of two main modules:

1. Timer module;

2. The synchronization module.

Timer module is a master module of the synchronization system. It forms the reference clock for all measurement subsystems. The timer receives the external trigger pulse with the amplitude of 5–10 V and duration of 20–100 ns. The positive edge of the pulse determines the beginning of the data registration. The trigger pulse is fed to the eight-channel digital delay line. This allows starting measuring subsystem at the user-defined times. The start and clock pulses can be transmitted with copper and fibre cables. The timer generates the reference clock for synchronization of the eight modules. In turn, each synchronization module can distribute start and clock pulses to the eight recorder modules.

2.2.1 Timer module

The external start pulse is received by the eight-channel software-controlled delay line which is based on the FPGA MAX II. FPGA generates the eight start pulses. Each of them formed by the digital delay line can be located relative to the start pulse with a delay divisible by 20 ns at intervals of up to 1.35 μs. Binding the start pulses to the clock rising edge for each channel is performed in the FPGA.

Clock is generated using crystal AD9552. The pulse-repetition frequency is 50 MSPS. The control of delay line and load of registers of crystal AD9552 are performed by the microcontroller. The time delays for the start pulse and control constants for the crystal AD9552 form with help of integrated interface SPI. The microcontroller is connected to the PC through 10/100 Ethernet. The start pulses from FPGA and clock from crystal AD9552 are fed to the electrical or fibre output drivers/transmitters and transmitted with corresponding communication lines.

2.2.2 Syncronization module

The synchronization module must receive the external start pulse and the reference clock with optical or electrical lines. Therefore, its structure includes the following elements:

1. The optical/electrical receiver of clock and the start pulse;

2. The main module which provides performing basic functions of the synchronizer.

The optical receiver is based on HFBR24 receivers and provides conversion of the optical signal to electrical. The resulting signals are fed to the high-speed comparators ADCM603 and ADCMP552. It allows matching levels of signal with levels of the basic module. In the case of the electrical receiver, signals from the input connectors are directly come to the comparators ADCM603 and ADCMP552. The main module of the synchronization module includes:

1. The crystal AD9552 providing «clean up» clock received from the timer. This operation reduces the value of the aperture uncertainty of the reference clock to 0.5 ps;

2. The crystal SY58052U providing a binding external trigger pulse to the clock reference;

3. The output buffer ADCLK948 having low latency and aperture uncertainty. This allows to avoid the degradation of the clock generated by crystal AD9552;

4. The microcontroller which sets output clock parameters in crystal AD9552 after power up.

3. Conclusion

The data acquisition system for Thomson scattering diagnostics for the GOL-3 and GDL (INP SB RAS, Novosibirsk, Russia) has been successfully completed. Four registration subsystems have been installed at the GOL-3. Each of which includes eight ADC signal recorders. GDT has got two such registration subsystems.

The recorder modules ADC12500 find application in other fields of the plasma physics. For example, they are used in the neutron diagnostics for separation of the gamma rays and neutrons, in the interferometry to calculate the phase shift and in the spectroscopy to generate the energy spectrum [5].

The synchronization system considered can be used in other applications. For example, it is used in the data acquisition system for the Globus-M (St. Petersburg, Russia) [6].

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