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3D Silicon Detectors

Gian-Franco Dalla Betta[1]
University of Trento and INFN TIFPA
Via Sommarive, 9 – 38123 Povo di Trento, Italy
E-mail: gianfranco.dallabetta@unitn.it

Twenty years after their introduction by Sherwood Parker and collaborators, 3D silicon detectors have reached their maturity. The ATLAS IBL represents an important milestone: it is the first application of 3D technology to a High Energy Physics experiment, and it has demonstrated the feasibility of a medium volume production with a relatively good yield. In spite of this significant achievement, the future Phase 2 upgrades of experiments at the HL-LHC are setting very challenging demands in terms of smaller pixel size, reduced sensor thickness, and ultra-high radiation tolerance, calling for the development of a new generation of 3D sensors. This paper reviews the state of the art in 3D detectors, and addresses the next directions of their development in view of the application to HL-LHC. The main design and technological issues are reported, as well as preliminary results from TCAD simulations

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1. Introduction

First introduced by Sherwood Parker in 1997 [1], 3D silicon detectors consist of an array of columnar electrodes of both doping types, oriented perpendicularly to the wafer surface and penetrating entirely through the substrate. This unique structure enables to decouple the active sensor thickness from the electrode distance, offering important advantages in terms of low operation voltage, fast time response [2] and high radiation tolerance [3]. Additionally, 3D technology allows for "active edges", i.e., deep trenches heavily doped to act as ohmic terminations of the sensors, able to reduce the insensitive edge region to a few micrometers [4]. Of course this comes at the expense of a more complex and expensive technology [5], due to the use of several non standard techniques, such as Wafer Bonding (WB) [6] and Deep Reactive Ion Etching (DRIE) [7].

In the past few years, very important progress has been made in the development of 3D sensors, passing from the earlier R&D phase with performance demonstration on a few prototypes (1997-2006) to more systematic studies (2007-2010) and finally to an industrialization phase (2011-2012), which led to the first application of 3D sensors in a High Energy Physics experiment, i.e., the ATLAS Insertable B-Layer (IBL) [8]. Besides confirming the excellent performance and radiation hardness of 3D sensors [9], this important achievement also demonstrated the feasibility of medium volume productions with a relatively good yield (~60% on selected wafers) [10], thus paving the way to using 3D detectors in other experiments planned for the phase 1 (e.g., the ATLAS Forward Physics experiment [11]), and phase 2 upgrades at the High Luminosity LHC (HL-LHC) [12]. In fact, while the former can use the same sensors developed for the IBL [13], the latter are setting more challenging demands in terms of smaller pixel size, reduced sensor thickness, and ultra-high radiation tolerance, that present 3D sensors cannot meet. As a result, a new generation of 3D sensors has to be developed, calling for a dedicated R&D effort, for which the main requirements, some ideas and preliminary results are presented in this paper.

The paper is organized as follows: in Section 2, the state of the art is reviewed; in Section 3, the requirements for 3D sensors to be used in phase 2 upgrades at LHC are outlined; possible technological approaches for future 3D sensors are discussed in Section 4, and preliminary layouts and TCAD simulation results are reported in Section 5. Conclusions are drawn in Section 6.

2. State of the art

The state of the art in 3D detectors is represented by the IBL sensors, which were developed within the ATLAS 3D Sensor Collaboration with a joint effort of all the processing facilities involved (Stanford, SINTEF, FBK, and CNM), although the final production was carried out only at FBK and CNM [8]. Two different technological approaches currently exist for 3D sensor fabrication: single-sided full 3D with active edges, and double-sided 3D with slim edges.

The single-sided approach was originally proposed at Stanford [5] and is now also available at SINTEF [14]: column etching is performed all through the substrate from the front

side of the sensor wafer for both types of electrodes, at the same time implementing active ohmic trenches at the edge. Columnar electrodes and trenches are completely filled with polysilicon. The bottom side is oxide bonded to a support wafer. This requires extra steps to attach and remove the support wafer.

The double-sided approach was independently developed by CNM [15] and FBK [16],[17] in slightly different versions: junction columns are etched from the front side, ohmic columns from the back side, without the presence of a support wafer. In the CNM processing, columns do not pass all through the wafer but stop at a short distance from the surface of the opposite side [15]; this was also the case for the first prototypes of FBK sensors [16], but the technology was later modified to allow for passing through columns [17].

Other aspects worth being recalled are the following:

a) single-sided 3D sensors can be made with four-side active edges [4], that instead are not feasible with double-sided 3D sensors, due to the absence of a support wafer. As an alternative, slim edges have been adopted for the IBL with a dead area of about 200 μm: while CNM sensors feature a 3D guard ring, surrounded by two rows of ohmic columns, FBK sensors feature a termination only based on ohmic columns [18];

b) in single-sided 3D sensors the substrate bias is applied from the front side, i.e., the same side where bump bonding is made. A possible alternative would require a post-processing treatment after support wafer removal: a hole in the insulating layers on the back side should be etched, and a metal wire bond pad should be deposited, but these extra steps are not fully engineered. On the contrary, in CNM and FBK sensors the substrate bias is applied from the back side, which makes these sensors compatible with standard planar sensors.

c) on wafer electrical tests are of paramount importance to identify bad pixel sensors at an early stage, before bump bonding. To this purpose, Stanford, SINTEF and FBK deposit a temporary metal layer that allows current-voltage tests to be performed in each sensor, whereas in CNM sensors the quality is evaluated by measuring the guard ring current. While the former method was proved to be very accurate, the latter failed to detect defects in the center of the sensors, so it is not reliable enough [19].

From the point of view of the electrical characteristics, one aspect to be carefully considered in view of operation at very large radiation fluences is the possibility to bias 3D sensors at the most appropriate voltage. In this respect, breakdown voltage could be an issue. In case of FBK IBL sensors, the breakdown voltage was relatively low, of the order of 50 V before irradiation and up to about 160 V after irradiation. After completing the IBL production, it was then decided to modify the technology and the design to improve the breakdown voltage. In particular, since the weakest point was demonstrated to be the junction column to p-spray junction on the back side, the junction columns were shortened stopping at about 20 μm from the opposite surface; moreover, the front side layout was improved [20]. As a result, the breakdown voltage was significantly increased both before and after irradiation [21].

In terms of functional properties, remarkable performances have been demonstrated for the IBL 3D sensors: in particular, they have shown hit reconstruction efficiency >98% for 15º inclined tracks at 160 V bias after $5x10^{15}$ n_{eq}/cm^2 [9]. Very encouraging results have also been obtained from the characterization of 3D pixel prototypes compatible with the PSI46 read-out chip [22],[23].

An important remark concerns the signal efficiency (SE) of heavily irradiated 3D sensors, which represents a key advantage compared to planar sensors: it was shown that SE essentially depends on geometrical considerations, as expressed by Eq. (1) [24]:

$$SE = \frac{1}{1 + 0.6L\frac{K_\tau}{v_D}\Phi} \quad (1)$$

where L is the inter-electrode spacing, K_τ is the damage constant for the electron effective trapping time, V_D is the electron drift velocity, and Φ is the irradiation fluence. Figure 1 shows a compilation of data relevant to irradiated 3D sensors from different manufacturers, featuring similar values of L, and showing very high signal efficiencies up to high fluences in good agreement with Eq. (1).

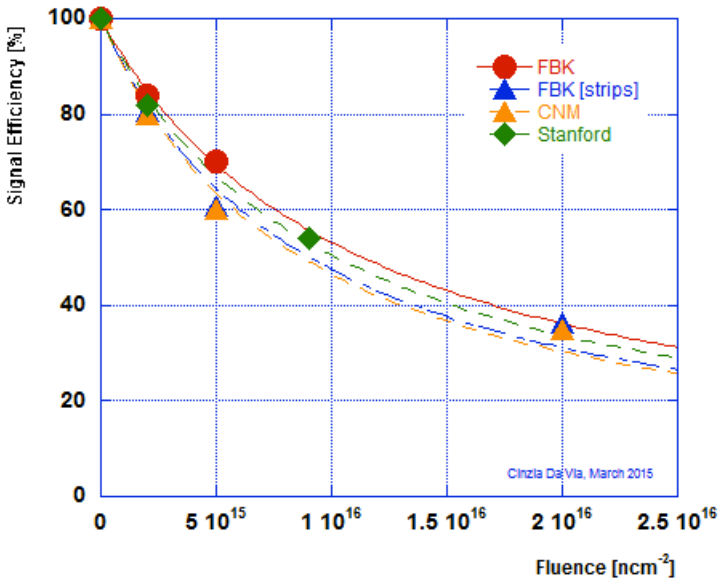

Figure 1 Compilation of signal efficiency in irradiated 3D sensors with fitting curves according to Eq. (1). With respect to the original plot from [10], and including data from FBK pixels [9], CNM strips [25], and Stanford diodes [26], new data from FBK strips are added [27].

3. Requirements for phase 2 upgrade experiments

Despite the IBL 3D sensor performances are remarkably good, the phase 2 upgrades at the HL-LHC call for several improvements, in particular in terms of increased radiation hardness (the maximum expected fluence for the inner layer is 2×10^{16} n_{eq}/cm^2) and capabilities of an efficient and accurate reconstruction of the tracks produced by charged particles in environments where their spatial density is very high. Occupancy considerations push towards a much higher granularity with respect to the pixels currently installed at the LHC: as an example, pixel dimensions considered by the RD53 Collaboration in the development of future read-out chips in 65nm CMOS technology are 50x50 μm^2 and 25x100 μm^2 [28]. Another requirement is to substantially reduce the material budget of each detection layer in order to improve the

accuracy of the reconstruction of primary vertices and decay. Moreover, a high geometrical efficiency should be pursued to allow for a more hermetic detector design.

The implications of these requirements on 3D sensor design and fabrication technology are manifold and mutually correlated: on one hand, a small inter-electrode spacing (L), comparable with the average carrier drift length due to charge trapping at the maximum considered fluences, is necessary to ensure the radiation hardness. On the other hand, in order to take advantage of the smaller pixel size for a high spatial resolution, the sensor active thickness should be decreased, so as to obtain smaller cluster dimensions. Thinner sensors also contribute to reduce the overall material budget and guarantee optimal track momentum resolution. Further reduction of the material budget can be obtained by implementing active edges (or at least very slim edges), preventing from overlaps between adjacent modules, which are needed to build a hermetic detector, thus reducing the amount of material in those specific regions of solid angle.

Both a small L and a small pixel size lead to a high density of columnar electrodes, with a detrimental effect on the geometrical efficiency (the electrode themselves are not efficient) and on the capacitance (noise). In this respect, electrode diameter should be reduced: assuming the aspect ratio (depth to diameter) attainable with DRIE to be constant, this calls for thinner substrates. In turn, since the electrode capacitance scales with its depth to a large extent, thinner substrates also mean lower noise. Finally, narrower electrodes on thin substrates can ease their (at least) partial filling with poly-Si to obtain some efficiency, at least before irradiation, and to allow for a higher layout flexibility.

From all the above considerations, making 3D sensors on thinner substrates appears the best solution, but there are also two important drawbacks to be considered: the first, obvious one is that thinner substrates also mean lower signals generated by impinging particles, so the thickness cannot be too small and the optimum value should be carefully determined as a compromise of several factors and also taking into account the properties of the read-out chips, and in particular the capability to operate at low thresholds.

The second problem with thinner substrates is their compatibility with the sensor fabrication facility and with the bump bonding process. With reference to FBK, the double-sided technology [17] used for the IBL production proved to offer several advantages in terms of process complexity, overall fabrication times, and sensor assembly within a system, mainly due to the absence of the support wafer. Nevertheless, it is not easy to process a wafer thinner than 200 micron without a support wafer, and this problem is even more critical for 6”- diameter wafers, to which the FBK pilot line was upgraded in 2013. As for the bump bonding, a serious problem with thin wafers is that they are prone to high bowing at the end of the process, whereas low values are normally required (e.g., <50 μm) in order for the yield of bump bonding to be acceptable. As a result, for thin 3D sensors, single-sided processes with support wafer should be preferred.

4. Technological approaches to make thin 3D sensors

With reference to Figure 2, some possible options can be envisioned:

a) according the original approach developed at Stanford, a sensor wafer of the desired thickness is oxide bonded to a support wafer (SOI substrate), which provides a good

mechanical stability during processing. Both junction (red) and ohmic (blue) columns can be made passing-through, with p-spray on both sides. The main problem is the support wafer removal, for which no fully engineered solution exists to date, and the difficulties, both in terms of layout and assembly, with providing the bias voltage from the front-side (i.e., the same side of the pixels where bump-bonding is performed), unless metal contacts could be made on the back-side after support wafer removal (post-processing).

b) an interesting alternative, compatible only with non-passing-through junction columns (to avoid early breakdown at n^{+}/p^{++} junctions), is using epitaxial wafers or SiSi direct bonded wafers, where a high resistivity sensor layer is grown/attached on top of a low resistivity substrate; the latter should be finally removed, but a thin portion of it could be left that would still allow a back-side metal to be deposited to apply the bias voltage.

c) As an alternative to support wafer removal as a post processing, option (a) can be followed by local thinning (by DRIE or by wet etching, e.g., by TMAH) of the support wafer from the back-side, while leaving frames of support wafer at the periphery of each sensor to improve its mechanical stability.

d) In case ohmic columns are etched also through the bonding oxide layer, local thinning from the back-side would expose the ohmic columns, thus allowing for bias voltage supply from the back-side by depositing an aluminium layer.

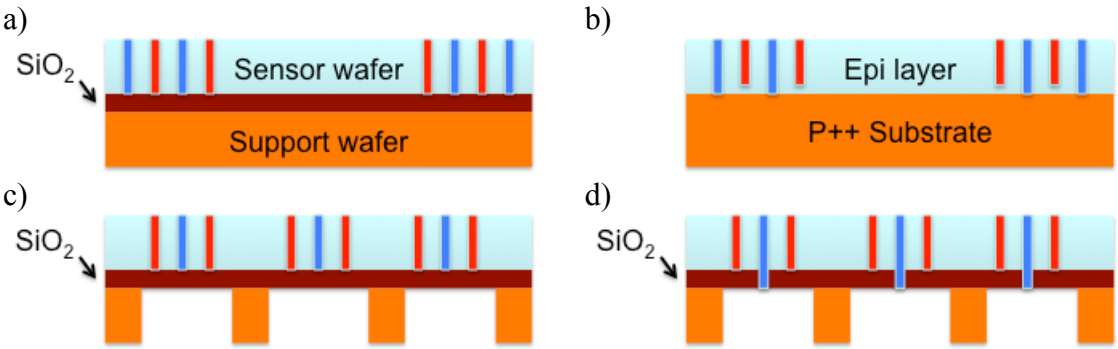

Figure 3 Possible single-sided technological options for thin 3D sensors: (a) SOI wafers "a la Stanford"; (b) epitaxial or Si-Si direct bonded wafer; (c) SOI wafers with back-side local etching; (d) SOI wafers with ohmic columns passing through the oxide and back-side local etching.

All approaches of Fig. 2 use a support wafer, so they are compatible with active edges [4]. As an alternative, slim edges can still be used: those developed for the IBL used a conservative design of 200µm [18], but tests made with more aggressive dicing have shown that 75µm would be sufficient with the present electrode structures, and further improvement are possible either by higher density column designs or different electrode shapes [29].

5. Preliminary results

With reference to the technological approach of Fig. 2(b), to be carried out on SiSi direct bonded wafers from Icemos Ltd., preliminary layouts of new 3D pixels compatible with the read-out chips from the RD53 Collaboration have been designed. The considered column

diameter is 5 μm that was proved to be feasible by FBK for DRIE etching down to a depth of about 150 μm, corresponding to an aspect ratio of almost 30:1.

Figure 3 (left) shows the layouts for the 50x50 μm^2 and the 25x100 μm^2 pixels. The former features one junction (N) column (1E) at the center of a cell, with an inter-electrode spacing L of about 36 μm. In this layout there's room enough to place the bump bonding pad at either side of the junction column. On the contrary, for radiation hardness considerations, the 25x100 μm^2 pixel is designed with two junction columns (2E), with an inter-electrode spacing L of about 28 μm. In this case the layout is pretty dense and there are strong constraints on the placement of the bump bonding pad, that would be anyway close both to the junction columns and to the ohmic columns, making this layout not so robust against misalignment problems. In this respect, more flexible designs could benefit from the possibility to place the bonding pads right on top of the junction columns in case they are completely filled with poly-Si.

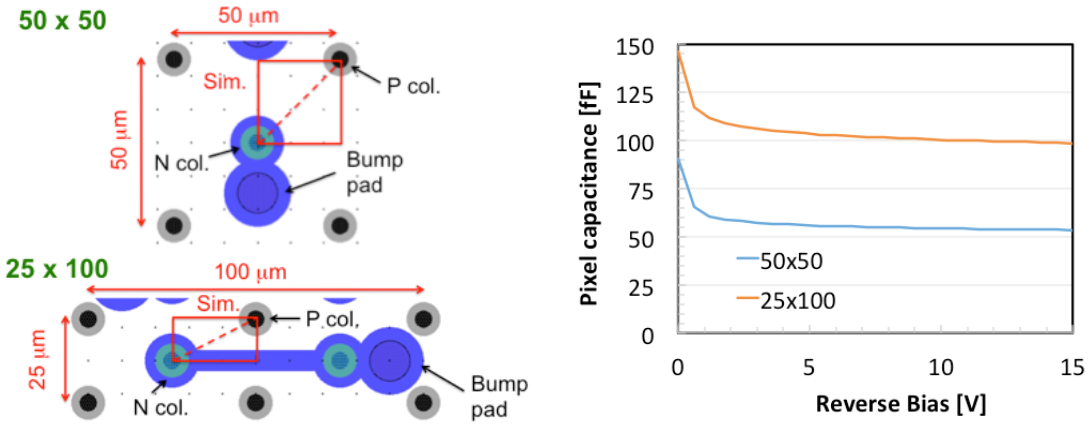

Figure 3 Pixel layout (left) and simulated pixel capacitance for an active thickness of 150 μm (right).

The two pixel layouts were evaluated by using TCAD simulations performed with Synopsys Sentaurus. All technological parameters are representative of FBK technology. Simulation domains are those indicated by the red square/rectangle in Figure 3 (left): owing to symmetry considerations, these are the simplest basic cells that can be considered. For capacitance simulations, three-dimensional domains of 150 μm thickness and junction column depth of 130 μm have been used in order to properly account also for surface effects, that were found to be non negligible in the IBL 3D pixel sensors fabricated at FBK [30]. On the contrary, for charge collection simulations, quasi-2d simulation domains, i.e., 1-μm thick slices, have been considered, incorporating the "Perugia" trap model [31] modified as described in [32] to account for bulk radiation damage.

Figure 3 (right) shows the simulated capacitance versus voltage curves. It can be seen that, owing to the small value of L, full depletion is achieved at very low voltage. The capacitance values are about 50 fF for the 50x50 μm^2 pixel and about 100 fF for the 25x100 μm^2 one: this is mainly due to the 1E configuration of the former and the 2E configuration of the latter. Both values include all contributions intrinsic to the 3D sensor, but not that from the bumps, that

might add a few tens of fF. In this respect, it is clear that the 25x100 μm^2 pixel is more critical with a total capacitance that would exceed the 100 fF limit set by the RD53 Collaboration [28].

As far as the signal efficiency is concerned, simulations of the two pixels at different irradiation fluences are reported in Fig. 4. Owing to the smaller value of L, the superior performance of the 25x100 μm^2 pixel is evident both in terms the maximum values of the signal efficiency and of the voltage necessary to reach them. In particular, with reference to the maximum fluence, it can be seen that the 25x100 μm^2 pixel features a signal efficiency of more than 50% already at 120 V, whereas the signal efficiency of the 50x50 μm^2 pixel slightly exceeds 30% (and is not yet saturated) at 250 V.

Nevertheless, it should be mentioned that the considered radiation damage model was validated up to irradiation fluences in the order of $1x10^{15}$ n_{eq}/cm^2 and tends to underestimate the signal efficiency at higher fluences. As an example, the same model provided an excellent agreement with experimental data for 3D sensors from FBK irradiated with protons at $1x10^{15}$ n_{eq}/cm^2 [33]. On the contrary, it did not reproduce the charge collection properties of 3D sensors irradiated with protons at $2x10^{16}$ n_{eq}/cm^2, and in particular it failed to predict the experimentally observed double-junction effect [27]. Improved trap models should therefore be used in the future to account for radiation damage at these very high fluences.

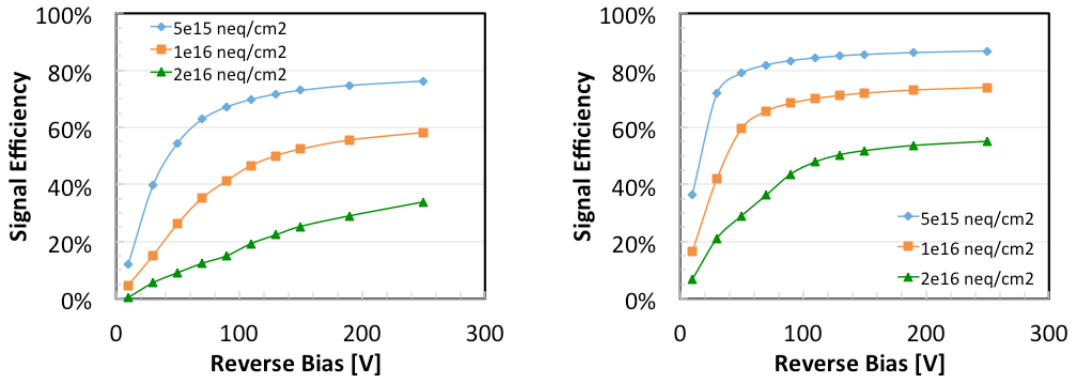

Figure 4 Simulated signal efficiency at different irradiation fluences for the two pixel layouts: 50x50 μm^2 (left) and 25x100 μm^2 (right).

6. Conclusions

Very impressive progress has been achieved in 3D detectors in the past few years, boosted by the ATLAS IBL project, and including demonstration of medium volume productions with reasonably good yield. However, the very demanding requirements of the phase 2 upgrades at HL-LHC call for the development of a new generation of 3D pixel sensors, with ~2x downscaling of all device dimensions, and improved radiation tolerance.

A 3-year R&D program (namely the ACTIVE project) has been jointly proposed to INFN by ATLAS and CMS to push 3D pixel technology towards HL-LHC requirements. The ATLAS-CMS synergy and the tight partnership with FBK can give a unique opportunity for technical leadership in the most demanding inner-most layers of HL-LHC detectors. During the first year of the project, FBK successfully proved the feasibility of the most critical process

steps (e.g., the etching by DRIE and filling with poly-Si of narrow columns), and the quality of a new raw material (e.g., SiSi direct bonded wafers). In parallel, the TCAD simulations, design and layout editing of new 3D sensors have been performed at the University of Trento. The fabrication of the first 3D batch is now being started at FBK.

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