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Electronics for HL-LHC Calorimetry

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The current read-out electronics of the ATLAS and CMS calorimeters will not sustain the running conditions expected at HL-LHC and needs to be replaced. We present a short overview of the proposed future architectures and of the on-going studies to develop the components necessary to implement such upgrade plans. Emphasis is set on R&D studies which are (or might be) in common between the experiments.

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1. Introduction

Both the ATLAS [1] and CMS [2] experiments are planning significant upgrades [3] of their calorimeter read-out and trigger electronics for operating at the High Luminosity LHC (HL-LHC), the so-called Phase II.

Several factors are driving the changes and the technological choices being investigated:

- Radiation resistance. By the end of Phase II, the detectors would have accumulated an integrated luminosity of around 3000 fb^{-1}. The lifetime of all detector components should be checked against this integrated dose and, if needed, replaced with more radiation tolerant versions.

- Ageing. Some components would have around 30 years of operation if they are still used in Phase II. This is a much longer period than the lifetime expected (of the order of 10 years) when they were designed and built. This poses serious reliability issues. Moreover, due to the lack of spares, obsolescence of the components and of the technologies, they are also increasingly difficult to maintain and repair.

- Performance. The expected increase in instantaneous luminosity ($5x10^{34}$ cm^{-2} s^{-1} with an expected average number of interactions per bunch crossing of μ=140) will degrade the performance of the calorimeters unless their read-out systems undergo substantial upgrades. This should allow the implementation of a new trigger architecture that will make use of the highest granularity information and resolution at the lowest possible trigger level. Improved calorimeter trigger primitives for electrons, photons, τ's and jets will be possible making extensive use of the detailed topology of the clusters and of the events. Moreover, the calorimeter trigger should allow matching with the planned track trigger at Level 1.

The new calorimeter read-out architecture will follow some general trends also in common to the other sub-detectors:

- All on-detector sums will be removed and only full granularity data will be transferred to the down-stream electronics.

- Data will not be buffered in the front-end, but rather streamed off-detector at the LHC bunch-crossing frequency (40 MHz).

- Fast pre-processors will be needed to convert raw data into calibrated information that feed the trigger system where improved and more complex algorithms can be applied.

- Off-detector buffers allow for a much higher trigger latency or purely software-based triggers.

2. Common Issues

To accomplish the program briefly sketched in the previous section, substantial changes are required on both the front-end and back-end systems of the ATLAS and CMS calorimeters. Problematics can be different between the experiments, due to the different calorimeter technologies

implied. However there are several issues which are in common between the experiments and that can profit from common developments.

- On-detector front-end electronics. The requirements asks for preamplification and shaping stages with low noise, fast shaping times and linearity over the full dynamic range, even after irradiation with the expected dose. The output of the preamplification stage needs to be digitized at the sampling rate of 40 MHz. The ADC must provide 12-bit resolution with 15/16-bit dynamic range to cover the full range of interesting energy deposits in the calorimeter. Low latency, low power consumption, radiation tolerance and immunity to Single Event Effects (SEE) are also required. Both Commercial Off-The-Shelf components (COTS) and custom ASIC developments are being pursued.

- High speed optical data links ($\gtrsim$10 Gb/s) are needed to transfer the large amount of data produced. COTS or custom developments (like the CERN GBT project) are under investigation. Radiation tolerance, in particular with respect to SEE, is one of the most important issues in such a development program.

- High performance back-end systems. Data transferred from the front end to the back end, will be processed by FPGA-based cards. For integrating these cards into a shelf system, the Advanced Telecommunication Computing Architecture (ATCA) has been selected in most cases. This is an open, multi-vendor framework that provides shelf and power management, fast fabrics and redundancy. While ATLAS seems oriented towards using the ATCA standard, CMS has chosen the μATCA standard, which supports mezzanine boards, conform to the AMC (Advanced Mezzanine Card) standard, connected directly to the backplane (without the need of a carrier card). Alternatively, development of high-bandwidth systems based on PCIe cards to interface detector specific front-end to DAQ systems on a switched network can be considered.

- New power distribution scheme. The replacement of the front-end electronics has the implication that new (lower) voltages will be needed to power the new boards. In one of the proposed design, starting form an intermediate voltage (12V or 24V) generated by main converters, Point-Of-Load (POL) regulators are used to perform DC-DC conversion on the front-end board. Commercial or custom solutions are being tested for low ripple, radiation hardness and sensitivity to magnetic field. For the analog part of the front end, for low-noise operation, Low Drop-Out (LDO) regulators are considered.

3. ATLAS

Electromagnetic calorimetry in ATLAS is provided by high-granularity lead/liquid-argon (LAr) sampling calorimeters. The electromagnetic calorimeter is divided into a central barrel ($|\eta| < 1.475$) and end-cap regions on either end of the detector ($1.375 < |\eta| < 2.5$ for the outer wheel and $2.5 < |\eta| < 3.2$ for the inner wheel). An iron/scintillator tile calorimeter gives hadronic coverage in the central rapidity range ($|\eta| < 1.7$), while a copper/LAr hadronic end-cap calorimeter (HEC) provides coverage over $1.5 < |\eta| < 3.21$. The forward regions ($3.2 < |\eta| < 4.9$) are instrumented with LAr calorimeters for both electromagnetic and hadronic measurements (FCals).

All studies performed so far indicate that the ATLAS calorimeters will continue to function at highest peak luminosities and over the integrated luminosities expected at HL-LHC. Studies are on-going to assess the performance of the forward calorimeters. Depending on the outcome of these studies it might be necessary to replace the FCal with a higher granularity calorimeter (the so-called sFCal) or to install a small calorimeter just in front of the FCal (the MiniFCal), to reduce the particle flux on it.

As explained in the previous section, the LAr front-end electronics, housed in front-end boards (FEBs) located outside the calorimeter cryostats will need to be replaced. The analog part of the HEC front-end electronics, which is located inside the end-cap cryostats,is in a relatively high radiation region. Intensive studies have shown that this electronics will operate with negligible deterioration at HL-LHC conditions, so that it does not need to be replaced. Finally, depending on the technological choices made for the forward calorimeter, new radiation hard electronics might need to be installed in the forward region.

A full replacement of the readout electronics of the hadronic tile calorimeter (which is housed in so-called "drawers") is also foreseen.

3.1 Tile calorimeter

The current front-end electronics is installed in 256 drawers that need to be replaced to implement a free-running design with 40 MHz digitization. The main front-end components, a mixed analog/digital main board, need to be replaced. Three alternative developments are under study: an evolution of today's 3-in-1 discrete card, that comprises shaper, 2-gain amplifier and 3-gain integrator for Cs calibration; a solution based on the FERMILAB QIE10 ASIC; a new ASIC development using 130 nm IBM process, which includes a 3 gain shaper and a 12-bit pipeline ADC.

On daughter boards, Kintex-7 FPGA and CERN GBTx are being studied for data transmission to the back-end. The transfer rate is 625 Gbps per Board and 20 Tbps in total. The back end, on FPGA-based full custom ATCA blade design, performs signal extraction, bunch-crossing identification for trigger, pipeline buffer, TTC signal distribution. One TileCal drawer is planned to be equipped with a full demonstrator front-end and back-end system to validate the new architecture and compare the different solutions proposed.

3.2 Liquid Argon calorimeter

To send all LAr calorimeter data off detector for triggering and for read-out at LHC bunch-crossing frequency of 40 MHz (for a total bandwidth of 140 Tbps), all FEBs and RODs need to replace with newer generation versions. The Phase-I new trigger boards (LTDB) [4] will stay to provide a Level-0 low latency trigger.

A new pre-amplifier and shaper will be integrated into a single ASIC; a low noise, 16-bit dynamic range amplifier, followed by low power differential shaping stage has been realized using Silicon-Germanium (SiGe) BiCMOS technology. A prototype has been produced using IBM 8WL 0.13 μm process; a cheaper process (IHP) will also be tried.

The choice of a new ADC will be also based on the studies performed for Phase 1 and will evaluate custom and commercial components. A custom 12-bit ADC, realized in IBM 8RF 130nm CMOS, with low power (30-50 mW/channel), low latency (<90 ns) and radiation tolerance (12

kGy, 3.3x10^{14} n_{eq}/cm^2, 6.3x10^{13} h/cm^2) has been designed. Among the COTS solutions, a 12-bit Texas Instruments ADC (ADS5272) performed best.

For data transfer a Link-on-chip (LOC) development in Silicon-on-Sapphire (SoS) 0.25 μm technology is being pursued; it has custom interface and serializer and will use VCSEL devices from Versatile Link for conversion to optical signal. This technology should allow a 8 Gbps design; Phase-II requires 12$\times$10 Gbps VCSEL arrays: this calls for an improved SoS process or a next-generation GBTx.

The data are received by the back-end using serial optical links on multi-fiber ribbons. The conversion to electronic signal will be performed by commercial components and de-serialization will be handled by fast FPGA transceivers. Data will be processed by high-bandwidth ATCA Pre-Processor boards. They will handle 1.2 Tbps input from front-end and send 250 Gbps trigger information to Level-0. Algorithms to be implemented include energy reconstruction, bunch-crossing identification, pipeline, trigger sums or more complex algorithms, like the extraction of EM shower shapes. These back-end solutions are already being studied for Phase I and will evolve into a Phase II design.

4. CMS

CMS makes use of a lead tungstate crystal electromagnetic calorimeter (ECAL) and of a brass/scintillator hadron calorimeter (HCAL), covering the region $|\eta| <3$. The ECAL barrel extends to $|\eta| <1.48$ while the ECAL endcaps cover the region $1.48< |\eta| <3.0$. A steel/quartz-fibre Cherenkov forward calorimeter extends the calorimetric coverage up to $|\eta| <5.0$.

The barrel ECAL and HCAL plan to replace the present electronic. In the ECAL both the digital (FE) and analog (VFE) parts will be replaced. In HCAL, probably already in Phase 1, there will be new electronics, making use of SiPM and new read out.

Extrapolation of the calorimeter performance to Phase II conditions, have shown that in the endcap region, the ECAL and HCAL will not be able to operate successfully. The plan is to replace them with new calorimeters, possibly with a different technology. This will of course imply a new electronics.

4.1 HCAL

In the HCAL, Silicon Photomultipliers (SiPM) will replace the present Hybrid Photon Detectors (HPD). A QIE10 chip will be used for charge integration and encoding. After processing by a radiation tolerant FPGA, data will be sent to back end via GBTx/Versatile Links. Preprocessing and event building will be done in μTCA modules.

4.2 ECAL

The plan for the barrel part of the ECAL is to remove all 36 supermodules and to replace the front-end cards and their services. In the new front end all crystal sums for the Level 1 trigger will be removed; all buffers will be also removed, and the data will be sent out at 40 MHz. CERN GBTx/Versatile link will be used both for data transfer to back end and for control: 10 Gbps rad-tolerant links will be needed. The new back end will be an evolution of the MP7 μTCA board, based on a Xilinx Virtex 7 FPGA, as developed for Phase 1 trigger.

In addition to the replacement of the digital part of the front-end, a replacement also of the VFE part of the front-end, which includes a charge preamplifier, a shaper and an ADC, is also being considered. The upgrade would mitigate the spikes in the APD due to interactions with hadrons (coming from primary interactions and backsplashes) causing anomalous high-energy deposits (around 1 spike per event is expected at HL-LHC); moreover it would also reduce the noise due to the increase in the APD leakage current due to neutron damage and from in-time and out-of-time pile-up. A lower shaping time would mitigate all these effects. An upgrade of the VFE would also imply an upgrade of the low-voltage regulator board to provide the required new voltages. In this case, an effort would be also done to reduce the power dissipation with respect to the present regulators. Studies are also on-going to investigate the possibility to redesign the cooling system to cool the ECAL barrel to 8-10 $^{\circ}$C to mitigate the APD radiation-induced dark current noise.

5. Conclusions

Goal of all LHC calorimeter electronic developments is to meet the challenging pile-up and radiation requirements and to ensure longevity of the systems throughout Phase II. A large program of R&D is on-going to identify the needed technical solutions. Although the difference in the calorimeter systems of the experiments limits the possibility of synergies, there are areas in which common development paths for on-detector and off-detector electronics are possible. This includes the qualification of radiation tolerant commercial components (ADCs, FGPAs,...); the qualification of custom devices, (like e.g. the QIE10 chip explored by both ATLAS and CMS); the implementation of the CERN GBTx/Versatile Link protocol (although a 10 Gbps radiation tolerant version is needed by ATLAS LAr and CMS ECAL); development and testing of distributed powering components (POL regulators,...); the development of FPGA-based ATCA or μTCA processing boards (and alternatively of PCIe FPGA boards).

References

[1] The ATLAS Collaboration, *The ATLAS Experiment at the CERN Large Hadron Collider*, *JINST* **3** (2008) S08003.

[2] The CMS Collaboration, *The CMS Experiment at the CERN LHC*, *JINST* **3** (2008) S08004.

[3] The ATLAS Collaboration, *Letter of Intent for the Phase-II Upgrade of the ATLAS Experiment*, CERN-LHCC-2012-022; LHCC-I-023.

[4] The ATLAS Collaboration, *ATLAS Liquid Argon Calorimeter Phase-I Upgrade Technical Design Report*, CERN-LHCC-2013-017; ATLAS-TDR-022-2013.