

Upgrade of the ALICE Inner Tracking System

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During the Long Shutdown 2 of the LHC in 2018/2019, the ALICE experiment plans the installation of a novel Inner Tracking System. It will replace the current six layer detector system with a seven layer detector using Monolithic Active Pixel Sensors. The upgraded Inner Tracking System will have significantly improved tracking and vertexing capabilities, as well as readout rate to cope with the expected increased Pb-Pb luminosity of the LHC. The choice of Monolithic Active Pixel Sensors has been driven by the specific requirements of ALICE as a heavy ion experiment dealing with rare processes at low transverse momenta. This leads to stringent requirements on the material budget of 0.3 % X/X_0 per layer for the three innermost layers. Furthermore, the detector will see large hit densities of $\sim 19 \text{ cm}^{-2}$ /event on average for minimum-bias events in the inner most layer and has to stand a moderate maximum total ionising dose of 700 krad and a non-ionising energy loss of $1 \times 10^{13} \text{ MeV}_{\text{neq}}/\text{cm}^2$. The Monolithic Active Pixel Sensor detectors are manufactured using the TowerJazz 0.18 μm CMOS Imaging Sensor process on wafers with a high-resistivity epitaxial layer.

This contribution summarises the recent R&D activities and focuses on results on the large-scale pixel sensor prototypes.

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1. Introduction

ALICE (A Large Ion Collider Experiment) [1] is a general-purpose, heavy-ion experiment at the CERN LHC. Its main goal is to study the physics properties of the Quark-Gluon Plasma. During the Long Shutdown 2 (LS2) of the LHC in 2018/2019, ALICE will undergo a major upgrade in order to significantly enhance its physics capabilities, in particular for high precision measurements of rare processes at low transverse momenta p_T .

1.1 ALICE Upgrade

The ALICE upgrade programme [2] during LS2 is based on a combination of detector upgrades improving their physics performance and preparing them for a significant luminosity increase to $L = 6 \times 10^{27} \text{ cm}^{-2}\text{s}^{-1}$ for nucleus-nucleus (A-A) collisions. The increased luminosity will lead to a Pb-Pb interaction rate of about 50 kHz. The study of rare probes at low p_T in heavy-ion collisions makes triggering inefficient due to the large combinatorial background [3]. Thus, the upgraded experimental apparatus is designed to readout all Pb-Pb interactions, accumulating events corresponding to an integrated luminosity of more than 10 nb^{-1} . This minimum-bias data sample will provide an increase in statistics by about a factor 100 with respect to the programme until LS2. The upgraded detector will provide improved vertexing and tracking capabilities at low p_T . In summary, the detector upgrade consists of the following sub-system upgrades:

- Reduction of the beam-pipe radius from 29.8 mm to 19.8 mm allowing the inner layer of the central barrel silicon tracker to be moved closer to the interaction point.
- New high-resolution, high-granularity, low material budget silicon trackers:
 - Inner Tracking System (ITS) [4] covering mid-pseudo-rapidity ($-1.2 < \eta < 1.2$).
 - Muon Forward Tracker (MFT) [5] covering forward pseudo-rapidity ($-3.6 < \eta < 2.45$).
- The wire chambers of the Time Projection Chamber (TPC) will be replaced by GEM detectors and new electronics will be installed in order to allow for a continuous readout [6].
- Upgrade of the forward trigger detectors and the Zero Degree Calorimeter [7].
- Upgrade of the readout electronics of the Transition Radiation Detector (TRD), Time-Of-Flight (TOF) detector, PHOTon Spectrometer (PHOS) and Muon Spectrometer for high rate operation [7].
- Upgrade of online and offline systems (O² project) [2] in order to cope with the expected data volume.

2. ALICE ITS Upgrade

The main goals of the ITS upgrade are to achieve an improved reconstruction of the primary vertex as well as decay vertices originating from heavy-flavour hadrons and an improved performance for the detection of low- p_T particles. The design objectives are to improve the impact

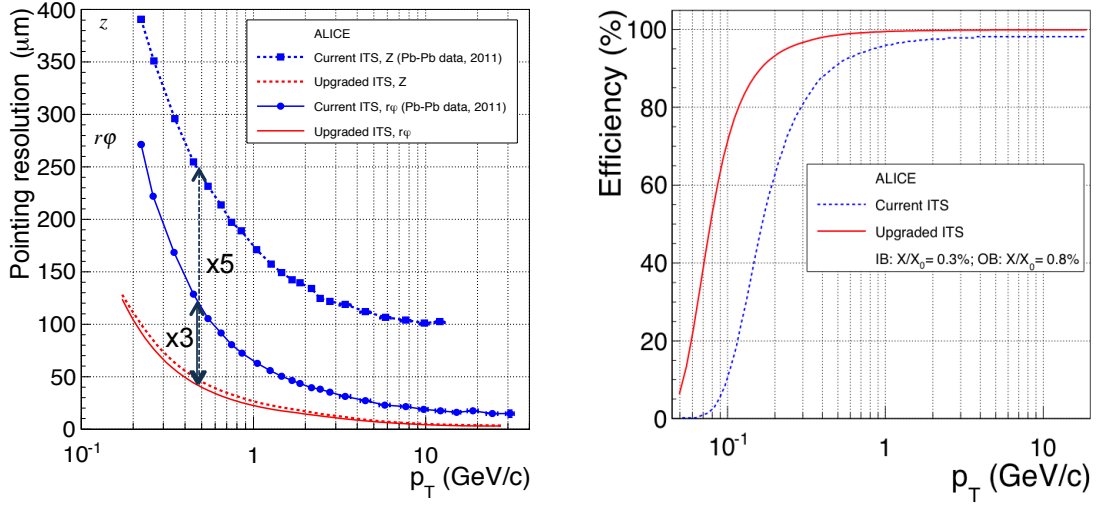


Figure 1: Simulated pointing resolution (left) and tracking efficiency (right) of the upgraded ITS, taken from [4].

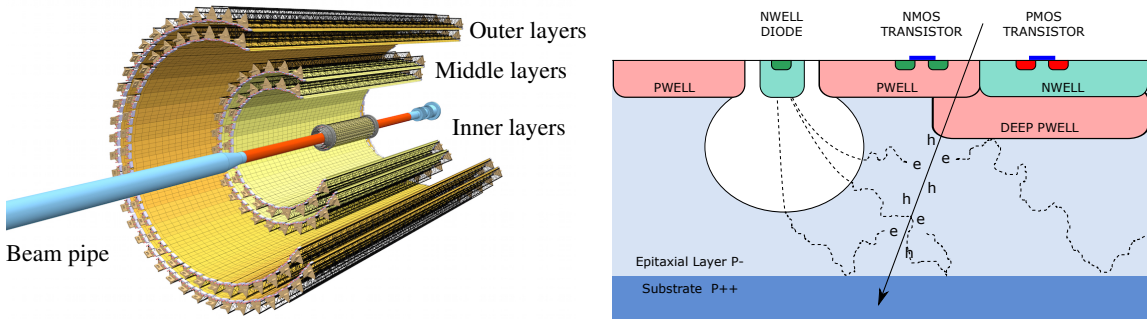


Figure 2: Layout of the upgraded ITS (left) and schematic cross section of a pixel of a monolithic silicon pixel sensor using the TowerJazz CMOS Imaging process (right), both taken from [4].

parameter resolution by a factor of 3 and 5 in the $r\phi$ and z coordinate, respectively, at a p_T of 500 MeV/c. Furthermore, the tracking efficiency and the p_T resolution at low p_T will improve. Corresponding Monte-Carlo simulations are shown in Fig. 1. Additionally, the readout rate will be increased to 50 kHz in Pb-Pb and 400 kHz in pp collisions. In order to achieve this the following measures will be taken. The innermost detector layer will be moved closer to the interaction point from 39 mm to 22 mm. The material budget will be reduced down to 0.3 % X/X_0 per layer for the innermost layers while for the outer layers will be about 0.9 % X/X_0 . In addition the granularity will be increased by an additional seventh layer and by shrinking the pixel size from currently $50\mu\text{m} \times 425\mu\text{m}$ to $O(30\mu\text{m} \times 30\mu\text{m})$. All layers of the upgraded ITS will be equipped with pixel sensors. The upgraded ITS is designed such as to allow easy removal and insertion during the yearly shutdown periods.

2.1 Layout and Running Environment of the Upgraded ITS

The upgraded ITS, as shown in Fig. 2, will have seven layers which are grouped into the

Table 1: General pixel-chip requirements [4].

Parameter	Inner Barrel	Outer Barrel
Chip dimensions	15 mm × 30 mm ($r\phi \times z$)	
Sensor thickness	50 μm	
Spatial resolution	5 μm	10 μm
Detection efficiency	> 99 %	
Fake hit rate	$< 10^{-5} \text{ event}^{-1} \text{ pixel}^{-1}$	
Integration time	< 30 μs	
Power density	$< 300 \text{ mW/cm}^2$	$< 100 \text{ mW/cm}^2$
Temperature	20 °C to 30 °C	
TID radiation hardness ^a	700 krad	10 krad
NIEL radiation hardness ^a	$1 \times 10^{13} \text{ 1 MeV n}_{\text{eq}}/\text{cm}^2$	$3 \times 10^{10} \text{ 1 MeV n}_{\text{eq}}/\text{cm}^2$

^aThese values include a safety factor of ten.

Inner Barrel, containing the innermost three layers, and the Outer Barrel containing the middle two and the outer two layers. The radii the layers are 22 mm, 31 mm and 39 mm and 194 mm, 247 mm, 353 mm and 405 mm, respectively. Although the requirements on the pixel chips are slightly different for the Inner Barrel and Outer Barrel, we aim to deploy the same chip on all seven layers (cf. Tab. 1). The upgraded ITS will provide pseudo-rapidity coverage of $|\eta| < 1.22$ for 90 % of the most luminous beam interaction region. The radial positions of the layers were optimised in order to achieve the best combined performance in terms of pointing resolution, p_T resolution and tracking efficiency in Pb-Pb collisions at hit densities of about $19 \text{ cm}^{-2}/\text{event}$ on average for minimum-bias events in the innermost layer. The detector will cover a total surface of 10.3 m^2 containing about 12.5×10^9 pixels with binary readout. The upgraded ITS will be operated at room temperature (20 °C to 30 °C) using water cooling. The expected radiation load at the innermost layer is expected to be 700 krad of Total Ionising Dose (TID) and $1 \times 10^{13} \text{ 1 MeV n}_{\text{eq}}/\text{cm}^2$ of Non-Ionising Energy Loss (NIEL) including a safety factor of ten. In order to meet the material budget requirements the silicon sensors will be thinned down to 50 μm .

2.2 Choice of Pixel Chip Technology

Summarising the considerations above, the upgraded ITS will have very thin sensors, very high granularity and will cover a fairly large area. Furthermore, the radiation levels are only moderate compared to the other LHC experiments. In the past decade there has been a lot of progress on Monolithic Active Pixels Sensors (MAPS), which can now be considered for the construction of tracking systems in high-energy physics experiments. MAPS allow for very thin sensors, as a single die is used as detection volume and for the readout electronics. Additionally, no bump bonding or similar interconnection of detection and readout chip are needed, and this interconnection usually limits cost and pixel density. The ULTIMATE chip of the STAR PXL detector [8] at RHIC is the first successfully running, large-scale application. However, further R&D is required to meet the much more stringent requirements of the ITS upgrade compared to the STAR experiment in terms of integration time, power consumption and radiation hardness.

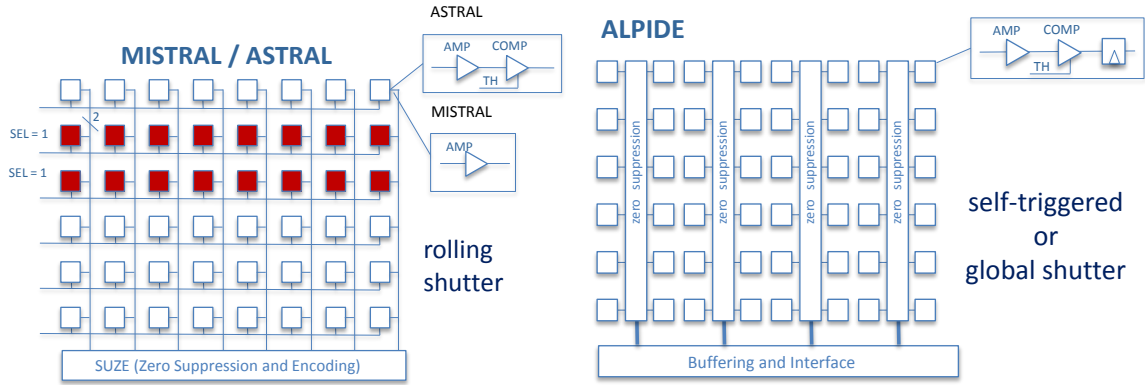


Figure 3: Sketch of the architectures deployed in the ASTRAL (left) and MISTRAL (right) design stream.

2.3 Pixel Chip Development

The sensors of upgraded ITS will be manufactured using the 0.18 μm CMOS Imaging Sensor process by TowerJazz [9]. This process provides up to six metal layers allowing for a high-density, low-power circuitry. Furthermore, the gate oxide thickness of about 3 nm provides a sufficient TID radiation tolerance. This has already been confirmed in measurements on basic transistor structures [10]. The key feature of the process, however, is the special deep p-well. As shown in Fig. 2, the n-wells of PMOS transistors are housed in additional p-wells, preventing the transistor n-wells from competing with the n-well of the collection electrode for charge collection. Hence, full CMOS logic can be used within the matrix and as consequence, more complex in-pixel circuitry is possible. An epitaxial layer with high resistivity ($\sim \text{k}\Omega\text{cm}$) serves as active volume. In order to increase the depletion volume and to optimise the charge-collection efficiency, a moderate reverse substrate bias can be applied. This is essential to increase the output signal of the collection n-well which is proportional to $\sim Q/C$. In order to achieve a high signal, the charge collected by the central pixel needs to be increased. Furthermore, the capacitance of the pixel needs to be minimised by shrinking the diode surface and increasing the depletion volume which is supported by additional reverse substrate bias. Achieving a good Q/C -ratio leads to an improved signal-to-noise ratio and as a consequence also to a less power consuming design of the circuitry.

2.4 Pixel Chip Architecture

Currently, two R&D design streams are under development, called ASTRAL and ALPIDE (cf. Fig. 3). The ASTRAL chip is based on a rolling-shutter architecture, where rows of pixels are read simultaneously and the integration time is defined by the time the shutter needs to return to the same row. ASTRAL contains in-pixel discriminators and end-of-column sparsification called SUZE. This architecture is based on the ULTIMATE chip developed for the STAR PXL detector. The MISTRAL is a variant of ASTRAL having end-of-column discriminators, resulting in a simpler in-pixel circuitry but a higher power density.

On the other hand ALPIDE operates in a global shutter mode. The shutter can either be started by an external trigger signal or be kept continuously open. In continuous-integration mode the shutter is only closed to advance to the next event. The chip features in-pixel discrimination

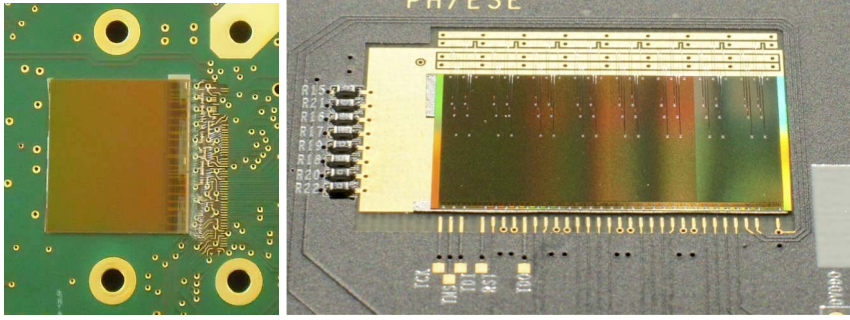


Figure 4: Two FSBB-M0 chips arranged in a column (left) and pALPIDEfs chip (right).

and in-pixel hit buffers. These buffers allow to acquire consecutive events while the readout of the previous event is still ongoing. Furthermore, a priority encoder is used to achieve in-matrix sparsification. Only pixels containing hits are propagated to the end-of-column further reducing the power-consumption and the area necessary for the peripheral logic.

After the successful development and characterisation of small-scale prototypes, large-scale prototypes, close to the final chip dimensions, of both ASTRAL and ALPIDE architectures are currently being characterised.

2.5 ASTRAL/MISTRAL Prototypes

The FSBB-M0 (cf. Fig. 4) is a Full-Scale Building Block of the MISTRAL design stream. Three FSBBs form a full chip. The FSBB-M0 chip features 416×416 pixels of $22\mu\text{m} \times 33\mu\text{m}$ which are read out by double-row end-of-column discriminators. The integration time of this prototype is $40\mu\text{s}$. The FSBB-A0 is an implementation of the ASTRAL version of the FSBB achieving $20\mu\text{s}$ integration time deploying in-pixel discrimination. A total of 25 FSBB-M0 have been extensively characterised in the laboratory, showing similar noise performance. The corresponding transfer function for the variation of the discriminator threshold is shown in Fig. 5. A Temporal Noise (TN), the time-like threshold dispersion, of 0.87 mV and the Fixed Pattern Noise (FPN), the

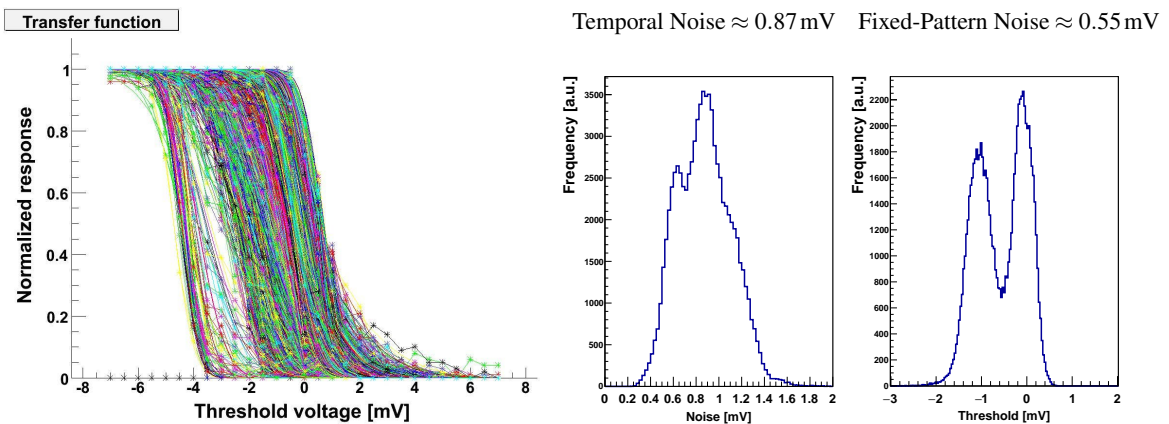


Figure 5: Discriminator transfer function (left), Temporal Noise distribution (centre) and Fixed Pattern Noise (right) of an example FSBB-M0.

Table 2: pALPIDEfs pixel properties.

Sector	n-well diameter	Spacing	p-well opening	Reset
0	2 μm	1 μm	4 μm	PMOS
1	2 μm	2 μm	6 μm	PMOS
2	2 μm	2 μm	6 μm	Diode
3	2 μm	4 μm	10 μm	PMOS

spatial spread of the pixel threshold, of 0.55 mV were achieved. The double-peak structures are due to cross-coupling. Further tests at the CERN SPS are planned for the near future.

2.6 pALPIDEfs - a Full-Scale Prototype of the ALPIDE

The pALPIDEfs is a full-scale prototype of the ALPIDE family (cf. Fig. 4) with a dimension of 30 mm \times 15 mm containing about 5×10^5 pixels of 28 $\mu\text{m} \times 28 \mu\text{m}$. The power consumption per pixel front-end is 40 nW leading to a power density of 4.7 mW/cm². In order to increase the depletion volume, a reverse substrate bias can be applied to this chip. In its current version, four sectors containing different design options are implemented and in particular, several diode geometries with different sizes of p-well openings and reset mechanisms, namely PMOS resets and diode resets as outlined in Tab. 2. The pALPIDEfs features in-matrix sparsification based on a priority encoder. The target power density for future prototypes of this family excluding off-chip data transmission is about 30 mW/cm².

The pALPIDEfs has been characterised in the laboratory as well as in test beam. The following results were obtained using a telescope of 6 or 7 pALPIDEfs at the CERN PS using a 6 GeV pion beam. The first results on detection efficiency and noise are shown in Fig. 6 (left). A detection efficiency of 99 % at a fake-hit rate of 10^{-5} was measured. The results were obtained having only

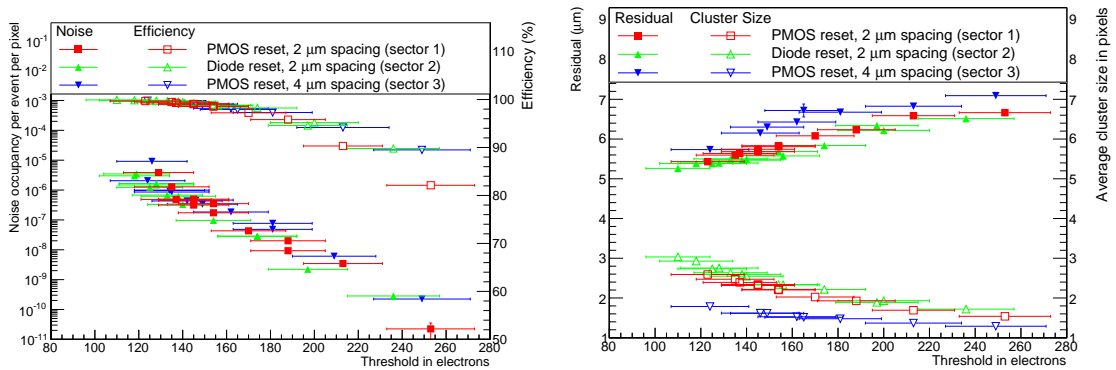


Figure 6: Detection efficiency (open symbols) and noise (full symbols) of the pALPIDEfs (left) and uncorrected position resolution (full symbols) as well as cluster size (open symbols) of the pALPIDEfs (right), both without the application of reverse substrate bias. The sectors 1, 2, and 3 are drawn with red, green and blue symbols, respectively.

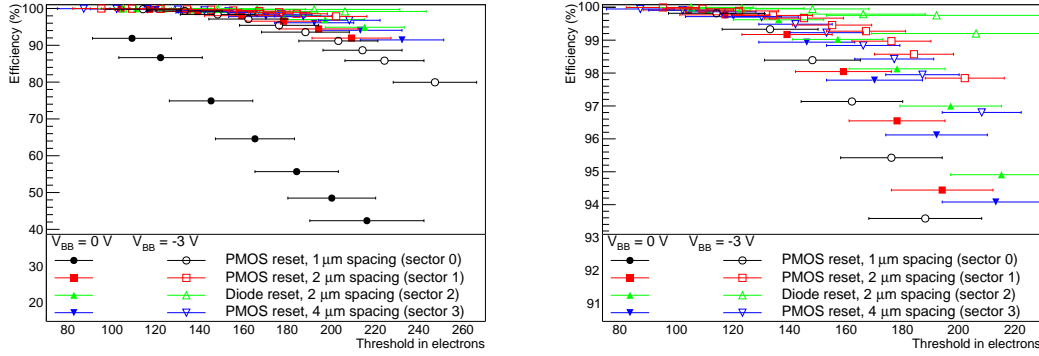


Figure 7: Influence of reverse substrate bias on the detection efficiency of the pALPIDEs (left) and zoomed view (right). Open symbols are with a reverse substrate bias of $V_{BB} = -3$ V and full symbols without reverse substrate bias. The sectors 0, 1, 2, and 3 are drawn with black, red, green and blue symbols, respectively.

20 pixels masked. The position resolution has been measured and the corresponding residuals and the cluster size are shown in Fig. 6 (right). This measurement still includes a tracking error of about $3 \mu\text{m}$ leading nevertheless to an uncorrected spatial resolution of about $5.5 \mu\text{m}$. In Fig. 6, sector 0 has been excluded. This sector reaches a detection efficiency of above 99 % only using reverse substrate bias as shown in Fig. 7. Also the other sectors gain margin using reverse substrate bias, allowing for higher thresholds maintaining detection efficiencies above 99 %. All results confirm the positive effect of a larger spacing on the detection performance. This can most likely be attributed to an increase depleted volume due to decreased side-wall capacitance. Furthermore, pixels with diode reset as in sector 2 perform better than the pixels with PMOS reset.

3. Mechanics and Assembly

As mentioned above, the upgraded ITS consists of an Inner Barrel (IB) and an Outer Barrel (OB). The basic element of a layer is the stave, which consists of a carbon space frame to which the cold plate and the cooling ducts are attached. Above the cold plate a number of pixel chips, 9 for the IB and 14 for the OB, connected to a common Flexible Printed Circuit (FPC) are glued (cf. Fig. 8, left). The FPC consists of a polyimide with a low thermal expansion coefficient plus aluminium and copper as conductor for the IB and OB, respectively. The chip will be connected to the FPC using laser soldering, allowing a distribution of the connection pads over the entire chip surface rather than its periphery. This has been successfully prototyped and is working on pALPIDEs chips. The staves of the IB will have a length of 270 mm. The staves of the middle and outer two layers of the OB will be 843 mm and 1475 mm long. In order to improve the pointing resolution, the material budget of the inner layers will not exceed 0.3 % X/X_0 on average per layer. The material budget will be higher in the regions of stave overlap and cooling pipes (cf. Fig. 8, right).

For the OB and its wider and longer staves further segmentations are introduced. An OB stave consists of two half-staves. The half-staves of the same stave as well as the half-staves of adjacent staves are overlapping in order to minimise the dead area. The material budget is 0.9 % X/X_0 per layer.

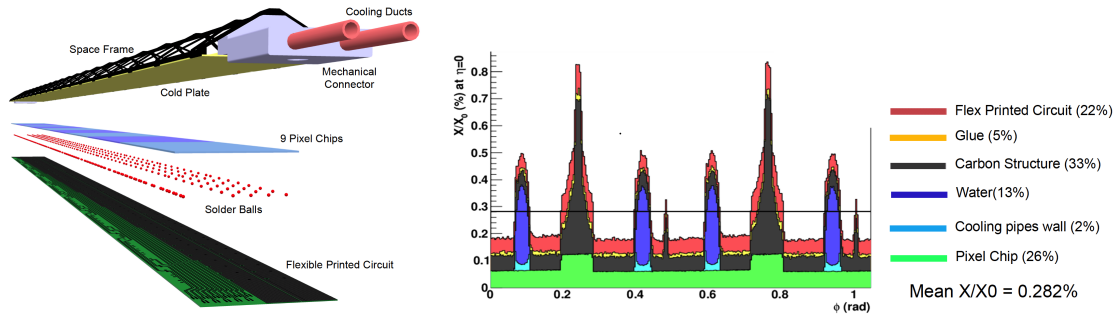


Figure 8: Material budget distribution of the inner barrel (left), exploded schematic view of an inner barrel stave (right).

First prototypes of the IB and OB mechanics have been assembled and have been successfully characterised for their mechanical strength and thermal properties [4].

4. Summary and Outlook

ALICE will replace the entire ITS by a MAPS-based, pixel-only tracker in 2019. This upgrade will significantly improve impact-parameter resolution and increase readout-rate capabilities. Moreover, better tracking efficiency and p_T resolution at low p_T will be achieved. For the pixel sensor R&D, large-scale prototypes of two separate design architectures are currently being characterised and have shown satisfactory results. The mechanical structures have been prototyped and successfully tested. Also the novel laser soldering to establish the connection between the pixel chips and the flexible printed circuit has been successfully applied to working prototype chips. Further close-to-final design prototypes will be tested in the near future and assembled in staves in order to prepare the mass production.

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