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The CMS Pixel Detector Phase-1 Upgrade

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The CMS experiment is going to upgrade its pixel detector during Run 2 of the Large Hadron Collider. The new detector will provide an additional tracking layer and increased rate capability, suitable for the projected instantaneous luminosities of Run 2, well beyond the original design targets of the present pixel detector.

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1. Overview

The present pixel detector of the CMS experiment [1, 2] has performed very well during Run 1 of the Large Hadron Collider (LHC). Point resolutions of 9.4 μm in $r-\phi$, 20–45 μm in z with high detection efficiency have been achieved [3]. The pixel detector plays a key role in tracking, vertexing and the high level trigger of the CMS experiment. It has been designed to tolerate the radiation damage corresponding to an integrated luminosity of 500 fb^{-1}, and data rates corresponding to an instantaneous luminosity of 10^{34} cm^{-2}s^{-1}. The LHC has reached almost 0.8×10^{34}cm^{-2}s^{-1} during Run 1, and due to the operation with 50 ns bunch spacing, the number of inelastic proton-proton collisions per bunch crossing (pile-up) has already been higher than the original design goal of 25.

Current planning foresees reaching 2.5×10^{34} cm^{-2}s^{-1}, corresponding to 70 pile-up events at 25 ns bunch spacing, before a high luminosity upgrade of the LHC and CMS. This significantly exceeds the rate capability of the present readout Chip (ROC) and data links. The "phase 1" upgrade of the CMS pixel detector should maintain or improve the performance of the present pixel detector in the presence of such high instantaneous luminosities until the end of Run 2.

The phase 1 pixel detector is an evolutionary upgrade based on the successful present pixel detector. The core of the detector is unchanged: pixel size and sensor design, analog front-end, and readout architecture. The required performance improvements are achieved by improving the rate capability of the readout, an additional tracking layer for robust pattern recognition in high pile-up conditions, and an optimized material budget. Many of the existing services, such as optical fibers and power cables, can not be replaced and will be re-used for the upgrade.

1.1 Detector layout

Like the present pixel detecor, the upgrade layout (Figure 1) has a cylindrical barrel section (BPIX) with an active length of 50 cm (pseudorapidity $|\eta|<1.5$)[1], and disks in the forward region (FPIX), covering the pseudorapidity $1.5<|\eta|<2.5$. The barrel layers are located at radii of 30 mm, 68 mm, 109 mm, and 160 mm. The innermost layer is almost 13 mm closer to the beam spot than the first layer of the present detector. This has become possible with the reduction of the outer radius of the CMS central beam pipe from 30 mm to 22.5 mm. The radii of layers 2 and 3 are basically unchanged with respect to the present detector. A 4$^{\text{th}}$ layer at a radius of 160 mm has been added to the barrel layout, which reduces the radial gap between pixel and strip detectors.

While the present forward pixel disks are constructed from wedge shaped detector panels, the phase 1 FPIX is built with modules that have the same rectangular geometry as the barrel part. Three disks are located on each side of the interaction region at distances of 29.1 cm, 39.6 cm, and 51.6 cm. They are sensitive in the radial region between 4.5 cm and 16.1 cm. FPIX and BPIX together provide four hit coverage up to pseudorapdity ±2.5, matching the acceptance of the outer Silicon Strip tracker of CMS.

The pixel size is 150 μm $\times$ 100 μm and pulse-height information is used for interpolating hit positions. Modules have an active area of 6.4 cm $\times$ 1.6 cm with two rows of ROCs bump-bonded to the n-type silicon sensor. The full detector has 123 million pixels in 1856 modules, an increase of almost a factor 1.9 with respect to the current detector.

[1]The CMS coordinate system has the origin at the nominal collision point and the z-axis along the counterclockwise beam direction. The pseudorapidity corresponding to an angle θ with respect to the positive z-axis is $\eta=-\ln(\tan\theta/2)$.

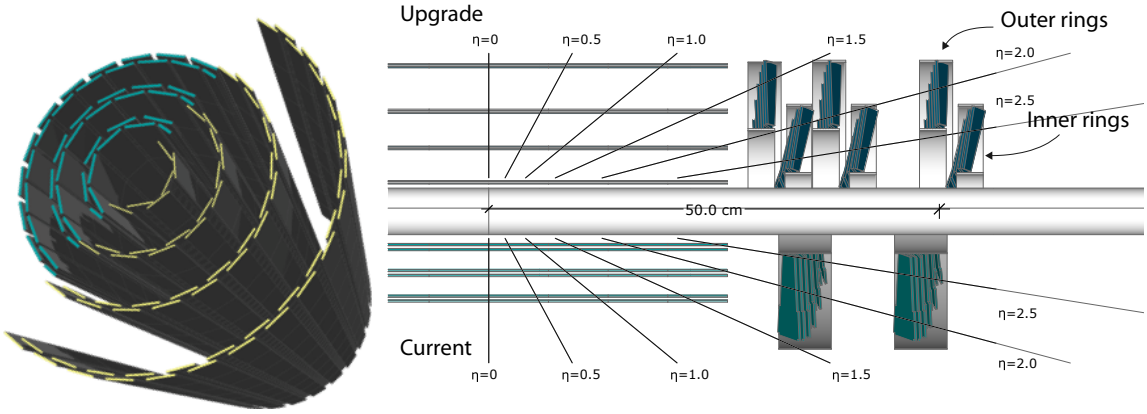

Figure 1: Layout comparison of the present CMS pixel detector and the phase 1 upgrade. The BPIX detector (left) has a reduced inner radius and an additional 4$^{\text{th}}$ layer at a radius of 160 mm. The FPIX detector has three disks per side, each disk consisting of two rings made of rectangular modules (right).

Despite the increased number of layers, the material budget of the pixel detector in the central region is almost unchanged. This is achieved mainly by moving the module connector point from the barrel endflange out to the service cylinder, far enough from the interaction region to affect only pseudorapidities $|\eta| > 2$, and a new low-mass cooling. With improved readout, the additional tracking layer, and the optimized material distribution, it will be possible to have tracking efficiencies that are comparable or better than the present detector in the higher luminosities expected near the end of the LHC Run 2 [4].

2. Readout Electronics

The readout chip and data links of the CMS pixel detector were built for hit rates of a few tens of MHz/cm^2 encountered for an instantaneous luminosity of 10^{34} cm^{2}s^{-1} with a bunch spacing of 25 ns. During the trigger latency of the CMS experiment, currently 4 μs, the pixel hit data must be stored inside the readout chip and only data corresponding to triggered events can be read out through serial optical links. The bandwith of the analog links of the present detector will be saturated at 2×10^{34} cm^{2}s^{-1}. Readout losses occur even before this point due to the statistical fluctuations of the data volume. The internal transfer- and buffer-capacity of the readout chip are designed for similar rates.

Since sensor type and pixel dimensions are unchanged, and the overall performance of the readout chip is excellent, the readout chip for the upgraded detector is derived from the present ROC, and keeps most of its characteristics: pulse-height readout, 52x80 pixels organized in 26 double columns of 2x80 pixels with common data transfer to latency buffers in the periphery outside of the active pixel region. The upgrade ROC [5] is manufactured in the same 0.25 μm CMOS technology, the overall layout and many building blocks are unchanged (Figure 2). The two main improvements needed for the upgrade are larger data buffers and higher detector readout speed. The buffer sizes have been increased from 32 (12) hits (time-stamps) per double column to 80 (24). The readout speed of the ROC itself is unchanged, but the transition from 40 MHz analog coded data to 160 MHz digital data allows faster readout of the modules. The module controller chip

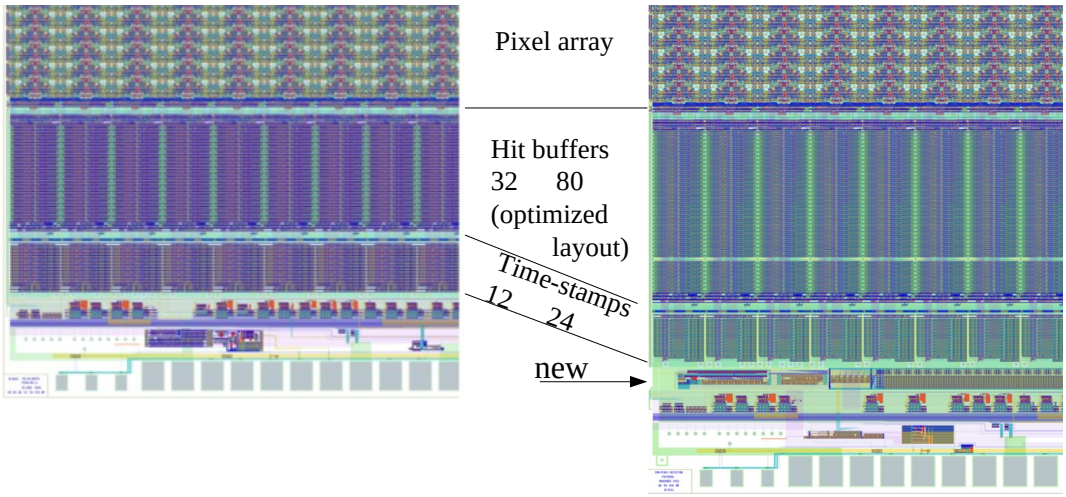

Figure 2: Layout detail of the CMS pixel ROCs for the present detector (left) and the phase 1 upgrade (right). Only a corner of the ROC is shown with 5 rows and 8 double columns of pixels. The pixel matrix is essentially unchanged. The main differences are in the enlarged latency buffers and additional blocks for the digital readout: pulse-height ADC, 160 MHz PLL, digital readout buffer. The digital readout chip is 0.4 mm longer which increases the module width.

multiplexes groups of ROCs onto 320 MHz links (400 MHz after 4b/5b-encoding), doubling the capacity per optical fiber [6]. The existing optical fibers for the present detector are re-used for the upgrade. By adding spares and laying new fibers, the total number of links is increased from 1312 to 2368. The number of links per module varies from one in the outer layers to four in the innermost layer, which will have a four times higher readout bandwidth than the present innermost layer with two analog links.

In addition to the higher rate capacity of the ROC, small improvements have been achieved in several important details. Using an additional metal layer for power distribution allowed better decoupling and pixel response uniformity. An optimized comparator minimizes time-walk and the effective operational threshold of the chip can be reduced from 3200 electrons in the present detector to below 2000 electrons for the upgrade. This will become important when the amount of charge per hit starts to decrease after radiation damage to the sensors. A highly irradiated detector will slowly degrade resolution and eventually become a binary detector. With a lower threshold the charge sharing among neighbouring pixels can be exploited longer for position interpolation.

Based on operational experience with the existing ROC and irradiation tests, further optimizations of internal biasing were made that extend the range of ionizing dose tolerable by the ROCs and reduce the need to re-adjust DACs with increasing accumulated dose.

The digital readout chips performed without problems after irradiation up to 120 MRad (4×10^{14} p/cm^2, 24 MeV, at the Karlsruhe Cyclotron), the maximal dose expected for the phase 1 upgrade. With some limitations the ROCs were operational up to 480 MRad. Data-losses have been measured with high-rate X-ray tubes for pixel hit rates up to 250 MHz/cm^2 and were found to be in excellent agreement with expectations based on detailed architecture simulations. Based on the same simulation fed with proton-proton collision data, the data losses in FPIX and BPIX layer

2-4 will be less than 2 %. This version of the readout chip is now in production.

A modified version of this readout chip is under development for the innermost BPIX layer, where pixel hit rates up to 600 MHz cm^{-2} may be encountered. This requires faster hit transfer from pixels to end-of-column buffers and dead-time-free buffer management. The majority of the modules for the phase 1 pixel detector is going to be assembled in 2015. The 96 modules of layer 1 represent 8 % of BPIX and will be built towards the end of module production.

3. Power and Cooling

With the additional layer, the number of pixels increases by a factor 1.9 with respect to the present detector. Furthermore, the power consumption will increase with rising hit rates. The foreseen installation in the middle of Run 2 does not allow installing a new set of the 40-50 m long power cables connecting the inner detector with the power supplies in the collision hall. More efficient use of the existing cables can be made with DC-DC converters near the front-end electronics and a higher supply voltage at the output of the power supplies. A solution based on the radiation hard FEAST2 ASIC [7] has been developed for the CMS pixel upgrade [8]. Converter modules on the service cylinders produce 3.0 V and 2.4 V from an input voltage of 10 V with 80% power efficiency. Voltage drops on the remaining 2 m between converter and pixel modules reduce this to the operating voltages of 2.4 V (digital) and 1.7 V(analog). Each converter can provide up to 3 A of current, 1184 modules are needed for the full detector. The power supplies of the present detector can be re-used after small modifications. The total power dissipated by the detector, including auxiliary electronics, detector leakage currents and ohmic cable losses, can be up to 9 kW.

A bi-phase CO_2 cooling system, replacing the present C_6F_{14} cooling, can remove the increased heat load using a minimal amount of material in the sensitive detector volume. It allows coolant temperatures of -20°C and lower, which is required to keep the leakage current of the silicon layers below the maximum permitted by the high voltage supplies and to prevent thermal runaway after particle fluences of 2×10^{15} $n_{eq}cm^{-2}$. Thin stainless steel tubes with 1.6 mm inner diameter and 0.05 mm wall thickness cool the modules in the central region where material minimization is crucial. The same cooling loops, with a wall thickness of 0.1 mm and diameter of 2.2 mm, run in the service cylinders. The heat load of the auxiliary electronics brings the liquid CO_2 arriving at the detector end-flange to the boiling point and ensures efficient evaporative cooling of the detectors. Vacuum jacketed coaxial tubes connecting the inner detector volume with the cooling plant have been installed during the 2014 shutdown. A cooling plant prototype has been built and operated successfully. Detailed verification of the cooling loop design is ongoing.

4. Mechanics and Insertion

Similar to the present detector, the cooling tubes form the backbone of the BPIX support structure. Each cooling loop goes through several sectors and is connected to the service cylinder at the radius of the service cylinders. The resulting complicated tube shapes are manufactured with a combination of 3d-bending and brazing. A prototype tube system is shown in Figure 3. In the detector, tubes are held in place by endrings made of foam/carbon fiber sandwiches and carbon fiber blades glued onto the tubes. Modules are held on the carbon fiber blades by 0.5 mm

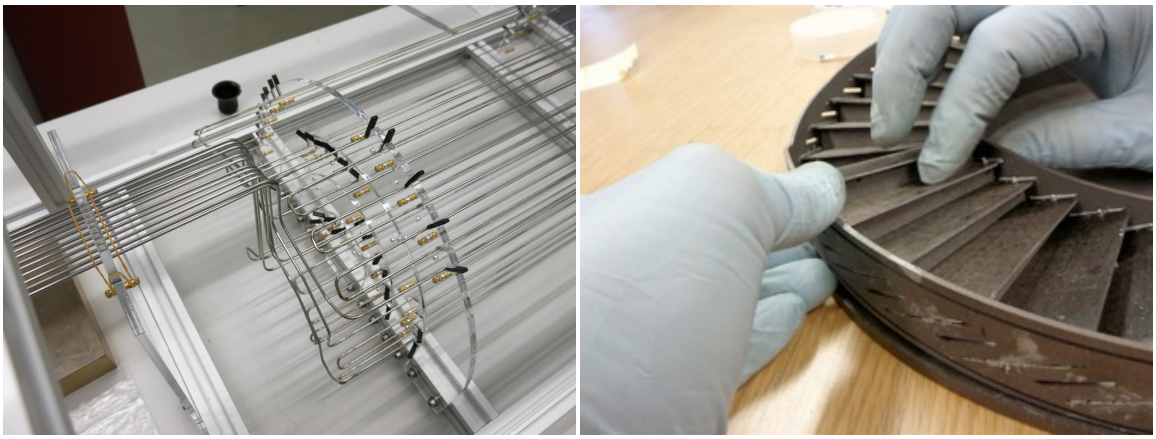

Figure 3: Photographs of the BPIX (left) and FPIX (right) mechanics prototype assembly. The BPIX cooling loops are shown on a temporary fixture without carbon fiber blades. The FPIX cooling tubes (not shown) are mounted in grooves of the rings connecting the TPG blades holding modules.

diameter screws. For better thermal heat transfer between the detector modules and the cooling tubes, high thermal conductivity carbon fiber material is used for the blades and the tubes are glued onto shallow grooves machined into the blades. This is essential for keeping the silicon temperature below -5° C.

In the FPIX detector with its turbine-like geometry, the cooling loops are not running directly underneath the modules. Instead, the modules are mounted on heat spreaders made out of thermal pyrolytic graphite (TPG), that efficiently bring the heat to the cooling pipes embedded in the rings that hold the blades (figure 3). Cooling loops are embedded in the ring material.

The pixel detector of the CMS experiment is installed into a cylindrical volume with a diameter of 40 cm and a length of 6 m. The presence of the beam-pipe of the LHC in the center of this volume with vertical support wires requires the pixel detector to be vertically divided. The BPIX system, including service cylinders at the $+z$ and $-z$–sides, is inserted from one end of CMS. Afterwards the four FPIX half-cylinders are inserted from both ends of CMS. The insertions are guided by grooves in bottom and top of the installation volume. The grooves are not straight, reflecting the varying beam-pipe and flange diameters along the path from the insertion region to the interaction point. The installation volume of the phase 1 detector is identical to that of the present detector and the installation procedure very similar. However, installation clearances as low as 3 mm arise as a consequence of the small radius of the first BPIX layer. A safe installation is only achievable with adjustable wheels that permit insertion with larger clearances. Only after the barrel has reached the final z-position, the half-shells are moved inward horizontally by 6 mm using remote operation tools. Wheels and procedure have been verified in the CMS detector during the shutdown in 2014.

5. Pilot System

The upgrade detector is scheduled for installation during a so-called technical stop of 4-5 months in the middle of Run 2. This leaves minimal time to integrate the new detector into CMS operation before the LHC resumes delivering high luminosity. It is therefore mandatory to avoid

disruptions of data-taking and to fully integrate the phase 1 detector into CMS data acquisition and detector control system as early as possible. To allow this integration, a pilot system is installed during the shutdown in 2014 and will be operated during the first part of Run 2 in parallel with the present pixel detector. The current FPIX has room and services for three disks, but only two disks have been built and installed. For the pilot system, 8 modules of the phase 1 detector have been mounted in the position of the third disk together with the corresponding auxiliary electronics and digital readout. Half of the pilot system is powered conventionally, the other half with DC-DC converters. All components are close to the final versions.

6. Summary and Outlook

The present pixel detector of the CMS experiment is likely to reach its rate limits during Run 2 of the LHC. An upgrade based on improvements of the present design, with higher rate capability and an extra tracking layer, is under construction. A readout chip has been developed with lower thresholds, improved buffering and digital readout. The 400 Mbit/s transmission doubles the bandwidth available per optical link. A powering system based on DC-DC converters permits continuing the use of the already installed power cables for a detector that grows by a factor 1.9. A new CO_2 cooling helps keeping the material budget low and provides low operating temperatures needed for operating silicon detector after radiation damage.

All components are in production or their final prototyping stage. Module assembly will start in 2015 and the detector will be ready for installation in a technical stop of the LHC starting at the end of 2016. The smaller diameter beam-pipe, new transfer lines for the CO_2 cooling and the pilot system have already been installed in the shutdown preceding Run 2. The pilot system will exercise operation of the upgrade pixel detector in CMS to prepare the transition in 2017.

Acknowledgments

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