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Initial Characteristics and Radiation Damage Compensation of Double Silicon-on-Insulator Pixel Device

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We are developing monolithic pixel devices based on 0.2-μm fully depleted silicon-on-insulator (FD-SOI) technology utilizing bonded wafers, where the silicon resistivities for the sensor and electronics parts are optimized separately. Application of the device for high-energy physics experiments is under investigation. The major concern for adoption in high-radiation environments is the total ionization dose (TID) damage caused by the accumulation of holes in the oxide layers. We have developed double SOI (DSOI) wafers, where an independent silicon layer is added underneath the buried oxide layer. The negative potential applied to this second silicon layer should compensate for the effects due to accumulated holes. The effectiveness of the compensation is characterized in detail using dedicated devices, TrTEGs, consisting of various types of individual FETs. The devices were irradiated with ^{60}Co γ up to 2 MGy. A general integration-type pixel sensor is also examined to evaluate the overall pre-irradiation and post-irradiation performance

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1. Introduction

Silicon-on-insulator (SOI) devices, where electronics circuits are built on a layered insulator, possess various unique features such as a small leakage current, fast response, immunity against single-event effects, and a wide range of operation temperatures. These characteristics are the results of a reduced parasitic capacitance and small active area realized in the SOI structure, where each FET[1] is entirely enclosed in SiO_2. In thin-silicon-layer devices, the silicon layer is fully depleted (FD-SOI) and the characteristics are further enhanced.

We have adopted the 0.2-μm FD-SOI technology of Lapis Semiconductor [1] for pixel-sensor fabrication, where the SOI "handle wafer" is employed as the sensor. The original idea of SOI application for realizing sensors was proposed at the beginning of the 1990s [2], followed by sensor developments [3] [4] employing SIMOX[2] SOI wafers. In contrast to SIMOX wafers where the wafer resistivity is unique along the thickness, we employ SOI wafers produced using Soitec SmartCut^{TM}technology [5], where two silicon wafers are mated with SiO_2 acting as a bonding layer. The technological features in our pixel-sensor development are based on this method, where the wafer resistivity can be optimized for the CMOS circuit and sensor parts individually.

Our SOI pixel development started in 2005 as one of the projects operated under the KEK Detector Technology Project [6]. Since then, developmental research has been carried out in cooperation with Lapis Semiconductor Co., Ltd.(formerly OKI Semiconductor). The process and wafer are briefly summarized in Table 1. The characteristics and history of high-resistivity wafer availability are also listed. The default SOI wafers use the Czochralski (Cz) growth process for superior mechanical stability. By default, n-type wafers with a high resistivity of 700 Ω cm are fabricated. To extend applications, we succeeded in the adoption of float zone (FZ) wafers to enable the selection of n- and p-type wafers with an even higher resistivity. With this success, a fully depleted sensor as thick as 700 μm was realized, which is indispensable for hard X-ray detection.

Table 2 lists the selected pixel devices currently under development in Japan [7]. The top

Table 1: Summary of the Lapis process and SOI wafer characteristics.

Process	0.2-μm low-leakage fully depleted SOI CMOS 1 poly + 5 metal layers (MIM capacitor and DMOS option) total thickness above top Si (SOI layer) $\sim$9 μm core voltage: 1.8 V, I/O voltage: 3.3 V
SOI wafer (200 mmϕ)	top Si: Cz 18 Ωcm, p-type, 40 nm buried oxide: 200 nm thick handle wafer thickness: 725 μm $\rightarrow$ thinned to 300 μm by Lapis SOI-Cz n-type (0.70 kΩ cm), as default SOI-FZ n-type ($>$3 kΩ cm), available since 2009 SOI-FZ p-type (25 kΩ cm), available since 2010 DSOI-Cz n-type (0.7 kΩ cm), available since 2012

[1] Field-Effect Transistor

[2] Separation by IMplantation of OXygen

group sensors, INTPIX to TDIPIX, are charge-integration-type sensors where the signal charge is digitized with ADCs located in the peripheral region or outside the chip. In the second group chips, CNTPIX and PIXOR, the signal is digitized on the pixel. Among these, PIXOR is being developed for the future Belle-II experiment at KEK, where signals in a 16×16 pixel array are summed into 16 rows and 16 columns in order to reduce the number of output lines while maintaining the original spatial resolution. STJSOI and MALPIX make use of the superior SOI CMOS performance. STJSOI, for example, has demonstrated that the CMOS FETs are operational at a temperature as low as 0.7 K.[8]

Since 2013, development research has been funded as a Grant-in-Aid Project of Japanese KAKENHI, an aid for Scientific Research in Innovative Areas. Many other devices are currently under development for applications in various fields covering high-energy physics, X-ray astronomy, materials science, medical applications, and nondestructive inspection.

The first major issue in pixel sensor design was the back-gate effect, e.g., the sensor bias applied to the back affects the operation of the CMOS circuit. This has been solved by implementing a buried p-well (BPW) for a p-type pixel node, which acts as an electrical shield [10]. The BPW design needs to be carefully optimized, because the shape of the BPW determines the detector capacitance, and therefore the pulse height.

The second issue is the total ionization dose (TID) damage [14]. Under irradiation, holes created in the oxide are trapped, whereas mobile electrons can escape, resulting in a positively charged insulator and negative shift in the threshold voltage [15]. Because each element is entirely enclosed in the nearby insulator, the effect of charge built-up is substantial. Evaluation of TID damage in single SOI devices has been reported previously [16],[17],[18].

In this paper, we report the initial evaluation results of the double SOI (DSOI) pixel sensor and present an understanding of the TID damage including TID damage compensation using the DSOI feature.

Table 2: Selected devices under development in Japan. Most of the devices have square pixels, as listed in the comment column, except for PIXOR.

name	brief description (designed by)	comment	ref
INTPIX	General Purpose Integration Type (KEK)	8–20 μm	[9] [10]
SOPHIAS	Large Area and High Dynamic Range for XFEL (RIKEN)	30 μm	[11]
XRPIX	X-ray Astronomy in Satellite (Kyoto U, KEK)	30 μm	[12]
LHDPIX	Nuclear Fusion Plasma X-ray (KEK, NIFS)	24 μm	
TDIPIX	Time Delaying Integration for X-ray Inspection (KEK)	12 μm	
CNTPIX	General Purpose Counting Type (KEK)	64 μm	
PIXOR	Future Belle II Vertex Detector (Tohoku U.)	35×70 μm	[13]
STJPIX	Superconducting Tunnel Junction on SOI (U. Tsukuba)	below 1 K	[8]
MALPIX	TOF Imaging Mass Spectrometer (KEK, Osaka U.)	ΔT = 1 ns	

2. TID Damage Compensation in DSOI Devices

The TID damage in DSOI devices was evaluated using dedicated TEGs (Test Element Group), where various types of NMOS and PMOS FETs were implemented so that the I–V characteristics of individual devices available in the Lapis process can be evaluated. The FETs [19] are for core and I/O types; low-, normal- and high-thresholds types; source-tie (ST; two types available) and body-tie (BT) connections together with body floating (BF); and with various W/L settings.

The TEGs were irradiated with ^{60}Co γ for a dose range from 2 kGy to 2 MGy. The irradiation took place at room temperature at dose rates of 1 kGy/h to 10 kGy/h. All terminals were grounded during irradiation. No intentional annealing was performed: the irradiated samples were kept refrigerated.

Figure 1 shows the I–V curves of NMOS and PMOS FETs irradiated to 2 MGy and the transitions when negative voltages (V_{SOI2}) were applied to the second silicon layer, measured at $V_{DS} = 1.8\,V$. The curves are compared with the pre-irradiation curves. As is evident, we can find an appropriate V_{SOI2} to compensate the threshold voltage back to the pre-irradiation value, but the transconductance g_m and subthreshold swing S behaviors are not restored to the original values.

Figure 2 presents the optimum V_{SOI2} voltages for all measured FETs, where the threshold voltage is restored to the pre-irradiation value. The tendency is that the optimum V_{SOI2} decreases

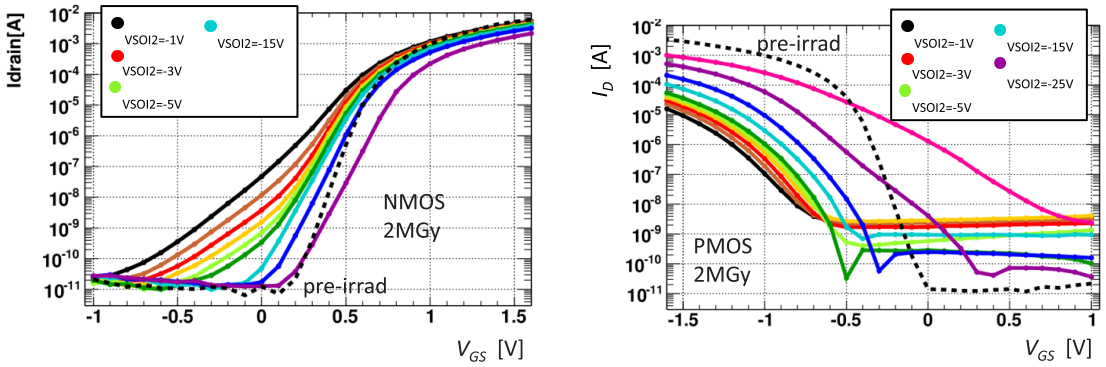

Figure 1: I–V curves of (left) NMOS and (right) PMOS FETs irradiated to 2 MGy. The curves are for various V_{SOI2} settings, compared with the one for pre-irradiation (dashed curve).

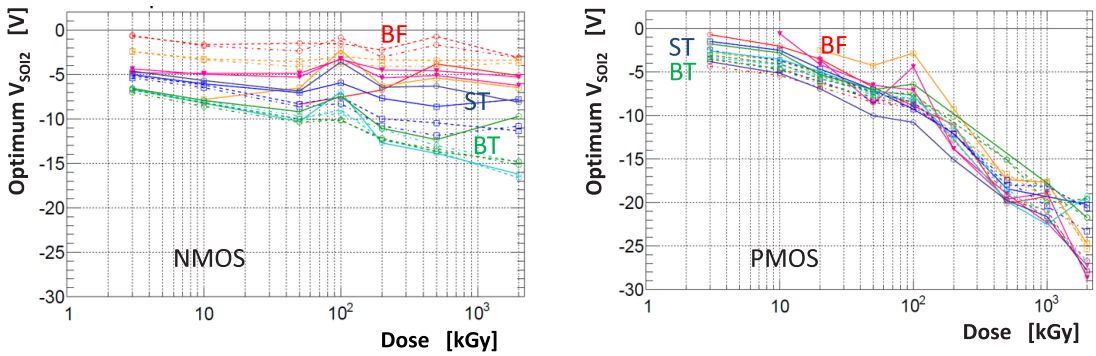

Figure 2: V_{SOI2} to compensate for the threshold-voltage shift as function of the dose. Data are shown for various (left) NMOS and (right) PMOS FETs.

(the absolute values increase) with the dose monotonically only for the PMOS. However, the saturation for the NMOS is caused by an effect known as ”rebound” [20]. Some spreads in the V_{SOI2} values are observed among the different FET types, noticeably for the NMOS FETs. The main contribution to the spread is due to the different body-connection scheme.

Although the threshold shifts can be compensated if V_{SOI2} is set to the individual optimum value, it is practically preferred if we have a couple of different V_{SOI2} lines applied to specific FETs, which exhibit similar threshold shifts.

Figure 3 shows the deviations in the threshold voltages from pre-irradiation for an example compensation scheme in which the FETs are grouped into body-tie, source-tie, and no body connection for the NMOS FETs and with or without body connection for the PMOS FETs. Furthermore, a common V_{SOI2} is applied for each group. The residual deviations in the threshold shifts are found to be mostly within 0.05 V. Depending on the application, further threshold tuning would be required, which would be substantially easier after the large shifts are mostly compensated, as shown.

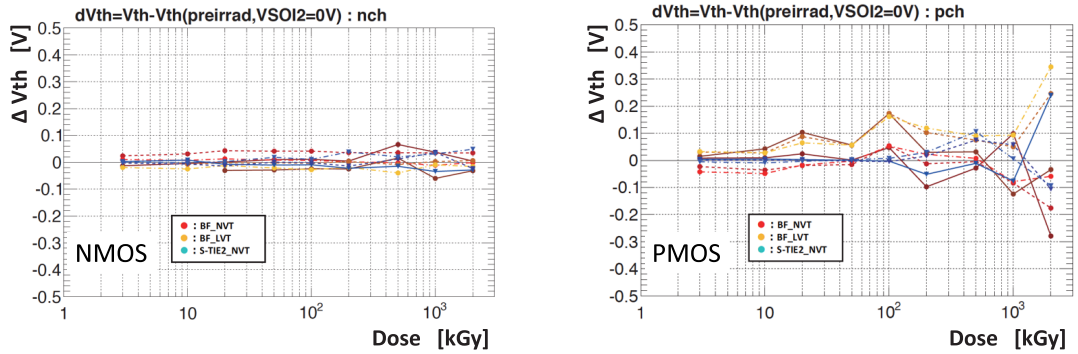

Figure 3: Residual threshold-voltage shifts of all tested FETs for (left) NMOS and (right) PMOS FETs, where a simple compensation scheme is applied (see text).

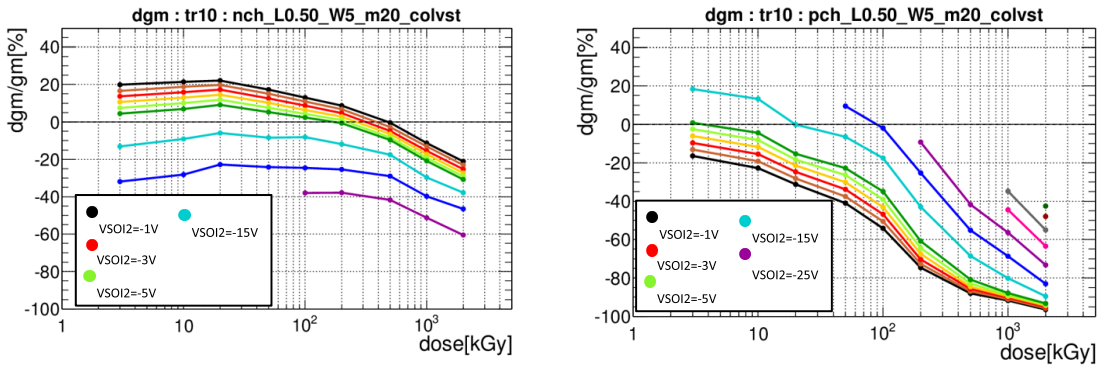

Figure 4: Percent shift in the transconductance of typical (left) NMOS and (right) PMOS FETs as function of the dose. Curves are for different V_{SOI2} settings.

The percent shift in g_m is plotted in Fig. 4 for typical FETs as a function of the dose for various V_{SOI2} values. The holes accumulated in the oxide promote (depress) the creation of an inversion

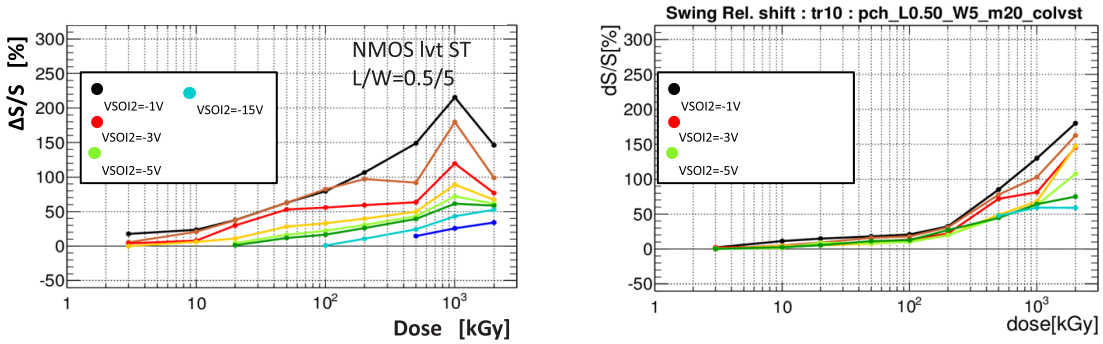

Figure 5: Percent shift in the subthreshold swing of typical (left) NMOS and (right) PMOS FETs as function of the dose. Curves are for different V_{SOI2} settings.

layer the in NMOS (PMOS) FETs, increasing (decreasing) g_m as the dose is accumulated. Applying a negative V_{SOI2} works oppositely, decreasing g_m in the NMOS FETs and increasing g_m in the PMOS FETs.

The percent shift in S is plotted in Fig. 5 for typical FETs as a function of the dose for various V_{SOI2} values. S is affected by the leakage current and is degraded with the dose for both NMOS and PMOS FETs.

The degradation in the transconductance should be directly linked to that in the carrier mobility. The mobility is evaluated from the I_d–V_{GS} curve measured at $V_{DS} = 0.1$ V (linear region) using the following relation:

$$I_D = \mu_{\rm eff} C_{\rm OX} \frac{W}{L} \{(V_{GS} - V_T)V_{DS} - \frac{1}{2}V_{DS}^2\}, \tag{2.1}$$

where $C_{\rm OX}$ is the gate oxide capacitance calculated using thicknesses of 4.5 nm for the core and 7 nm for the I/O FETs. The effect of the mobility degradation [21] due to the existence of gate field is further taken into account in the formula:

$$\mu_0 = \frac{\mu_{\rm eff}}{1 + \theta(V_{GS} - V_T)}, \tag{2.2}$$

where θ is an empirical positive constant. In practice, we calculated the mobility as a function of V_{GS} and, because the above function gives a smaller $\mu_{\rm eff}$ with V_{GS} whereas the mobility in the subthreshold region increases with V_{GS}, we determined μ_0 as the maximum mobility value in the dependence. The obtained μ_0 is plotted in Fig. 6. The data points are not shown for the PMOS FETs at the highest doses because the maximum in the μ_0–dose curve is not obtained; the threshold is too low, reaching below V_D.

3. Characteristic Evaluation of the DSOI Pixel Sensor

We have evaluated the characteristics of the DSOI pixel sensor using an INTh2 device, which

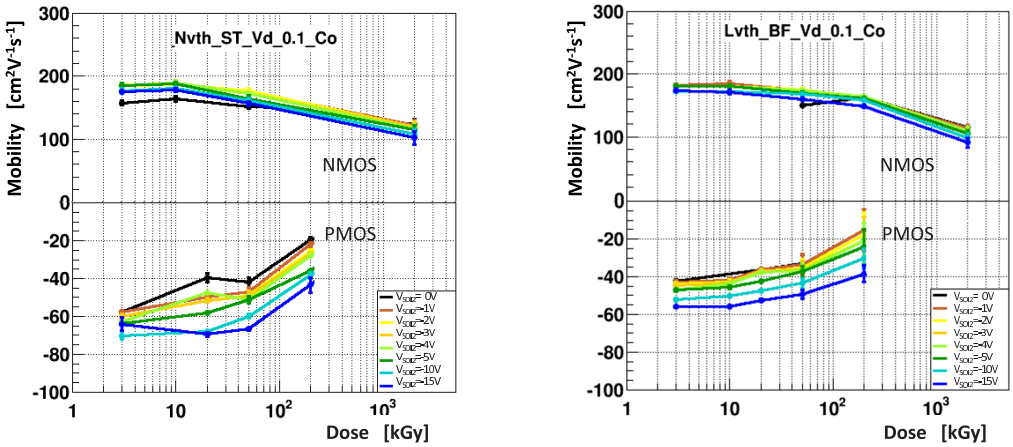

Figure 6: Mobility of typical (left: normal threshold, source tie and right: low threshold, body floating) NMOS and PMOS FETs as function of the dose. The negative data are for the PMOS FETs. Curves are for different V_{SOI2} settings.

is an active-pixel-type sensor with pixels 18 μm $\times$ 18 μm square. The diagram of the on-pixel circuit is shown in Fig. 7. The analog signal selected by the column–row addresses is extracted out of the INTh2 chip and then digitized by a 12-bit ADC on a SEABAS data acquisition board [22]. The INTh2 device has a single V_{SOI2} control common to all pixels. The characteristic evaluation was carried out by testing the electronics functionality by changing the reset voltage V_RST (see Fig. 7) to the input stage and by testing the entire sensor functionality by injecting a 1024-nm infrared pulse laser [23]. The laser with this wavelength penetrates the silicon mostly, and in some cases, liberates energy almost uniformly along its path, thus simulating the passage of high-energy charged tracks. The time profile of the laser was measured with a fast photodevice, resulting a peaking time of 15 ns with a decaying tail extending further by 40 ns.

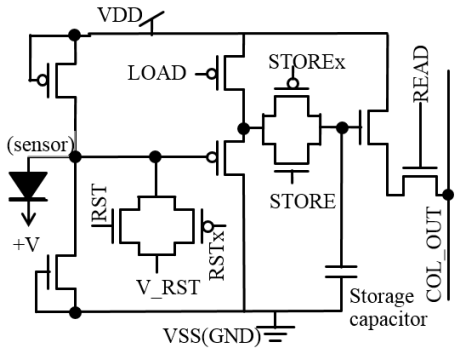

Figure 7: On-pixel circuit diagram of the INTh2 device. The reset voltage V_RST is used to test the functionality of the circuit.

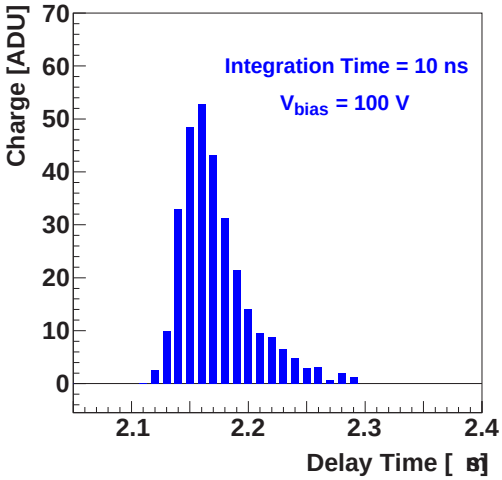

Figure 8: Time structure of the signal measured at the ADC. The delay time was scanned with the integration time set at 10 ns.

3.1 Thinned INTh2 Device

The pixel devices processed by Lapis were further thinned down to 107 μm by Nihon Exceed Co.[24] For a handle-wafer resistivity of 700 kΩ cm, the sensor is fully depleted at a bias of 50 V. No further processing, e.g., aluminization, was applied to the backside so that the laser was injected from the backside.

Figure 8 shows the time structure of the analog signal measured at the ADC. The signal was integrated for 10 ns by changing the delay time with respect to the trigger for laser emission. The time profile is typically extended for 150 ns.

Crosstalk was evaluated by injecting the laser at the center of one of the pixels (pixel number 195, see Fig. 9). The laser spot was typically 4 μm $\times$ 4 μm . The crosstalk depends on the bias voltage and integration time. The crosstalk in a fully depleted sensor is noticeably small with little dependence on the integration time.

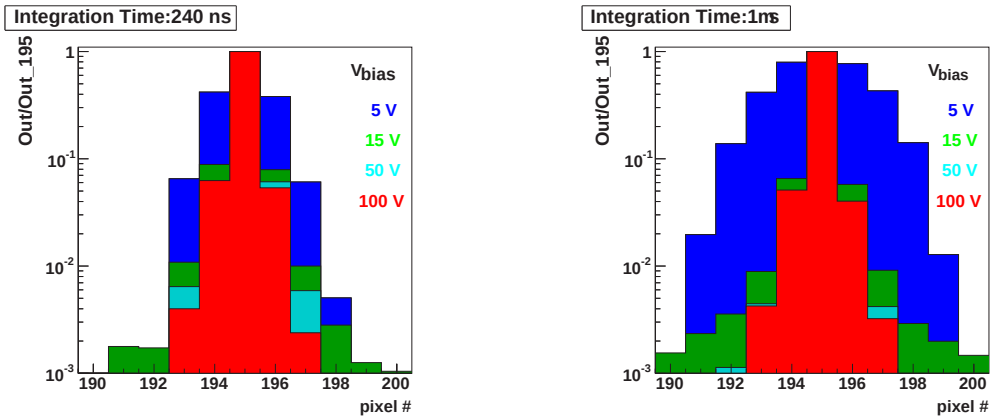

Figure 9: Crosstalk to neighboring channels when the laser was injected at the center of pixel 195. The data are shown for two integration time settings, 240 ns and 1 μs, at bias voltages of 5, 15, 50, and 100 V.

3.2 Irradiated INTh2 Device

The DSOI sensor of 300 μm thickness was irradiated to 100 kGy with Co γ, and the performance was evaluated.

The functionality of the CMOS electronics was measured from the response to a change in the V_RST voltage. As shown in Fig. 10, although the responsible range affected should be narrow because of the irradiation, applying V_{SOI2} enlarges the range. The responsible range was not observed at $V_{SOI2} = 0$.

The response of irradiated sensor was tested with the IR laser injected from the top side. Because the tested device was 300 μm thick, the response is expected to increase linearly as a function of the square-root of the bias voltage. As shown in Fig. 11, the response is found to follow the expected trend. The linearity is compared with the non-irradiated device, where the V_RST voltages to define the pedestals were optimized for both samples, as they are different, as evident in Fig. 10. Although there is a difference in the offset values, the irradiated sensor also exhibits a linear response over a wide range.

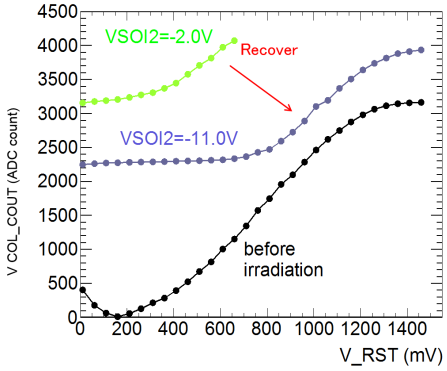

Figure 10: Response of the INTh2 sensor irradiated to 100 kGy. The electronics functionality is measured as a function of the reset voltage. With $V_{SOI2} = 0$, the responsible range is barely observed, whereas the range increases with increasing V_{SOI2}. The curves are compared with the pre-irradiation response.

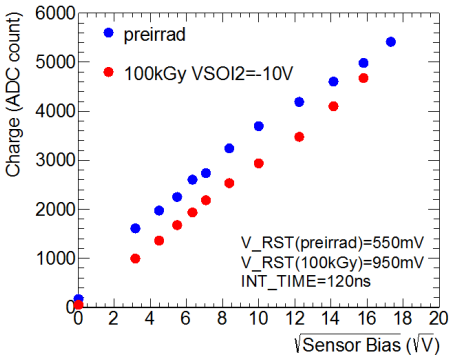

Figure 11: The response curve to the IR laser as function of the square root of the bias voltage, compared with the pre-irradiation curve. The response increases with the bias because the full depletion voltage is approximately 400 V for this device of 300 μm thickness.

4. Summary

We have evaluated the TID damage in SOI devices and the TID compensation in DSOI devices. The threshold-voltage shifts can be compensated mostly up to 2 MGy. Because the degree of the threshold shifts is different between NMOS and PMOS FETs and among different body-connection schemes, separate optimization is preferred.

The transconductance and subthreshold swing are also degraded. They are not fully recoverable by V_{SOI2} adjustment, notably above 100 kGy. The degradation in the transconductance, for example, is explained by the degradation in the mobility.

Fast signal collection and small crosstalk are demonstrated in the DSOI device. Taking these advantages and the TID compensation into account, the DSOI devices can be regarded as suitable for future ILC experiments [25] in which the annual dose is expected to be approximately 1 kGy/year.

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