PROCEEDINGS OF SCIENCE

Three Dimensional Integrated Circuits Bonded to Sensors

L. Altman[3], G. Carini[6], G. Deptuch[5], F Fahim[5], P. Grybos[1], U. Heintz[3], J. Hoff[5], S. Holm[5], R. Lipton*[5], P. Maj[1], M. Narain[3], C. Neher[7], S. Poprocki[4], A. Shenai[5], P. Siddons[2], R. Syarif[3], R. Szczygiel[1], J.Thom[4], M. Trimpl[5], M. Tripathi[7], P. Wittich[4], R. Yarema[5], Z. Ye[8], T. Zimmerman[5]

[1] *AGH, Krakow*
[2] *Brookhaven National Laboratory*
[3] *Brown University*
[4] *Cornell University*
[5] *Fermilab*
[6] *SLAC National Accelerator Laboratory*
[7] *University of California, Davis*
[8] *University of Illinois, Chicago*

E-mail: lipton@fnal.gov

We report on the processing and performance of 3D integrated circuits (3DIC) bonded to silicon sensors. The circuits were part of the Fermilab-sponsored two-tier 0.13 micron run at Tezzaron and Global Foundries. They include designs for the CMS track trigger, ILC vertex detectors, and x-ray correlation spectroscopy. Sensors were bonded to the 3DICs using die-to-die solder ball bonding as well as a chip-to-wafer oxide bonding process (Ziptronix DBI®) similar to the wafer-to-wafer bonding process used for the 3DICs.

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*Speaker.

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1. 3D Circuit Technology

Three dimensional electronics are a set of technologies being developed to stack multiple layers of silicon wafers and interconnect them vertically [1] [2]. These technologies are being pursued by the electronics industry as an alternative to the increasing cost and technical challenges posed by device scaling. 3D technology promises shorter, lower capacitance interconnects, smaller footprint, heterogeneous integration, and higher bandwidth. Fabrication of a 3DIC requires wafer thinning and bonding, Through Silicon Via (TSV) interconnect, precise alignment, and wafer to wafer interconnect. For particle physics these technologies can provide high density, low capacitance (low power) interconnection to pixelated detectors.

In particle physics we care about bonding sensors to complex analog/digital electronics. 3D enables intimate interconnection between sensors and readout circuits, unique functionality with innovative circuit/sensor topologies, separate digital, analog and data communication tiers, and multi-layer micro/macro pixel designs which can provide high resolution with minimal circuitry. Wafer thinning enables low mass, high resolution sensors. Bonding technologies enable very fine pitch, high resolution pixelated devices. It also provides the possibility for unique circuit and sensor geometries to address problems such as forming triggers based on tracks at Level 1 at CMS.

2. Processes and Designs

A number of techniques have been developed for the basic 3D technologies of wafer bonding (themocompression, adhesive, oxide) and via insertion (first, middle, or last). We have been exploring and evaluating candidate technologies commercially available in small volume or R&D facilitaties. Our initial work on 3D utilized the MIT-Lincoln Laboratory process based on 0.18 micron silicon-on-insulator technology [3]. We then began to explore commercial approaches based on copper-copper thermocompression from Tezzaron [4] and Direct Oxide bonding (DBI ®) from Ziptronix [5]. The devices discussed in this paper utilize the oxide bonding-based DBI® process with TSV wafers fabricated by Tezzaron.

The oxide bonding process utilizes pairs of wafers with deposited silicon dioxide surfaces. These surfaces, when planarized by chemical mechanical polishing and chemically activated, will bond spontaneously on contact. The initial weak Van-Der Walls bonds can be made permanent by thermal processing. The DBI® process combines oxide bonding with imbedded metal: the imbedded metal layers are compressed during thermal processing due to the difference in thermal expansion between the metal and SiO_2, resulting in an electrical bond between layers. The resulting stacks for two and three tier devices are shown in Figure 1.

In 2008 Fermilab coordinated the first 3D multiproject run for high energy physics with contributions from 15 institutions [6]. The run utilized the Chartered (now Global Foundries) 0.13 micron process with 1 micron diameter, 6 micron deep tungsten TSVs deposited early in the wafer processing. A single reticule was used for both the top and bottom tiers with the top tier mirrored on the right hand side of the reticule allowing a single wafer design to be used for both top and bottom layers. The original Tezzaron copper thermocompression process utilized an array of 2.7μm copper octagons on 4μm pitch. The copper provided both electrical contact and mechanical support. There were a number of issues with this submission and subsequent processing, including

bad centering of the reticule pattern, aging of copper, and misalignment of wafers, which must be aligned to within one micron. The thermocompression design was modified for DBI® processing by adding an oxide layer with imbedded 1.2μm diameter copper on top of the octagons, with the oxide providing the mechanical contact. The DBI® process solved the initial issues of wafer alignment encountered in the thermocompression bonded wafers from Tezzaron. Fermilab provided three designs for the run VIP - an ILC vertex chip, VICTR - a CMS track trigger chip, and VIPIC - an x-ray imaging design.

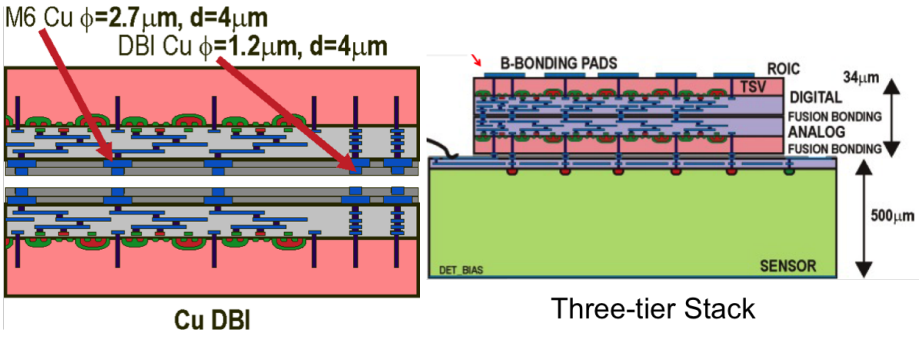

Figure 1: Left - Sketch of the two-tier 3D Stack. Right - Sketch of the three-tier 3D Stack.

After the wafers were face-to-face DBI® bonded, the ≈750μm thick bulk silicon was ground to expose the imbedded tungsten TSVs. The silicon surface was etched and an insulating oxide layer deposited. The surface was again planarized and a patterned top aluminum layer deposited which provided the contacts to the TSVs. This completed the processing of the two-tier wafers.

Sensor integration utilized a chip-to-wafer bonding process (Figure 2). The sensor wafer was fabricated at Brookhaven Laboratory. It is a 500μm thick p-on-n design with thin aluminum and oxide layers to comply with the topography requirements of the Ziptronix DBI® process. Each sensor is 8 x 8 mm, with active areas matching the various circuit geometries. After the topside Readout Integrated Circuit (ROIC) wafer processing described above, the patterned face of the two-tier stack was oxide bonded to a silicon handle wafer. The stack was then flipped over and the TSV exposure process was repeated for the bottom wafer. The DBI® layers were then deposited on this ROIC wafer stack with a matching pattern on the sensor wafer. The ROIC wafer is then diced, its surface activated and placed on the sensor wafer. After thermal treatment the handle wafer is ground and etched away, revealing the top pads that were deposited in initial wafer processing. Redundant pads on the sensor periphery, connected through the ROIC wafer TSVs and DBI® seed metal layers were also revealed in the final processing. The resulting two-tier readout chip extends 34 μm above the sensor wafer surface (Figure 3). After the bonding, scanning acoustic microscopy was utilized to detect bond voids and select chips for further testing.

3. Results for Chips DBI® Bonded to Sensors

3.1 VIPIC Tests

Most of the testing to date has concentrated on the VIPIC chip. VIPIC is designed for x-ray correlation spectroscopy with sparsified, deadtimeless readout with a frame time less than 10μs.

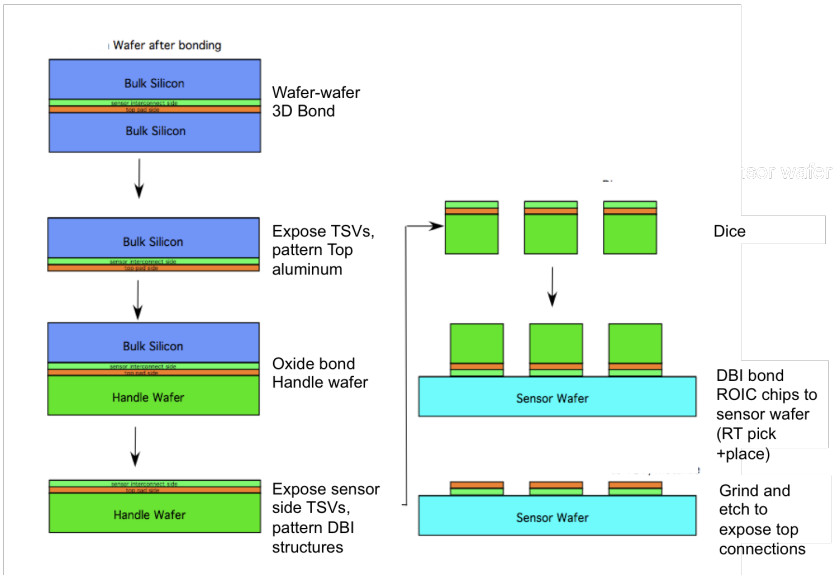

Figure 2: Process steps to bond two-tier 3D chips to the sensor wafer.

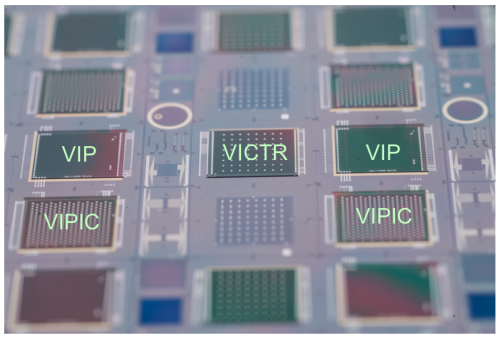

Figure 3: VIP, VICTR and VIPIC chips bonded to the Brookhaven sensor wafer. The ROICs extend 34 microns above the sensor surface.

The chip has a 64x64 array of pixels on 80 micron pitch with a shaping time of 250 ns. The chip is separated into analog and digital tiers with I/O bump bond pads distributed on the top surface. There are 25 inter-tier connections/pixel. A matrix of chips with this pad design can be bump bonded to a backplane to provide a four-side buttable array.

Before the DBI® bonded chips were available we also bump-bonded VIPIC chips to test sensors from Hamamatsu (HPK). These sensors were 300 microns thick with pixels on 100 micron pitch. The mismatch between the 80 micron ROICs and 100 micron pitch sensors was accommodated by utilizing a special ROIC bump pad pattern, skipping every fifth ROIC pixel. The availability of both bump and DBI® bonded devices allows us to compare the performance of the two technologies.

Chips were bench tested with a National Instruments Flex-Rio system with both ^{109}Cd and ^{55}Fe sources. Figure 4 shows a radiograph taken with the VIPIC of a watch gear using the ^{55}Fe source. This demonstrates full operation of the three-tier VIPIC with only a few dead channels. Figure 5 shows the noise distributions for the bare chip, the chip bump-bonded to the HPK sensor,

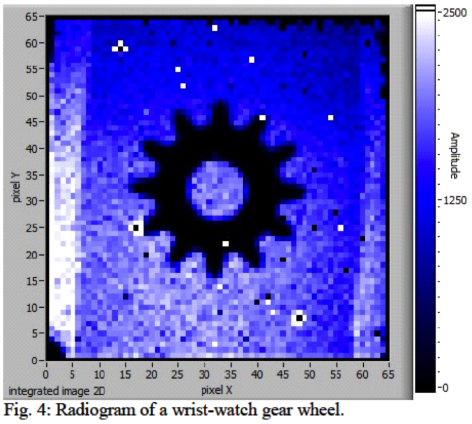

Fig. 4: Radiogram of a wrist-watch gear wheel.

Figure 4: Radiograph of a watch gear utilizing the VIPIC chip DBI® bonded to 500 micron thick sensor and an Iron 55 source.

and the chip DBI® bonded to the BNL sensor. Signals are calibrated to the ^{55}Fe and ^{109}Cd x-ray lines. The noise of the DBI® bonded assembly is 37.7 $\pm$ 3.1 electrons, compared to 70.2 $\pm$ 9.5 electrons for bump-bonded channels, and it is only 7% noisier than unbonded channels. The HPK and BNL sensors have somewhat different geometries and thicknesses. The DBI® bonded assembly has low interconnect capacitance due to the small geometry of the DBI® interconnect stack, which consists of a 8 μm DBI® seed pad, and 5 μm DBI® post interconnect. We therefore expect the load capacitance for the DBI® bonded devices to be dominated by the inter-pixel pad (48 μm) and implant (40 μm) capacitance ($\approx$17 fF). In the bump bonded detector bump bond pads have significant additional capacitance due to the coupling of bump pads to the silicon substrate ($\approx$50 ff) and $\approx$50μm diameter solder balls. The lower load capacitance in the DBI® bonded VIPIC is also reflected in larger gain for the DBI® bonded assembly.

3.2 VICTR Tests

The VICTR chip was designed as a prototype for a vertically integrated CMS track trigger module. The track trigger is based on the correlation of hits between closely spaced pairs of silicon strip detectors to identify candidates for hits associated with high momentum tracks. These correlations are inherently local and a 3D chip with TSVs is able to locally correlate hits from the top and bottom sensors, rather than routing signals around the periphery [13]. The two layers of a module consist of a long strip ($\approx$ cm) and a short strip ($\approx$ mm) sensor. In our case, based on chip size limitations the short strip sensor has 64 (ϕ) x 5 x 1mm (z) strips and the long strip sensor has 64 x 5 mm strips, both with 100 micron ϕ pitch. In the VICTR the top tier contains the long strip tier and the bottom contains the short strip tier and digital logic. The VICTR front end is based on a modification of an FEI4 design [14] utilized for another part of the 3D submission and is partially optimized for larger capacitance. A final design would have the VICTR DBI® bonded to the short strip tier with the long strip tier bump bonded to the long strip sensor through an interposer.

We have performed initial tests of a single VICTR chip DBI® bonded to a short strip sensor. This test chip is only partially bonded, with 109 of the 320 channels connected to the sensor. The initial tests also have the detector partially depleted (30 V of 170 V). Under these conditions the

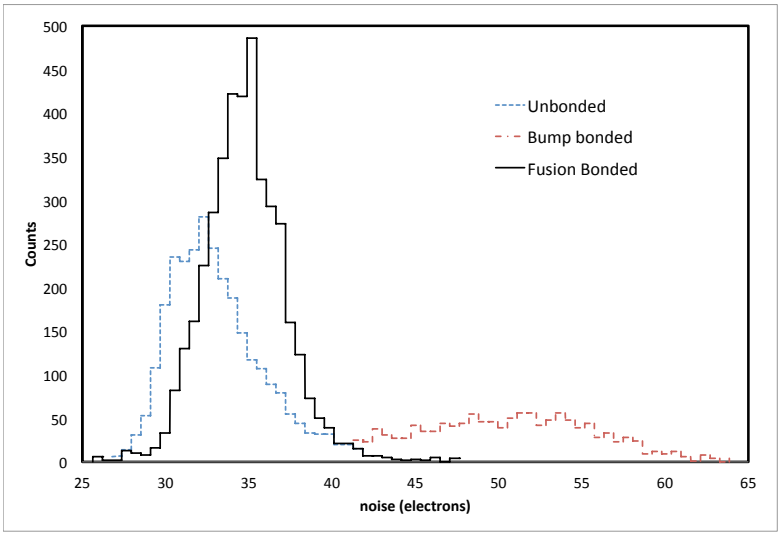

Figure 5: VIPIC noise measurements with floating, DBI® bonded, and bump bonded inputs. The unbonded sample consists of pixels that were not bonded due to the mismatch in HPK sensor and VIPIC pitch.

noise from bonded channels is about 700 electrons and that for unbonded channels is approximately 470 electrons. A sample turn-on curve for the Cd^{109} source is shown in Figure 6.

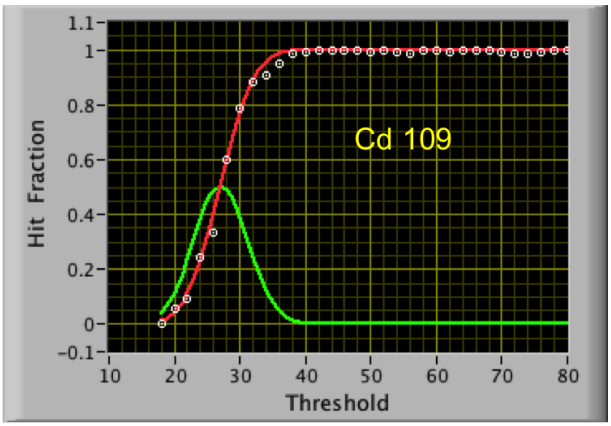

Figure 6: Turn-on curve for the VICTR chip bonded to a sensor.

3.3 VIP Tests

The VIP chip is designed as a demonstrator ILC vertex readout chip with single bunch time stamping. This application requires low mass, small pixels for good position resolution, and requires low power. These requirements were originally what drove us to investigate 3D technology, as the necessary functionality could not be accommodated in conventional hybrid pixel devices.

The VIP consists of a 192 x 192 array of 24 x 24 μm pixels. The pixels contain a charge integrating front-end with two sample and hold circuits for analog correlated double sampling. The pixels also contain an 8 bit digital time stamp. The chip utilizes a token passing scheme for sparse readout [3].

We have performed initial tests on the VIP and have successfully read out all 36,864 pixels. Figure 7 shows a radiograph of a tungsten mask patterned with a Fermilab logo placed on the top of the stack and exposed to a Cd^{109} source. Noisy pixels are suppressed.

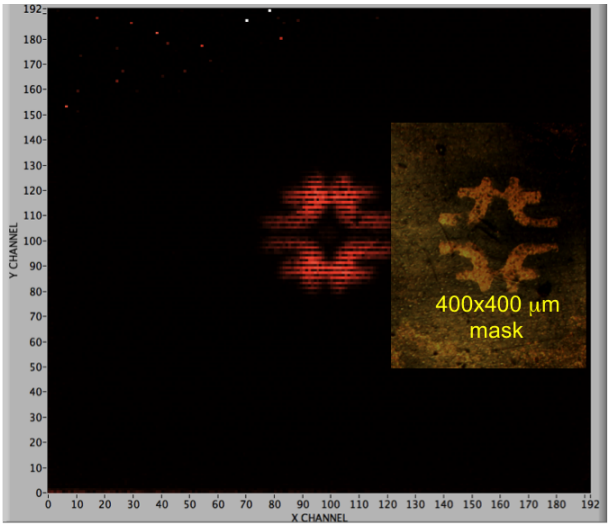

Figure 7: Radiograph of a $\approx$ 400 x 400 μm tungsten shadow mask (inset to the right) placed on a VIP chip oxide bonded to a sensor and exposed to a Cd^{109} source.

4. Next Steps

Before common application of these technologies for particle physics two problems must be solved. First the technologies have to be commercially available at reasonable cost. This depends on the path of commercial adaptation of 3D, but is likely to become more common in 3-5 years as transistor scaling becomes increasingly difficult and expensive and the commercial world moves to complex heterogeneous designs. Second, we need to deploy large areas of complex sensors with minimal dead area. Sensors can be made large with good yields, but a process like DBI® chip-to-wafer suffers from placement yields below 90% as the presence of micron-sized dust particles can result in mm-sized bond voids. A possible solution to this problem is to combine the 3D bonding process with 3D sensor (active edge) processing to provide reticule-sized active tiles that can be butted on all four sides to provide a fully active array of arbitrary size. The integration of the two technologies can provide a path to large area, complex, pixelated arrays at a reasonable cost.

We hope to demonstrate this in the near future by combining an active edge sensor fabricated by VTT [15] with a dummy ROIC. The sensor is a 200 μm thick n-on-p design fabricated on a 525 μm thick handle wafer. The intention is to demonstrate four side buttable pixelated sensor arrays fabricated with wafer-scale 3D bonding technology without using through-silicon-vias. In our design topside connections are made by thinning the top wafer to $\approx$ 10 μm and etching to

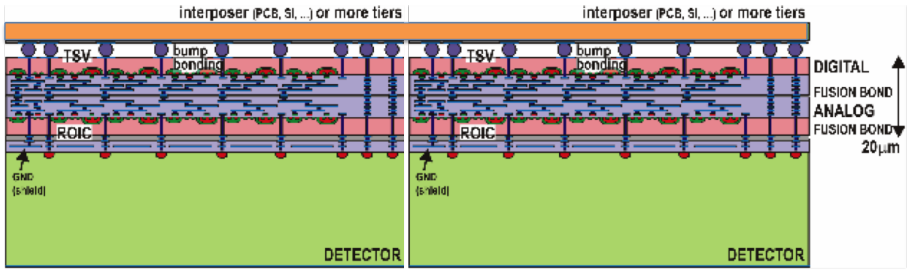

Figure 8: Interconnectivity for a sensor array based on 3D interconnect and active edge processing.

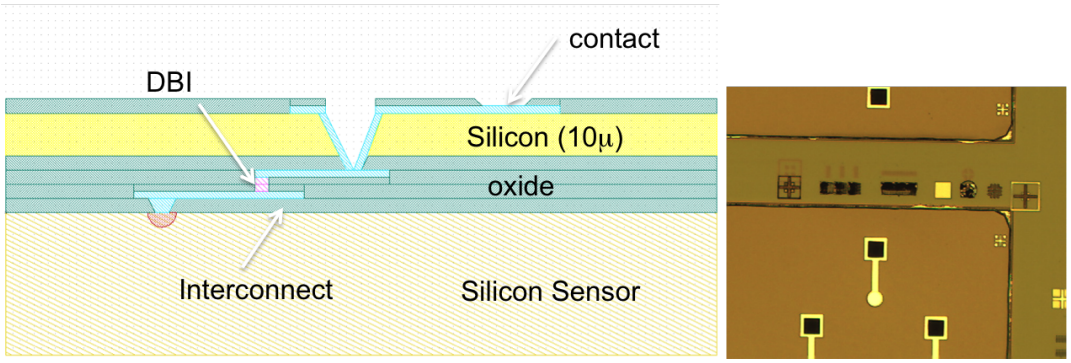

Figure 9: Left - Layup for the 3D/Active edge device.Right - Photograph of the processed wafer. The dark squares are where the top silicon is etched to contact the dummy ROIC wafer.

reveal what would normally be the bottom metal layer of the ROIC. An insulating oxide layer is deposited and etched, and top contact metal is deposited and patterned. The stack is shown in Figure 9. This process is now complete through topside patterning. The wafer stack must now be etched to remove the silicon between the sensor islands and the handle wafer will be removed. The silicon-on-insulator nature of the stack means that the process can be used to fabricate very thin sensors (<50 μm) integrated to ROICs.

5. Conclusions

We have now demonstrated a commercial process for 3D wafer-wafer and chip-to-wafer bonding. Our initial results show a significant reduction in noise relative to the conventional bump bonding process. This reduction in noise is likely to become more significant as the pixel pitch decreases and bumps become more closely spaced. Lower noise has several implications. It can be traded for power, which is very much a limiting factor in the design of future vertex detectors, from HL-LHC to ILC and CLIC. A system with lower noise can also accommodate lower thresholds, and therefore thinner, more radiation hard sensors. The design freedom allowed by separation of analog and digital sections and distribution of power and ground throughout the chip, such as on VIPIC, can also provide designers with the tools to minimize noise due to the coupling between analog and digital sections.

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[15] VTT TECHNICAL RESEARCH CENTRE OF FINLAND, P.O. Box 1000, FI-02044 VTT, Finland http://www.vtt.fi/index.jsp