PROCEEDINGS OF SCIENCE

DBBC3 Development

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The RadioNet3 JRA project named 'DBBC3' is progressing as planned. The first units of the 4 GHz bandwidth samplers are available as well as the CORE3 processing elements. The first functional mode for both of them has been successfully tested and the construction of two further DBBC3 units is under way. The main parts of the system are shown together with their performance, and an overview of the implementation is presented for data-rates of 32 and 64 Gbps with two examples of their application: a) astronomical for the EVN and for millimetre VLBI with the EHT (Event Horizon Telescope), and b) geodetic for the VGOS broadband network.

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1.Introduction

The RadioNet3 joint research project DBBC3 [1] (Joint Research Activities DIVA) is the continuation of the DBBC [2] system development. The aim is to engineer the third generation of a VLBI digital back-end. In this document a review of the instrument is presented describing the current status and the novel elements. Indeed several additional parts have been developed and incorporated into the system. In this document the description focuses on the L-version, supported by RadioNet3 and is the first to be realised. It is being specifically developed for the EVN network. The L-version is capable of output data-rates of 32 and 64 Gbps an can be applied for both astronomy with EVN and EHT (Event Horizon Telescope), and also geodesy with VGOS (VLBI Global Observing System) [3] .

2. DBBC3-L Architecture

The DBBC3 system needs to meet some fundamental requirements: it has to be backwards compatible with the existing back-ends of the previous generations and has to be able to support the new functions in a much wider input band. Moreover it should be able to handle all the required modes of operation for the planned EVN goals (minimum 2 times 4 GHz bandwidth) and VGOS (2 times 14 GHz bandwidth). As many stations are active in both networks a single system is mandatory. To be compatible with the existing systems, the new hardware needs to be mechanically and electrically level-compatible. This aspect is useful because existing DBBC terminals in the field could be upgraded to meet the new performance requirements by simply replacing the relevant parts. Components of the DBBC3 can be inserted in the DBBC2s which are in operation world-wide to improve their performance by offering additional functionality. The much higher performance of the new backends requires new hardware parts, to be accompanied by new firmware. As was mentioned, in a first step the DBBC3-L will be developed as a fully qualified 4 GHz DBBC. At the same time it can be used for the full 14 GHz required by VGOS operating with more 4 GHz pieces of band, as a preliminary phase during the development of the DBBC3-H type, which will be able to sample the full 14 GHz VGOS bandwidth in a single piece, capable then to operate at much higher data rate in a single band .
In fig. 1 a schematic view of the DBBC3-L architecture is shown. The system consists of an analogue to digital converter "ADB3-L", the processing unit with a powerful FPGA

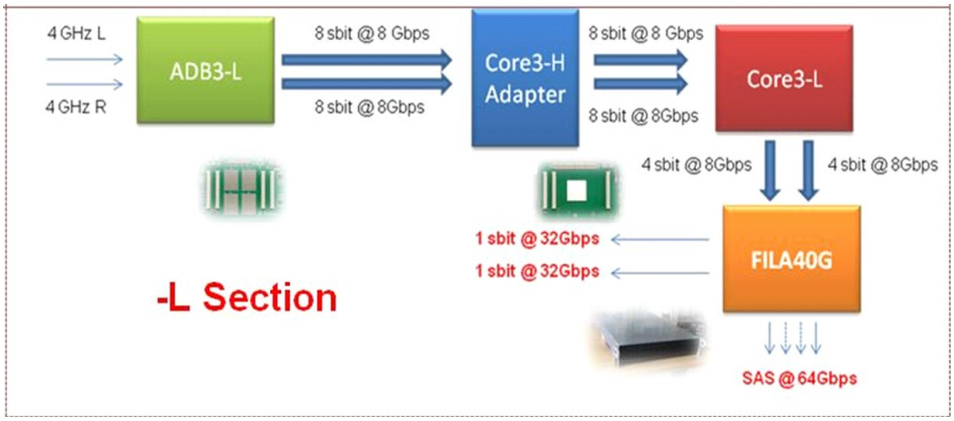

Fig. 1: Schematic view of the DBBC-L architecture

"CORE3L", and the unit responsible for transporting the processed and formatted data onto 40/100 Gb Ethernet "FILA40G".

3. Status of the main elements

3.1 ADB3-L

To convert the wide band analogue receiver signal to a digital representation, state of the art sampler chips are being used. A single ADB3-L sampler board has four samplers, which can be configured for a variety of functions, single and multiple input bands, real or complex sampling. Indeed, for example, in real mode the four samplers can be fed with a single input signal for handling the full 4 GHz bandwidth, or they can be fed with two signals of 2 GHz instantaneous bandwidth each, or with four signals of 1 GHz bandwidth each.
This board (see Fig. 2) has been designed, tested, and is ready for further development of firmware and testing till the production version can be released.

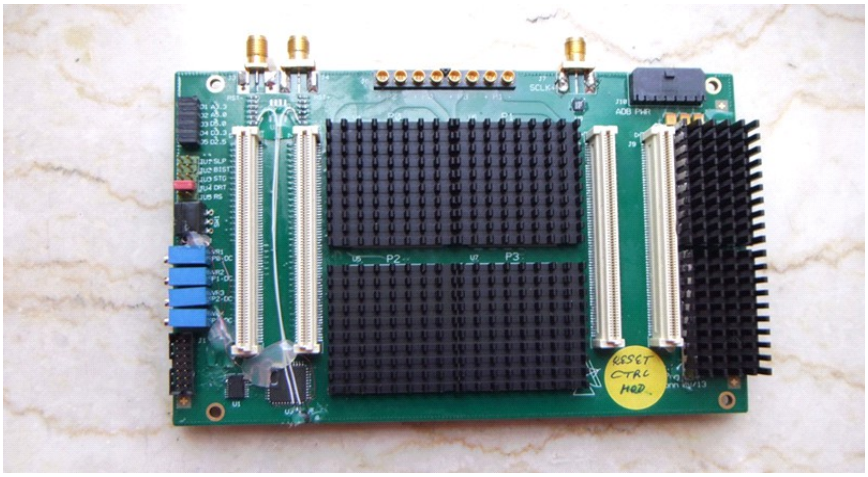

Fig. 2: Prototype of the ADB3-L board. The 4 samplers are hidden under the 4 heat sinks in the centre. Four white connectors for the high speed buses are on the left and right side.

2.3.2 CORE3-L

The sampled data have to be transported to the processing stage: data coming from the sampling board ADB3-L are routed to the CORE3 processing card using the lanes of the high speed input bus. This board is able to process data in different ways: DSC (Direct Sampling Conversion), DDC (Digital Down Converter) or PFB (Polyphase Filter Bank) firmware. From the pool of the processed channels a subset is selected according to the desired output data-rate defined by the observer or as limited by the recording or network media. The data is output through the high speed output bus.
Additional input and output connections are available to maintain the compatibility with the DBBC2 stack. The large digital signal processing resources available in the FPGA chosen for the CORE3-L allows to perform very sophisticated and powerful data processing.
The CORE3-L prototype has been debugged using firmware developed ad hoc. In Fig.3 a picture of the prototype board is shown. Further engineering is needed to reach the final production stage.

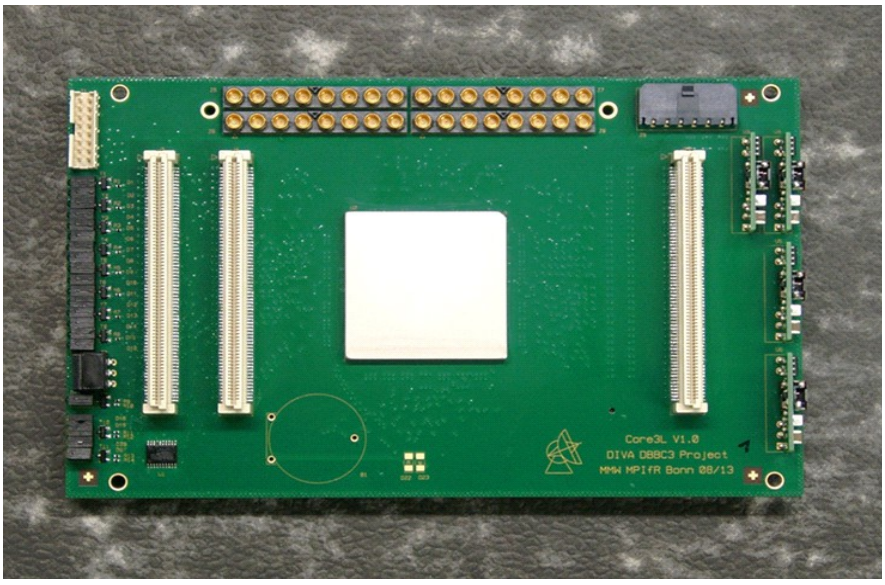

Fig. 3: Prototype of the CORE3-L board. In the centre the FPGA can be seen. The connectors for the high speed buses are visible on the left and right side. On the top are two rows of additional input connectors.

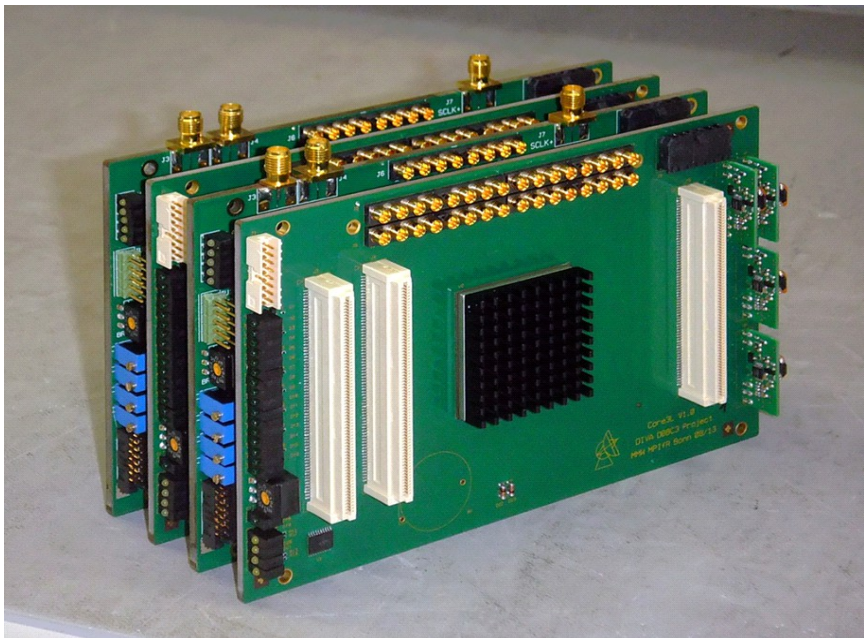

Fig. 4: Stack of two ADB3-L and CORE3-L for processing 4 GHz of bandwidth are shown as used in the DBBC3

4. The environment

In order to verify the behaviour of the integrated samplers and the processing units, a complete environment is required which produces the ancillary frequency and time signal needed for maintaining the phase coherence and the correct propagation of time through the whole system.

The sampler and processing boards are inserted in the so-called DBBC stack, which is a general purpose chain of boards like in the DBBC2, put in sequence together with an initial and a final element in the stack to input/output different signals. Moreover both the main ADB3-L and CORE3-L functional units have to be controlled by a computer to set and drive all the operations without fixed settings.
The very high output data rate makes it necessary to use 10 GE ports. So two different types of such interfaces have been developed within the project to provide a broad range of possibilities. The 10 GE ports are part of the environment but represent a very high end solution where more general applications could be envisaged.

4.1 The clock and time generation: CAT3

The whole system has to be driven by a clock which has to be extremely stable in frequency and synchronised with the UT time. The CAT3 board is a synthesiser developed for this project and capable of generating the clock signal at a programmable frequency, which for our purposes is kept fixed at 2048 MHz. The phase stability of the synthesiser needs to be the best possible. For this reason apart from the selection of components able to generate a highly stable signal, it is necessary to phase lock the synthesiser with an atomic clock, which in a VLBI station is normally a Hydrogen-Maser.

The CAT3 generates the sampling clock of 2048 MHz and the time reference signals at a rate of one pulse per second, called 1PPS, synchronised with an external UT time keeping generator, like a GPS receiver normally in use at a VLBI station.

The sampling clock is used in the ADB3-L for producing the digital version of the analogue signal applied at the input of the ADB3-L and to generate the running clock accompanying the digitised data to be transferred to the CORE3-L processing board. In this way all functions of the sampler and processing board are tightly coupled to a a clock which is extremely stable in frequency and synchronised with the UT time.

The 2048 MHz clock in the ADB3-L when used to sample the analogue signal is then reduced up to 256 MHz and this clock is producing the data samples in double data rate to be transferred through the HSI-HSI2 bus to the processing board. The 1PPS signal is transferred to the elements of the chain using the CCM bus, as in the usual DBBC stack, and in this way is made available to all the elements in the chain requiring it.

4.2 Network interfaces: FILA10G-S4 and C3_OPTINT

The CORE3-L output data can follow two different routes: either through the HSO bus included in the stack or using internal 10 GE interfaces.

In the first case an external 10 GE interface with more ports than used for the DBBC2 is required, and for this function the FILA10G-S4 interface board was developed, which includes support for 4 independent 10 GE ports. It is fed by 8 VSI standard interfaces. Any single CORE3-L can be used with a maximum of two VSI output equivalent ports, due to the limited capability of the I/O pins with respect to the full maximum output data rate, so a single FILA10G-S4 can receive data from a up to four independent CORE3-L.

The second method to produce data is to use the internal 10GE output ports available on the CORE3. This solution is very efficient when a large volume of data has to be produced, but

of course requires that part of the internal general resources are used to implement the network formatting and packaging. This suggests that the best solution has to be selected depending on the general range of application required, balancing the internal CORE3-L resources with the external ones offered by the FILA10G-S4.

The internal CORE3-L output route does not include the physical layer interface. For this project it has been realised in a dedicated board named C3_OPTINT. It is capable of supporting eight SFP+ 10 GE transceivers. It can be placed as a regular element in the DBBC stack and is directly connected with the CORE3L which drives all its output lines to enable the proper performance.

4.3 GCoMo: analogue Nyquist adapter and conditioning module

The ADB3-L sampler is capable of operating in the first Nyquist zone, which for our purposes is limited to 4096 MHz. In order to adapt the back end to different receivers/IF systems having an output in a pretty variable range, and at the same time to be able to process the full VGOS band covering the range 2-14 GHz, an additional unit has been developed, named GcoMo. It processes the input band limited to a maximum of 4 GHz to the first Nyquist zone in a very flexible way. This card can also adapt the analogue signal levels to what is required by the ADB3-L. This includes automatic gain control (AGC) or manual gain control and allows to perform total power measurements of the incoming signals. A complete prototype has been developed and debugged, and is now on its way to reach the production stage.

Fig. 5: Left: Internal view of the DBBC3. In the centre the stack with the two ADB3-L and CORE3-L can be seen. Right: Front view of the DBBC3.

References

[1] G. Tuccari, DBBC3, Proceedings of the 20th EVGA Meeting and 12th Analysis Workshop, Bonn, Germany, pag. 19-21, 2011.

[2] G. Tuccari, Development of a Digital Base Band Converter (DBBC): Basic Elements and Preliminary Results, New Technologies in VLBI, Astronomical Society of the Pacific Conference Series, ISSN 1050-3390, Vol. 306, 177-252, 2004.

[3] A.E. Niell, A. Whitney, B. Petrachenko, W. Schlüter, N. Vandenberg, H. Hase, Y. Koyama, C.Ma, H. Schuh, and G. Tuccari, VLBI2010: Current and Future Requirements for Geodetic VLBI Systems, 2005 IVS Annual Report, pp. 13−40, 2006.