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The Belle II Pixel Detector — How to handle high occupancy

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The innermost Pixel Detector (PXD) of the Belle II experiment makes use of the DEPFET (Depleted P-channel Field Effect Transistor) technology to provide the accurate position measurements that are needed for the reconstruction of B meson decay vertices. It has to work in very challenging conditions: The instantaneous luminosity of $8 \times 10^{35}\,\mathrm{cm}^{-2}\,\mathrm{s}^{-1}$ expected at the collider SuperKEKB causes a high event rate and a large background, the resulting sensor occupancy is furthermore increased by the PXD's close proximity to the interaction point.

This contribution presents the strategies of how to deal with the aforementioned challenging conditions in terms of sensor layout and electronic readout. These strategies are: a segmentation of the sensor to allow different operating voltages (to deal with inhomogeneous irradiation); the four-fold rolling shutter readout (making readout four times as fast); a fast electronic shutter, the so-called "Gated Mode" (to make the sensor blind during short periods of increased background particle flow); and zero-suppressed readout focused on small "Regions of Interest" (to suppress background hits).

These strategies have been demonstrated on prototype sensors with prototype readout electronics.

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1. Introduction

The upgrade of the KEKB collider (at KEK in Tsukuba, Japan) to SuperKEKB results in a 40-fold increase in luminosity, with a target peak value of $8 \times 10^{35}\,\mathrm{cm}^{-2}\,\mathrm{s}^{-1}$ [1]. This high luminosity makes upgrades of the Belle detector necessary. The expected occupancy for the inner tracking sensors renders the use of double-sided silicon microstrip sensors unfeasible, so the future Belle II detector will feature silicon pixel sensors for the two innermost layers of vertexing detectors. These two layers form the Pixel Detector (PXD), which uses 40 silicon pixel sensors in total, each with 250×768 pixels. The typical pixel size is $50\,\mu\mathrm{m} \times 75\,\mu\mathrm{m}$ [1].

Nevertheless, the high luminosity poses a challenge even for silicon pixel sensors. It causes a high event rate and a large background, the resulting sensor occupancy is furthermore increased by the PXD's close proximity to the interaction point. The readout system of the PXD can handle occupancies up to 3 % [1], and we apply a range of strategies to keep the occupancy at a manageable level. These strategies include a thoughtful sensor design (to handle inhomogeneous irradiation and increase the readout speed) and sophisticated readout schemes (to handle periods of increased background particle flow and to reject background hits).

2. The DEPFET sensor

Each pixel of the DEPFET (DEpleted P-channel Field Effect Transistor) sensor consists of a field effect transistor sitting on a depleted silicon substrate, as is shown in Figure 1. The measurement principle works as follows [2]:

1. The intrinsic charge carriers of the silicon bulk are removed by sidewards depletion.
2. When an ionizing particle hits the sensor material, it deposits a part of its energy and creates electron-hole-pairs.
3. The electrons are collected in the "internal gate", a local potential minimum directly below the transistor channel. The holes are collected at the back contact and don't contribute to the signal.
4. When the transistor is turned on by an appropriate gate voltage, the transistor channel is modulated by the collected charge in the internal gate, resulting in an increased drain current.[1]
5. This drain current is digitized by the readout electronics.
6. The readout is non-destructive, and the electrons in the internal gate have to be actively removed by applying a potential to the clear contact.

This measurement principle has several advantages [2]:

- Low noise: instead of voltages we read currents, so the noise is influenced by the low capacitance of the readout electronics, instead of the higher capacitance of the drain lines.
- Low power consumption: only a small subset of the sensor is in ON state at a time, due to the "rolling shutter readout mode" (see section 4).
- High gain ($g_\mathrm{q} \approx 0.5\,\mathrm{nA}$ per electron) and consequently high signal-to-noise ratio ($SNR \approx 40$) [3].
- The silicon can be thinned down to 75 µm, and serves as sensor material, support structure and substrate for metal routings and ASICs (Application Specific Integrated Circuits).

[1] Note that the charge collection of the previous step happens always, also when the transistor is in the OFF state.

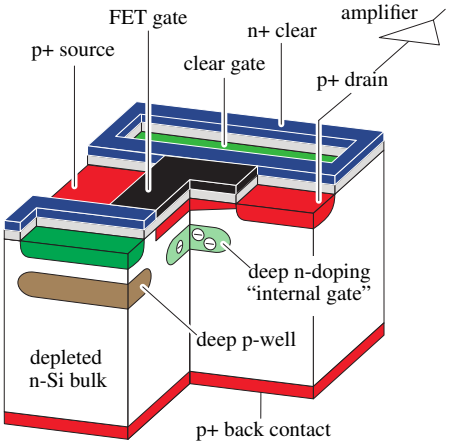


Figure 1: Principle of a DEPFET pixel: A field effect transistor (p+ source, FET gate, p+ drain) sits on top of a depleted silicon substrate. Particle-induced electrons are collected in the internal gate and modulate the drain current. The stored electrons are removed via the n+ clear contact.

3. How we handle inhomogeneous irradiation

Irradiation will change the silicon properties, resulting in a shifted optimal working point in terms of operation voltages [4]. We expect around 20 kGy of photon irradiation per year, and 1010 $\mathrm{cm}^{-2}\,\mathrm{ab}^{-1}$ neutrons, both of which will be inhomogeneous [1]. To reduce the effect of the working point shift, the sensor is supplied with three different gate voltages. This is illustrated in Figure 2. That way, we can adjust the optimal voltages of three sensor parts along the z-axis to account for irradiation. The PXD power supplies are prepared to provide these three different gate voltages.

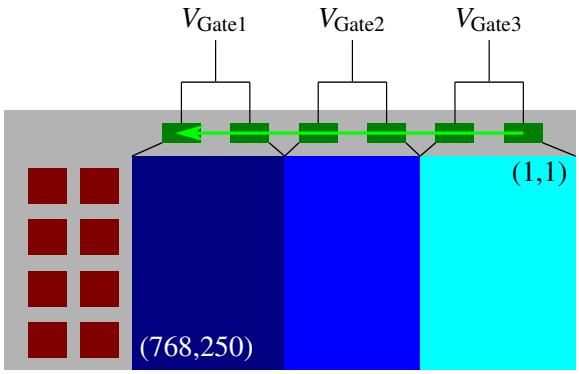


Figure 2: The DEPFET sensor can be supplied with three different gate voltages $V_{\mathrm{Gate1-3}}$. That way we can account for irradiation-induced shifts of the operation point. The green boxes symbolize the "Switcher" chips, which apply the gate and clear voltages consecutively to the pixel rows, and the red boxes symbolize the "Drain Current Digitizer (DCD)" and "Data Handling Processor (DHP)" chips, which read the drain currents and perform processing.

4. How we decrease the readout time

The readout is performed in a "rolling shutter mode", i.e. the sensor rows are read out sequentially by always the same readout electronics [1]. For the schematic sensor in Figure 2 the readout starts

at the right side and moves to the left. The Read-Clear cycle for one pixel row takes roughly 100 ns [1], which would result in a total frame time of nearly 80 µs. As a speedup we address four pixel rows in parallel, as sketched in Figure 3. This speedup reduces the frame time to 20 µs.

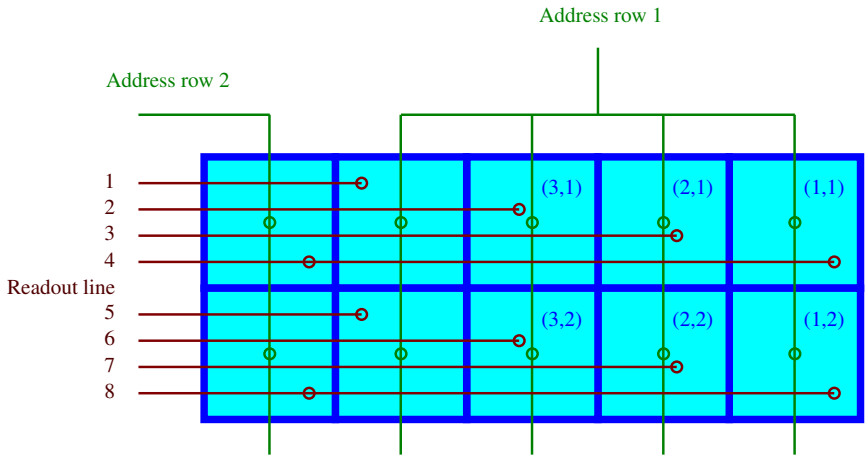


Figure 3: The "four-fold readout" scheme addresses four pixel rows at the same time. This scheme reduces the total frame time by a factor four, and increases the neccessary number of readout channels by a factor four.

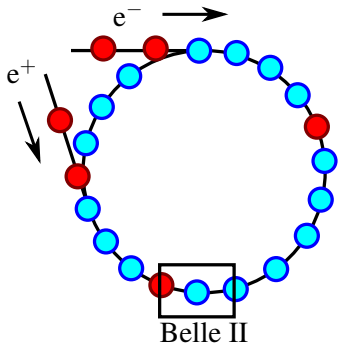
Consequently, this "four-fold readout" needs four times the number of readout channels, which is perfectly feasible. The 250×768 pixels of a sensor are read out by 192 address rows and 1000 readout lines. The four-fold readout is a proven technique; it has been used in several beam tests and is used in everyday laboratory operation.

5. How we handle "noisy bunches"

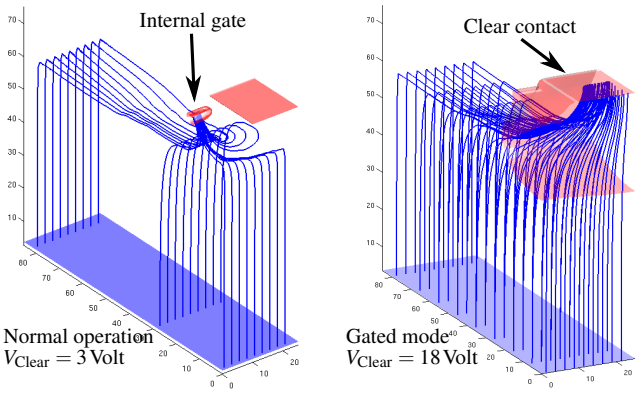
The collider SuperKEKB continuously injects new particle bunches with a total frequency of 50 Hz. These "noisy bunches" need to cool down for 4 ms, emitting many background particles [1]. The resulting occupancy would cause a deadtime of 20 % for the Pixel Detector, which is not feasible.

All sensors have to be blinded during the short time when a noisy bunch passes the detector. While other subdetectors of Belle II simply stop their readout, DEPFET sensors have to stop the charge collection in the internal gate. This is done by switching into the so-called "gated mode". This is a kind of "electronic shutter", where the field configuration in the sensor is modified. While in normal operation all electrons are collected in the internal gate, in gated mode the clear contact is most attractive. All the electrons created during gated mode operation are cleared immediately, and none of them reaches the internal gate to distort the signal. Furthermore, all the charge in the internal gate is preserved; the signal state before the gated mode is untouched. It takes approximately 300 ns to go into gated mode operation and back to normal readout [5]. The whole transition can be triggered selectively when noisy bunches pass.

This operation mode has been proven to work on small prototype sensors [5], but it still has to be proven on the full-scale sensors with the final version of the readout electronics.



(a) Injection scheme of SuperKEKB: New particles are injected into their host bunches with 25 Hz per beam. During the cooldown phase (4 ms) the noisy bunches pass through the Belle II detector with 50 Hz.



(b) Simulated electron drift trajectories during normal operation (left) and in gated mode (right): During normal operation (left), all electrons drift to the internal gate, regardless of where they are created inside the depleted sensor substrate. In gated mode (right) all electrons drift directly to the clear contact [1].

Figure 4: The injection scheme of SuperKEKB (4a) makes it neccessary to shield the PXD against noisy bunches. This is achieved with the "gated mode" operation (4b).

6. How we reject background hits

During the frame time of 20 µs a DEPFET sensor accumulates a lot of uninteresting background hits with no way of distinguishing them from the real signal hits. Due to the large amount of data it is not feasible to send all hits (signal and background) to the readout electronics to be sorted out offline. The data rate is limited by the data transmission line to 1 GBit/s per sensor [1]. The Pixel Detector therefore relies on information from outside, in particular from the Silicon Vertex Detector (SVD). Tracks measured in the SVD are extrapolated to the PXD sensors, where "Regions of Interest" (ROIs) are defined. Only hits inside these ROIs are read out, the rest is discarded. Tracking and calculation of ROIs happens on trigger level within 5 µs, *before* the PXD is read out [1].

There are two systems which provide regions of interest:

1. The High Level Trigger (HLT): This system performs track finding and track fitting of tracks in the SVD and Central Drift Chamber (CDC) using the same software as for offline analysis. On top of that it performs the track extrapolation to the Pixel Detector [6].
2. The Data Concentrator (DATCON): This FPGA-based system performs SVD-only track finding and track fitting in hardware, using a fast Hough transform algorithm. Also the track extrapolation is done in the FPGA [7].

The regions of interest found by these two systems are merged with a logical OR operation, to make sure that all signal hits are preserved. This has been proven to work in a beam test, where sensors from both the Silicon Vertex Detector (SVD) and PXD were tested [6, 7]. Both HLT and DATCON succeeded in delivering meaningful Regions of Interest, and the readout electronics successfully stored hits inside these regions and rejected hits outside.

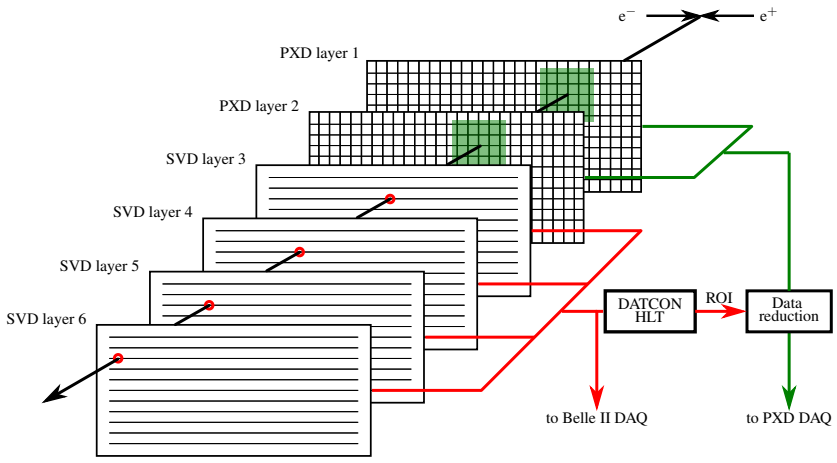


Figure 5: Background suppression for the PXD: The Silicon Vertex Detector (SVD) tracks particle trajectories with high timing accuracy (red circles), yielding a prediction of where the particle should have left a hit on the PXD sensors. Around these predicted hit positions we define "Regions of interest" (ROIs, green squares). Only hits inside these ROIs are read out.

7. Conclusions

The Belle II Pixel Detector (PXD) applies several strategies to keep the occupancy at a manageable level below 3 %. Some strategies operate already on the level of sensor design: We can supply three different gate voltages to account for inhomogeneous irradiation, and we read out four pixel rows in parallel to reduce the total frame time. Other strategies involve sophisticated readout techniques: we use the "gated mode" to make the sensor blind during short periods of increased background particle flux, and use fast track information from outside detectors to reject background hits.
These strategies have been proven to work on prototype sensors with prototype readout electronics.

References

[1] Doležal, Z. and Uno, S. (editors) *Belle II Technical design report, KEK Report 2010-1 (arXiv:1011.0352 [physics.ins-det])*, arXiv (2010), URL `http://arxiv.org/abs/1011.0352`.

[2] Kemmer, J. and Lutz, G., *New detector concepts*, Nuclear Inst. and Methods in Physics Research, A, 253 (1987) 365.

[3] Richer, R., Andricek, L. and Fischer, P., *Design and technology of DEPFET pixel sensors for linear collider applications*, Nuclear Inst. and Methods in Physics Research, A, 511 (2003) 250.

[4] Lindström, G., *Radiation damage in silicon detectors*, Nuclear Inst. and Methods in Physics Research, A, 512(1-2) (2003) 30–43.

[5] Prinker, E., *Testing of the Gated Mode for the Belle II Pixel Detector*, Master's thesis, Ludwig-Maximilians-Universität München (2015).

[6] Bilka, T. et al., *Demonstrator of the Belle II Online Tracking and Pixel Data Reduction on the High Level Trigger System*, arXiv, URL `http://arxiv.org/abs/1406.4955`.

[7] Schnell, M., *Development of an FPGA-based Data Reduction System for the Belle II DEPFET Pixel Detector*, Ph.D. thesis, Rheinische Friedrich-Wilhelms-Universität Bonn (2015).