

Development of the electromagnetic calorimeter waveform digitizers for the Muon $g-2$ experiment at Fermilab

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The upcoming Fermilab E989 experiment will measure the muon anomalous magnetic moment a_μ . This measurement is motivated by the previous measurement performed in 2001 by the BNL E821 experiment that reported a 3-4 standard deviation discrepancy between the measured value and the Standard Model prediction. The new measurement at Fermilab aims to improve the precision by a factor of four reducing the total uncertainty from 540 parts per billion (BNL E821) to 140 parts per billion (Fermilab E989). Such an improvement requires a reduction by a factor of three in the systematic uncertainties. Among other improvements, a new calorimetry system is being designed and built for the E989 experiment. This paper describes the waveform digitizer system deployed for the electromagnetic calorimeter.

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1. Introduction

The anomalous magnetic moment of the muon $a_\mu = \frac{g-2}{2}$, where g is the gyromagnetic ratio, is a long-standing precision test of the Standard Model (SM). The magnetic moment of the muon is defined as:

$$\vec{\mu} = g \frac{Q}{2m} \vec{s}, \quad (1.1)$$

where Q is the electric charge of the particle, m is the mass and, \vec{s} is the spin vector. In Dirac theory $g = 2$ and therefore there is no contribution from the anomalous part to the magnetic moment. Contributions from higher order QED, hadronic and weak interactions shift g slightly above 2. The latest measurement performed in 2001 by the BNL E821 experiment [1] reported a measured value of $a_\mu = (116592089 \pm 63) \times 10^{-11}$, which represents a 3-4 standard deviation discrepancy from the current SM prediction. The difference could be a sign for physics beyond the SM such as supersymmetry [2, 3] or dark photon [4]. This tantalizing result motivates the new measurement of a_μ that will be performed by the E989 Collaboration at Fermilab [5]. E989 aims to reduce the total systematic uncertainty from 540 ppb to 140 ppb, collecting 21 times more data (factor about four reduction in statistical uncertainty) and improving the detector and magnetic field systems (factor about three reduction in systematic uncertainties). As shown in Fig. 1(a), if both the measured value and SM prediction remain the same and given the expected improvement in the measurement, the difference between measurement and prediction would exceed five standard deviations significance. The theoretical uncertainty is dominated by hadronic vacuum polarization and hadronic light-by-light contributions. The vacuum polarization contribution is determined using data from e^+e^- collisions. New experimental results are now available [6] and anticipated [7]. Work is in progress to improve the prediction of the light-by-light [8, 9] contribution. The theoretical precision could consequently be improved from 420 ppb to 250 ppb leading to an 8 standard deviation significance between measurement and prediction.

The anomalous magnetic moment is extracted from measurement of the anomalous spin precession frequency ω_a of the muon in a magnetic field:

$$\vec{\omega}_a = -\frac{Q}{m} a_\mu \vec{B}. \quad (1.2)$$

The muons are stored in a magnetic storage ring with a 7.1 m radius operating at 1.45 T and a cyclotron frequency of 149 ns. The positive muons stored in the ring decay into positrons via the parity-violating V-A interaction. Therefore the energy spectrum of the decay positrons in the laboratory, where the muons are boosted, depends on the muon spin angle relative to the muon momentum direction. In consequence the number of high-energy positrons oscillates at the ω_a frequency (see Fig. 1(b)). The role of the calorimetry is thus to measure the energy of the positrons and their arrival time. The magnetic field intensity will be measured via nuclear magnetic resonance techniques in terms of the Larmor precession frequency of a free proton ω_p . Given ω_a and ω_p , the anomalous magnetic moment is extracted via:

$$a_\mu = \frac{\omega_a \mu_p m_\mu g_e}{\omega_p \mu_e m_e 2}, \quad (1.3)$$

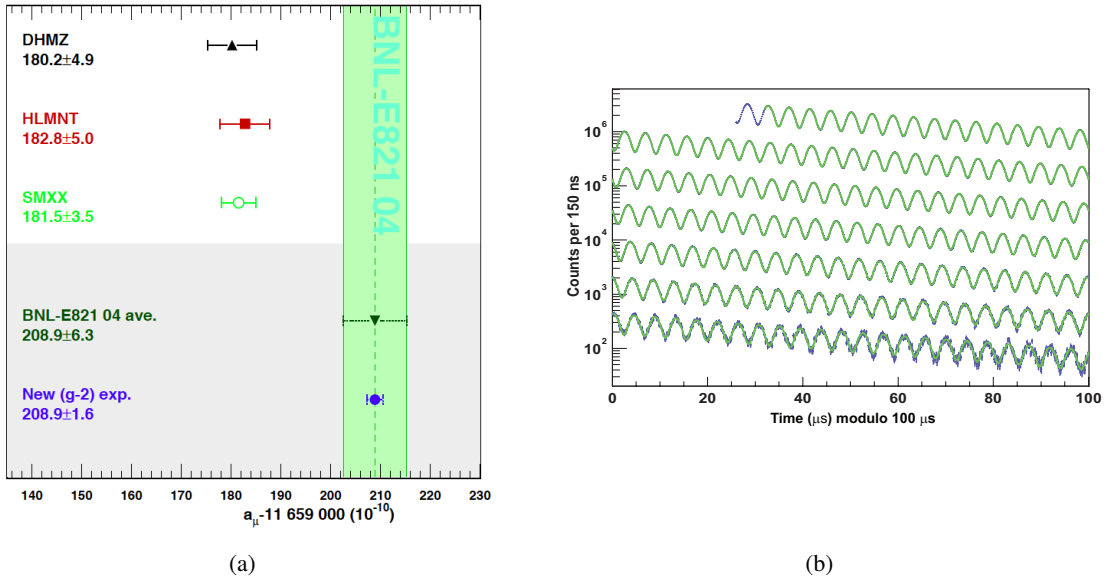


Figure 1: 1(a) Summary of the current SM prediction along with the BNL E821 measurement and the projected uncertainty on the incoming Fermilab E989 experiment. 1(b) Number of high-energy positrons versus time for the 2001 data set from the BNL E821 experiment.

where the proton-to-electron magnetic moment ratio μ_p/μ_e , the muon-to-electron mass ratio m_{μ}/m_e and the electron gyromagnetic ratio g_e come from other measurements as well as SM theory [10, 11].

2. Electromagnetic calorimetry

2.1 Calorimeter design

The goal of the calorimetry for the Fermilab E989 is to be able to measure the arrival time of a positron with a 100 ps accuracy and to measure its energy with a resolution better than 5% for an energy of 2 GeV. Čerenkov calorimetry [12] was chosen due to its fast response that satisfies the timing requirement. There will be 24 calorimeter stations deployed around the storage ring. Each calorimeter station is segmented in 54 lead fluoride crystals with dimension $25 \times 25 \times 140 \text{ mm}^3$. Each crystals is read out by a monolithic 16-channel silicon photomultiplier (SiPM) having 57,344 $50\text{-}\mu\text{m}$ pixels.

2.2 Read-out electronics: waveform digitizer

2.2.1 Requirements

Each SiPM will convert the Čerenkov light created inside the crystal to an analog waveform. Those signals have to be digitized in order for the data acquisition system (DAQ) to process them for on-line analysis and storage on disk (for off-line analysis). The read-out electronics have to comply with the calorimeter resolution requirement (timing and energy). Table 1 summarizes the resulting requirements.

Feature	Driving Consideration	Requirement	Design choice
Digitization rate	Pileup identification	≥ 500 MSPS	800 MSPS
Bit depth	Energy resolution/Pileup	12 bits	12 bits
Station readout rate	Fill length and repetition rate	≥ 3 Gbit/s (avg.)	4 Gbit/s (avg.)
Master clock stability	Negligible ω_a systematic	< 10 ps over $700 \mu\text{s}$	-
Sampling clock stability	Time base for frequency ω_a	< 1 Hz (< 1 ppb)	-

Table 1: Summary of the minimum clock and digitization requirements for the calorimeter waveform digitizer

A dominant sources of uncertainty on the ω_a measurement comes from pile-up, when two positrons hit the same calorimeter within a short time window. The overall pile-up requirement for the experiment is that the system must be able to distinguish pulses separated by 5 ns; this requires a digitization sampling rate of at least 500 MSPS. Given that a higher digitization rate would provide headroom and allow for better signal fidelity, the choice was made for a 800 MSPS sampling rate. The energy resolution budget and the need for headroom in pile-up study set the analog-to-digital converter (ADC) to have a 12-bit resolution. The anticipated muon fill length of $700 \mu\text{s}$ and repetition rate of 12 Hz requires the read-out rate of each waveform digitizer to be at least 3 Gbit/s on average. Given the desired precision on the measured ω_a frequency, the sampling clock should have a stability better than 1 Hz, i.e. about 1 ppb. The sampling clock of 800 MHz will be generated from the 40 MHz master experiment clock that provides the time reference to all the detector systems. The up-conversion happens on-board of the waveform digitizer by means of a clock synthesizer. The master clock has to be stable over a muon fill of $700 \mu\text{s}$ below a 10 ps level.

2.2.2 Design overview

The waveform digitizer design complies with the Advanced Mezzanine Card (AMC) and micro-Telecommunications Computing Architecture (μTCA) standards. The AMC standard provides modularity in the board design and the μTCA environment provides power, packaging, cooling and connectivity. The design choice does not use two redundant μTCA controller hubs (MCH); one of them is replaced by a custom board called AMC13. The AMC13, developed by Boston U. for the CMS hadron calorimeter upgrade effort [13, 14], provides the primary experimental interface to the waveform digitizer. It provides the 40 MHz master experimental clock, trigger and control signals via the CERN TTC protocol [15]. It provides as well parallel data transfer between the 12 waveform digitizers hosted in one VadaTech VT892 μTCA crate (60 Gbits/s aggregate) and the DAQ computer via a 10 Gbit/s optical link.

Figure 2 shows the design of the main board. It is a five-channel digitizer (one channel per crystal, 1296 channels total), each channel having an ADC (TI ADS5401) and its associated field programmable gate array (FPGA) to control the acquisition logic (Kintex 7K70T). The ADC chip consists of two interleaved ADCs operating at half the sampling rate with a common track and hold front-end that operates at the full sampling rate. Each channel has a 1 Gbit DDR3 memory (Micron MT41J64M16) that can buffer 120 muon fills. The so-called master FPGA (Kintex 7K160T) is responsible for interfacing the waveform digitizer with the rest of the crate (AMC13 and MCH). It

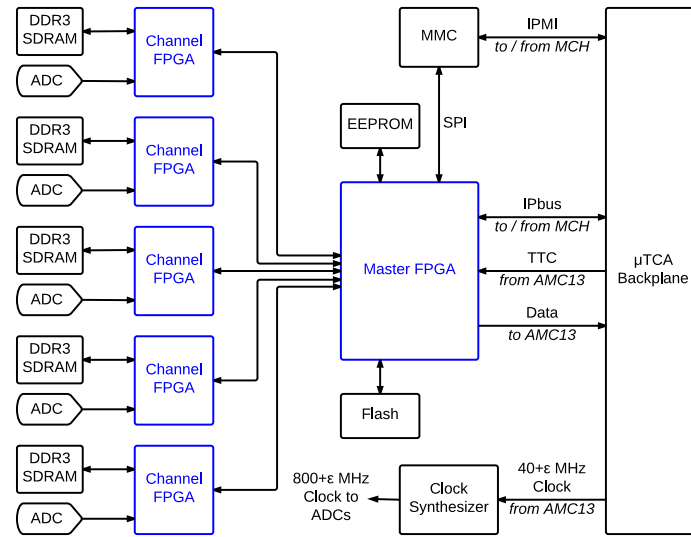


Figure 2: Block diagram of the anticipated final version of the five-channel waveform digitizer main board.

has to decode the TTC signal received from the AMC13 via the backplane to extract trigger and control signals (the AMC13 decodes the clock from the TTC signal and send it along the TTC signal to the master FPGA). It controls the data acquisition of the five channels, passing along the trigger signal and transferring data from each channel sequentially to the AMC13. The master FPGA communicates with the MCH (VadaTech UTC002) either via the intelligent platform management interface (IPMI) [16] or IPbus [17] protocols for configuration. A flash memory (Micron N25Q256A) allows the master and channel FPGA to be programmed automatically when the nominal power is delivered to the board. Figure 3(a) shows the current main board prototype being tested. The master clock that is provided to each channel ADC to sample the data is blinded and up-converted from the $40+\varepsilon$ MHz clock to $800+\varepsilon$ MHz by the TI LMK04906 clock synthesizer. The clock synthesizer chip up-converts the clock by means of dual phase lock loops and an internal voltage-controlled oscillator. The clock synthesizer generates six independent outputs with programmable delay that could be used, if necessary, to ensure synchronization of the five sampling clocks sent to the five ADCs. The sixth channel will be used for real-time monitoring of the up-converted clock frequency. The clock, as well as the trigger signal, can be delivered from an external front panel on the main board

The first mezzanine board is the power supply board (see Fig 3(b)). It supplies all the analog and digital voltages generated from the 12 V payload provided by the μ TCA crate via the backplane. On an earlier prototype version the power supply and regulation were implemented on the main board itself. It suffered from power regulator failures that rendered the board irreparable. Moving the power supply to a mezzanine card allows for an easy replacement without affecting the main board and provides more design flexibility. The second mezzanine card is the analog front-end board (AFE). Its role is to adapt the analog waveform coming from the SiPM board to meet the main board's requirements. The AFE's key features include a DC-coupling in order to avoid rate-dependent effects (the waveform rate drops from about 10 MHz to 20 kHz between the



Figure 3: The current five-channel prototype of the waveform digitizer: 3(a) the main board only and 3(b) the main board with its power supply (on the left) and analog front-end (on the right).

beginning and the end of a muon fill), a digital offset to use the full 1 V peak-to-peak range of the ADC and bandwidth filtering to reduce noise (anti-aliasing filter).

2.2.3 Performances

The current, and last, waveform digitizer prototype is being tested at Cornell U since July 2015. The intrinsic noise level of the waveform digitizer should remain below 1.5 mV to avoid noticeable degradation on the measured energy resolution of 5% in the calorimeter. Figure 4 shows that this requirement is met with the current prototype. Channel-to-channel noise level differences arise from the variation in capacitance in the trace lengths. The data acquisition chain of each channel (interfacing from the ADC to the DDR3 memory) was successfully tested using digital test patterns generated by the ADC itself. 10 MHz sine-waves were sent to the AFE as the first test with an actual waveform. The result is shown in Fig. 5(a). The residual distribution from the least-square fit has a width larger than the intrinsic noise level of the waveform digitizer by about 0.2 mV. Tests were performed successfully to ensure that the 4 Gbit/s transfer rate is reached. Another important step was completed by filling entirely one μ TCA crate with 12 WFDs and programming all the FPGAs. Noise data were read-out without noticing baseline noise variation.

The first end-to-end test was performed recently at Cornell U. A pulsed laser mimicking the Čerenkov light inside a calorimeter crystal fired a SiPM that sent its analog waveform to the waveform digitizer. The data acquisition of the digitizer was controlled by the MIDAS DAQ software [18, 19] and the collected raw data were processed via the ROME software. Figure 5(b) shows two captured pulses a repetition rate of 20 MHz. This test stand will allow to characterize the waveform digitizer in realistic operating condition. Anticipating conclusive test, the full production of more than 300 boards is expected by the end of 2015.

3. Conclusion

The calorimeter waveform digitizer system is being built for the new Muon $g-2$ experiment at

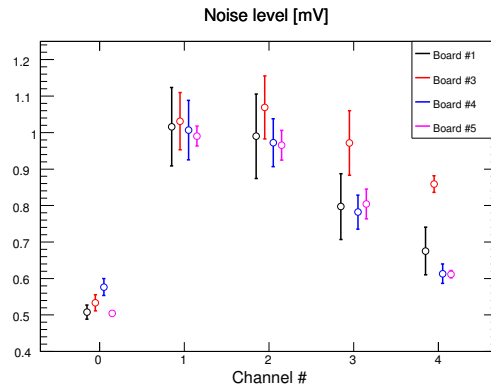


Figure 4: Intrinsic noise level of the five digitization channels for four boards with the current prototype design.

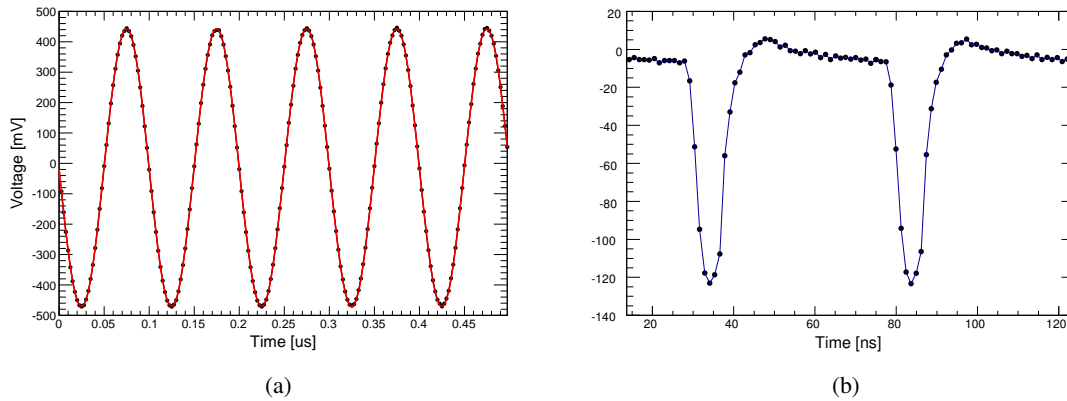


Figure 5: 5(a) 10 MHz digitized sine-wave to which was applied a least-square fit (one interleaved ADC only). 5(b) Digitized SiPM pulses fired by a laser (20 MHz repetition rate).

Fermilab. The experiment plans to begin data taking by summer 2017. The expected improvement in the systematic uncertainties require a new state-of-the-art calorimetry system with associated read-out electronics. The read-out electronics consist of 1296 channels digitizing at 800 MSPS with a 12-bit ADC resolution and a read-out rate per five-channel waveform digitizer of 4 Gbit/s. The prototyping stage is near completion and full production should happen before the end of the year 2015. A complete end-to-end test (calorimeter, electronics, DAQ, clock distribution system) will happen using the electron beam at SLAC during spring 2016. The first result with 1-2 times the BNL E821 statistics is expected for summer 2018.

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