

## Development of the photomultiplier tube readout system for the first Large-Sized Telescope of the Cherenkov Telescope Array

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The Cherenkov Telescope Array (CTA) is the next generation ground-based very high energy gamma-ray observatory. The Large-Sized Telescope (LST) of CTA targets 20 GeV – 1 TeV gamma rays and has 1855 photomultiplier tubes (PMTs) installed in the focal plane camera. With the 23 m mirror dish, the night sky background (NSB) rate amounts to several hundreds MHz per pixel. In order to record clean images of gamma-ray showers with minimal NSB contamination, a fast sampling of the signal waveform is required so that the signal integration time can be as short as the Cherenkov light flash duration (a few ns). We have developed a readout board which samples waveforms of seven PMTs per board at a GHz rate. Since a GHz FADC has a high power consumption, leading to large heat dissipation, we adopted the analog memory ASIC “DRS4”. The sampler has 1024 capacitors per channel and can sample the waveform at a GHz rate. Four channels of a chip are cascaded to obtain deeper sampling depth with 4096 capacitors. After a trigger is generated in a mezzanine on the board, the waveform stored in the capacitor array is subsequently digitized with a low speed (33 MHz) ADC and transferred via the FPGA-based Gigabit Ethernet to a data acquisition system. Both a low power consumption (2.64 W per channel) and high speed sampling with a bandwidth of >300 MHz have been achieved. In addition, in order to increase the dynamic range of the readout we adopted a two gain system achieving from 0.2 up to 2000 photoelectrons in total. We finalized the board design for the first LST and proceeded to mass production. Performance of produced boards are being checked with a series of quality control (QC) tests. We report the readout board specifications and QC results.

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## 1. Introduction

Very high energy (VHE) cosmic gamma rays provide clues of understanding the origin of cosmic rays, the mechanism of particle acceleration around black holes and the nature of cold dark matter. The imaging atmospheric Cherenkov telescopes (IACTs) are nowadays the standard detectors for VHE gamma rays. Multiple telescopes take a Cherenkov-light stereoscopic image of an extensive air shower (EAS) induced by a gamma ray entering the atmosphere. The Cherenkov Telescope Array (CTA) is the next generation VHE gamma-ray observatory. The Large-Sized Telescope (LST) [1] has a 23 m mirror dish and targets 20 GeV – 1 TeV gamma rays. Its camera has 1855 photomultiplier tubes (PMTs) as photon detectors. With its large mirror dish, the night sky background (NSB) photons are also detected at a rate of several hundreds MHz per pixel. On the other hand, the duration of the Cherenkov light flash is only a few nanoseconds. In order to suppress NSB contamination to shower images and to improve the signal-to-noise ratio, it is necessary to sample the signal waveform at rate of  $\sim 1$  GHz and to reduce the signal integration time down to a few ns.

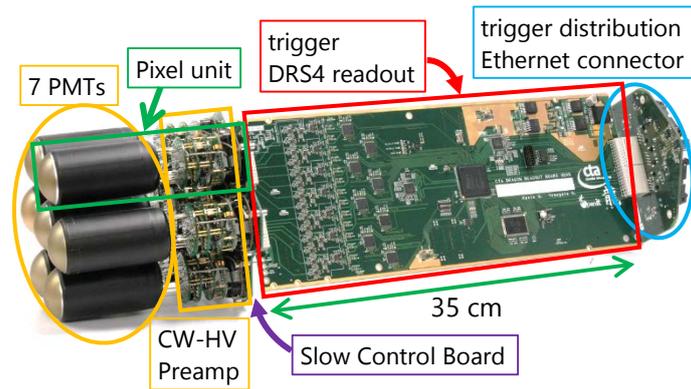
However, a GHz flash analog-to-digital converter (FADC) is in general expensive and has a high power consumption with large heat dissipation. On the other hand, the “DRS4” chip [2], which is an application specific integrated circuit (ASIC) of switched capacitor arrays (SCAs), can sample at a rate of GHz with low power consumption. We have developed a readout board adopting the DRS4 and have demonstrated that it can properly digitize the fast PMT signal. We report the design and the performance of the final version of the readout board to be installed in the camera of the first LST.

## 2. Design of the readout system

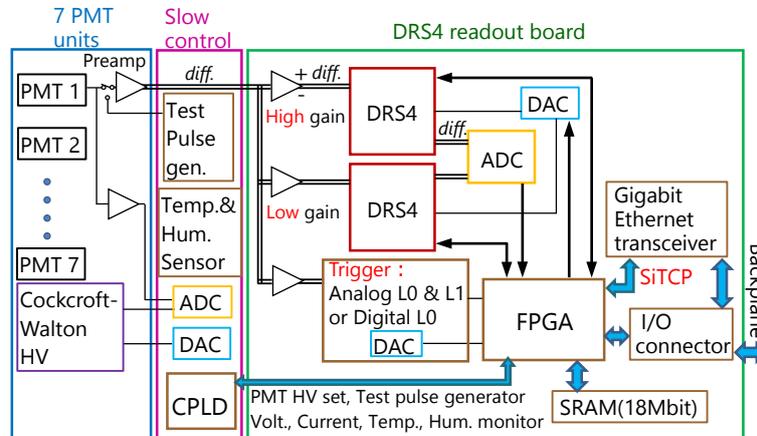
### 2.1 Overview

The focal plane camera of the LST has 1855 PMT pixels and consists of 265 modules with seven pixel units each. Figure 1 shows a photograph of a 7-PMT module to be installed in the camera of the first LST. The 7-PMT module consists also of a slow control board (SCB) [3], a DRS4 readout board and a backplane board which has several connectors for the +24 V power supply and for interfaces with other external modules. Each pixel unit is composed of a PMT, a Cockcroft-Walton high voltage supply circuit and a preamplifier ASIC named PACTA.

Figure 2 shows the block diagram of the readout system. On the DRS4 readout board, each signal from the PACTA preamplifiers is divided into three lines: a high gain line, a low gain line and a trigger line. The high gain and low gain signals are sampled by the DRS4 chip at a 1 GHz rate. When a trigger signal is generated, the stored waveform is digitized by an external slow ADC at a rate of  $\sim 33$  MHz. The digitized data is then sent to a field programmable gate array (FPGA) and transferred to the data storage server through the backplane board and switches via the Gigabit Ethernet transceiver. This technology of transmission of waveform data and slow control is available by implementing SiTCP [4] on FPGA. The Xilinx Spartan-6 FPGA controls eight DRS4 chips, a 12-bit ADC, a static random access memory (SRAM) which can store 18 Mbits of data and a digital-to-analog converter (DAC) used for correction of the input and output ranges of DRS4s.



**Figure 1:** Photograph of a 7-PMT module to be installed in the camera of the first LST.



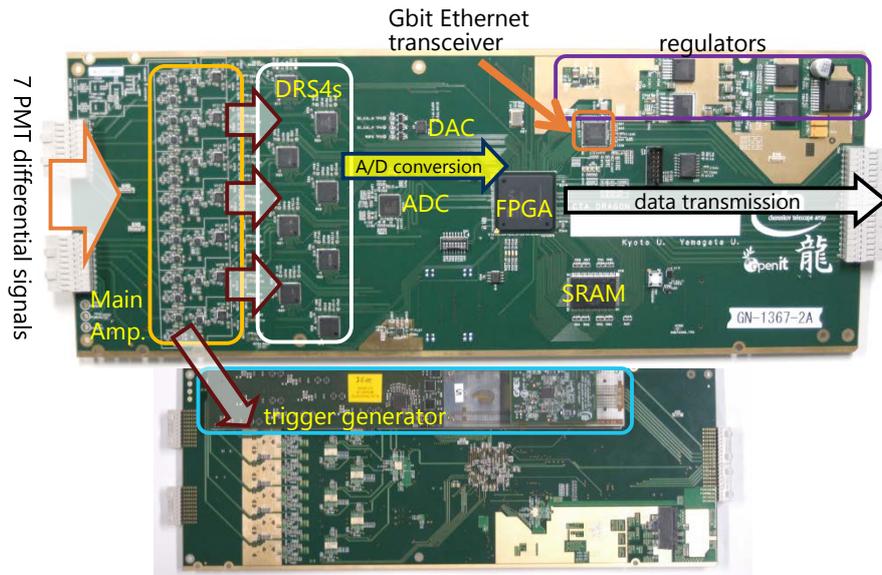
**Figure 2:** Block diagram of a 7-PMT camera module.

In addition, it communicates with a complex programmable logic device (CPLD) on the SCB and a FPGA on the backplane board via serial peripheral interface (SPI).

Figure 3 shows a photograph of DRS4 readout board with a size of 35 cm  $\times$  13.6 cm. A SCB and a backplane board are connected to the left and right side connectors respectively. The power consumption per channel without pixel units is 2.64 W. It has four connectors as the interface to mezzanine boards of trigger generator circuit. Details of the parts on the board are described in the following subsections.

## 2.2 DRS4

The Domino Ring Sampler (DRS) has been developed at the Paul Scherrer Institute (PSI), Switzerland, for the MEG experiment [5]. The latest version, DRS4, is also used in the MAGIC experiment [6]. The DRS4 chip has nine differential input channels with 950 MHz bandwidth and each channel has 1024 storage capacitors whose write switches are operated via a chain of inverters named domino wave circuit. The sampling speed can be changed from 700 MHz up to 5 GHz according to reference clock from the FPGA. In addition, a low noise level of 0.35 mV (rms) (after offset correction) and a low power consumption of 17.5 mW per channel at 2 GHz sampling



**Figure 3:** Photograph of front side (top) and back side (bottom) of the DRS4 readout board.

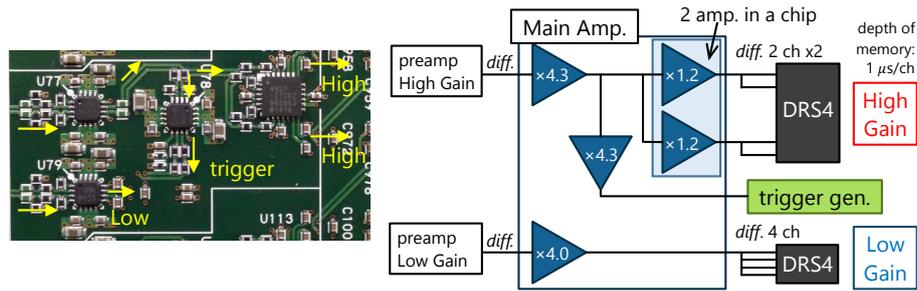
are demonstrated [7]. Eight DRS4 chips are loaded on the readout board and each chip is connected to two PMT channels. It is possible to cascade up to eight DRS4 channels for a deeper sampling depth. Cascading is realized in the following way; there is an 8-bit register in the chip, each bit of which corresponds to one DRS4 channel. A channel is activated only when the corresponding bit of the register is high. Connecting the same signal line to multiple DRS4 channels and activating them one after another, the sampling depth can be summed. For the readout board, four DRS4 channels are cascaded, which means the signal of each input is sampled in 4096 capacitors and the sampling depth is  $\sim 4 \mu\text{s}$  in the case of 1 GHz sampling.

### 2.3 Main amplifier

Figure 4 shows a photograph and a block diagram of the main amplifier on the DRS4 readout board. It is designed to achieve wide bandwidth of  $>300$  MHz and to have a dynamic range up to 2000 photoelectrons by using a high speed current feedback amplifier, Analog Devices ADA4927. Five amplifiers are used per PMT channel and two of them are integrated in one chip. As described above, in the readout board, four DRS4 channels are cascaded and thus, four identical signal lines per channel must be prepared. It was known from simulation that the bandwidth can be significantly improved by increasing the number of amplifiers dealing with the four signal lines because the capacitance load per amplifier is decreased. Therefore, the main amplifier of high gain PMT channels is designed so that four DRS4 channels are fed by two amplifiers.

### 2.4 Trigger mezzanines

There are two types of trigger logic; analog trigger and digital trigger. For the analog trigger, level 0 and 1 (L0, L1) mezzanine boards for trigger generation are mounted on the DRS4 readout board as shown at the bottom of Figure 3. The trigger circuit on the L0 mezzanine generates an analog waveform which is the sum of pulses from seven PMT channels. This pulse is distributed to



**Figure 4:** Photograph of the main PMT channel amplifier (left) and block diagram showing its interfaces (right).

the L1 mezzanines on neighbor modules by a backplane board. On each L1 mezzanines, the pulses from a backplane board are summed up and discriminated. By this method, the energy threshold can be decreased. On the other hand, for the digital trigger, only a L0 mezzanine board is mounted. PMT signals are discriminated pixel by pixel and backplane boards make the decision to trigger by a geometrical pixel hit pattern. The readout board is compatible with both trigger types, which can be exchanged by simply replacing the mezzanines.

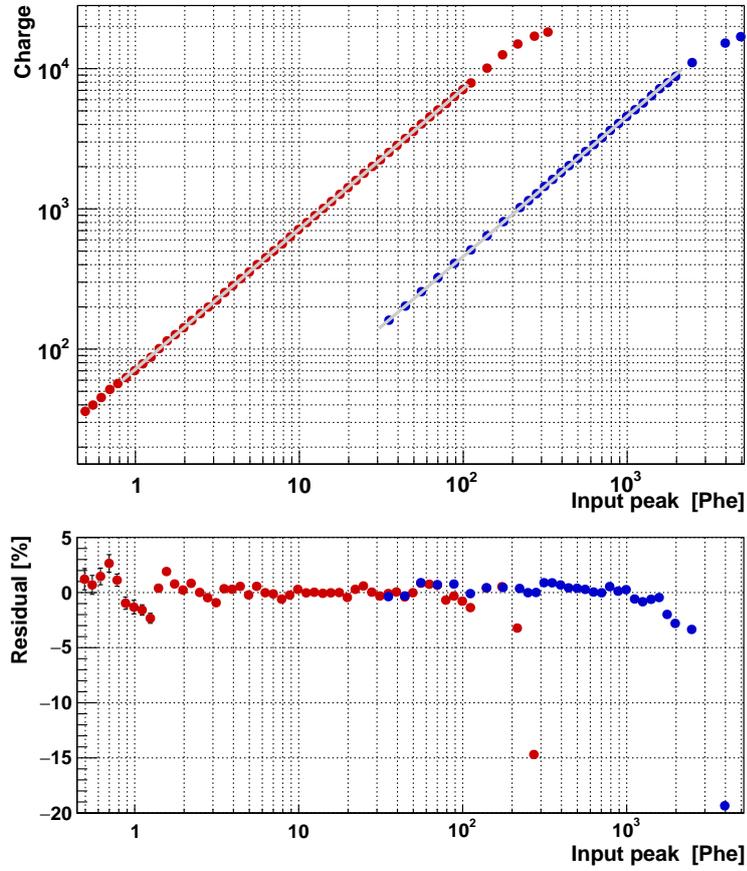
### 3. Performance of the readout system

#### 3.1 Fundamental performance

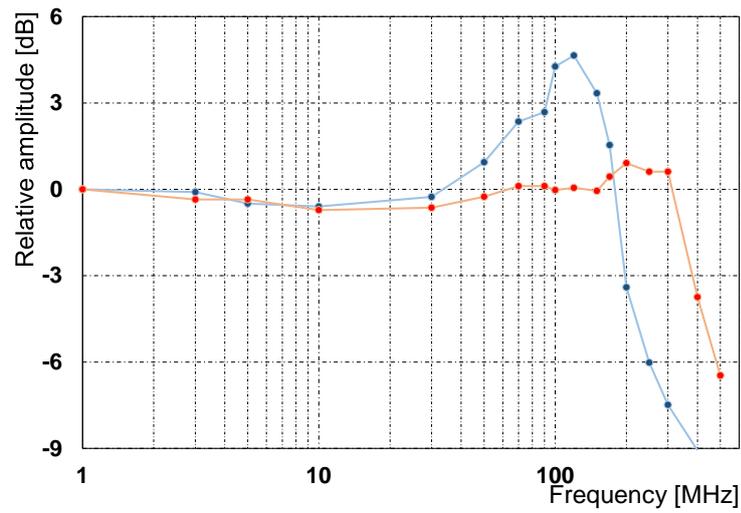
We have evaluated the performance of the DRS4 readout board and several results of measurements are shown below.

First, we evaluated the main amplifier. Dynamic ranges of high-gain and low-gain lines are shown in Figure 5. It is demonstrated that linearity within 5 % is totally guaranteed from below 1 up to  $>2000$  photoelectrons. Figure 6 shows the bandwidth of the high gain and low gain lines. The high-gain line achieves a bandwidth of  $>300$  MHz, which is wide enough to measure Gaussian like waveforms with a full width at half maximum (FWHM) of as fast as 2 ns. On the other hand, the low gain line achieves  $\sim 180$  MHz. Since this channel processes signals significantly larger (more than 30 photoelectrons) than typical NSB, this bandwidth limitation is not considered a relevant shortcoming.

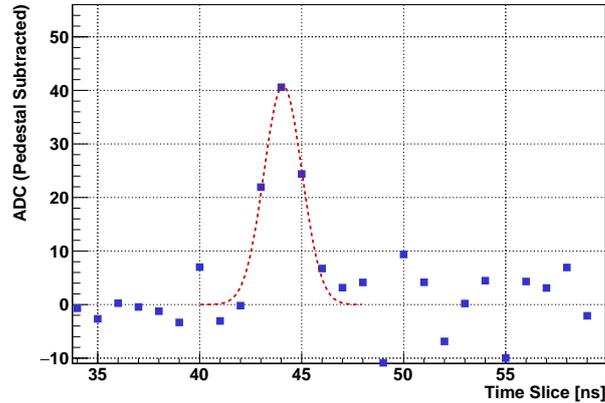
We also performed measurements of signals from a PMT via the SCB. Figure 7 shows a pulse waveform of a single photon signal from a PMT sampled by the DRS4 readout board at a rate of 1 GHz. It was measured with weak light from a LED and with a PMT gain of 40000. As shown in the figure, we successfully digitized the PMT signal with a FWHM of 2–3 ns. We analyzed the waveform data and created a single photoelectron charge distribution (Fig. 8). As shown in the figure, the single photoelectron peak is clearly seen. Both the pedestal peak and single photoelectron peak are fit by Gaussian distributions, and the signal-to-noise ratio, defined as (single-photoelectron mean – pedestal mean) / pedestal rms, is calculated to 5.26. In addition we also measured the time jitter of test pulses from a trigger and determined that it is lower than  $\sim 1$  ns (rms) at a sampling rate of 1 GHz.



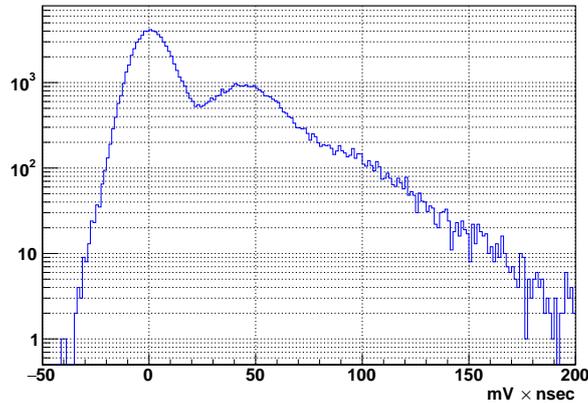
**Figure 5:** Dynamic ranges of high (red) and low (blue) gain lines of the DRS4 readout board (top) and residuals between measured values and the fit line (bottom).



**Figure 6:** Bandwidths of high (red) and low (blue) gain line.



**Figure 7:** Pulse waveform of a PMT single photon signal sampled by the DRS4 readout board at a rate of 1 GHz.



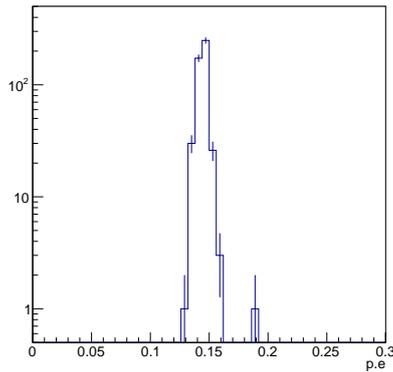
**Figure 8:** Charge distribution of single photoelectrons. The horizontal axis is in units of  $\text{mV} \times \text{ns}$ .

### 3.2 Quality control results

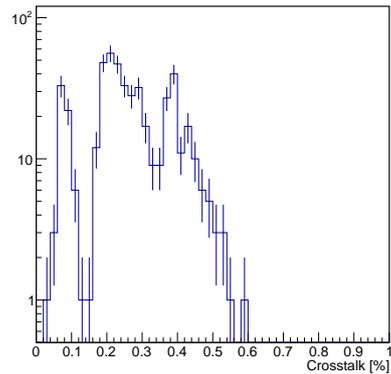
We have started to mass-produce  $\sim 300$  readout boards in total for the first LST. 69 boards have been produced by now and submitted to the LST quality control process. Figure 9 shows a distribution of amplitude rms of zero-signal events. As shown in these figures, the noise level of all boards is less than 0.2 photoelectrons. Figure 10 shows the distribution of the maximum crosstalk levels for the tested channels, which are measured by the test pulses injected from the SCB. All of them showed levels below 0.6 %. In addition, non-linearity of all boards is less than  $\pm 5\%$ .

## 4. Conclusion

We have developed and completed a readout system to be installed in the first Large-Sized Telescope of CTA. We demonstrated that it can successfully sample waveforms of a PMT by using the analog memory ASIC DRS4 chips at a 1 GHz rate. It achieves a low power consumption of



**Figure 9:** Distribution of noise for all channels of 69 quality checked boards, which is defined as amplitude rms of zero-signal events. The horizontal axis is in units of photoelectron.



**Figure 10:** Distribution of biggest crosstalk levels for all channels of 69 quality checked boards. The horizontal axis is in units of percentage to input amplitude of neighbor channels.

2.64 W/ch, a wide bandwidth of  $>300$  MHz at high gain line, and a wide dynamic range from below 1 up to 2000 photoelectrons.

## Acknowledgments

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## References

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