The IceCube Generation-2 Digital Optical Module and Data Acquisition System

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With recent exciting observations of astrophysical TeV- to PeV-energy neutrinos and new competitive measurements of GeV-energy atmospheric neutrino oscillations in the IceCube neutrino observatory at the South Pole, the design of a second generation Antarctic neutrino observatory, IceCube–Gen2, is underway. The design calls for two new instrumented volumes, one a denser in-fill array to extend the sensitivity of IceCube to energies low enough to gain sensitivity to the neutrino mass hierarchy, and one approximately ten times larger than IceCube, about 10 cubic kilometers in extent, to improve the sensitivity of IceCube to high energy astrophysical neutrinos and their sources. The detectors will share many common hardware elements and will leverage the successful hardware and software of the first generation experiment. They will feature updated data acquisition electronics using commercially available components and taking advantage of advances in embedded computing power. We describe the status of the modernized in-ice Digital Optical Module (DOM) and the supporting surface electronics and data acquisition components.

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1. Introduction

With the recent observations of TeV astrophysical neutrinos and very competitive measurements of atmospheric neutrino oscillations, there is interest in adding onto the IceCube detector to increase its acceptance by a large factor. IceCube's Digital Optical Modules (DOMs) were quite successful and form the basis of the design for a new generation (Gen2) DOM, taking particular advantage in improvements in fast, low power digitizers and programmable logic while retaining the proven overall design of the first generation DOM and many of the remaining available parts. The Data Acquisition (DAQ) system consists of the hardware modules that read the DOM data after cable transmission, and aggregate that data onto Ethernet for online (software) triggers and filters that can request detailed readouts of the DOMs through the same hardware. The Gen2 surface hardware readout system will be backwards compatible with the original IceCube DOM readouts, but will be able to be deployed either indoors or outdoors at the top of the detector strings. Additionally, a major design goal will be a decreased physical footprint in the surface building.

PINGU and the High Energy Array extensions to IceCube have decidedly different physics goals, but will have a nearly uniform hardware implementation at the DOM level[2, 3]. Detector module spacing and triggering allow for the vastly different physics objectives. With the common design elements, an overall philosophy of Gen2 IceCube DOM and DAQ development is to keep as much commonality as possible, keep as much of the IceCube hardware heritage in place, but gain from electronics developments in the decade since the IceCube hardware design was frozen. Research and development for the Gen2 detector elements has been progressing over the last year and a half or so, and now has hardware samples of much of the detector signal chain, though in lab-only physical formats, and with some of the elements yet to be implemented. Near future development will continue with the goal of increased integration and the ability to have reasonable detector hardware in hand ahead of, and in support of, a funding proposal.

2. Digital Optical Modules

The IceCube DOM evolved from the earlier AMANDA analog optical module with primary goals of high-reliability, accurate waveform digitization, and flexibility in surface readout [1]. The primary design differences between first and second generation DOMs are highlighted in Fig. 1. The analog delay required for the first generation digitizer is eliminated, and there is an overall simplification and consolidation of the electronics, while the mechanics remain very faithful to the original proven design.

High level requirements for the DOMs include a sampling rate of >160MSaps in order to adequately digitize the PMT pulse, data transmission rate of greater than 1 Mbps, absolute time discrimination on the order of 1–2ns, power consumption of <4W (IceCube actual) and ideally <2W per DOM, and dynamic range to cover from at least 1/25 of a single photoelectron (SPE) up to about 425 SPE for PINGU (perhaps higher for the high energy extension). The dynamic range available is being investigated including the possibility of dynamic pulse compression.

The overall system architecture of the Gen2 DOM is shown in Fig. 2. In all cases, we show the baseline hardware design in this paper; however, there are alternate technologies, chip selections, and firmware paths under investigation with final trade studies to take place through system
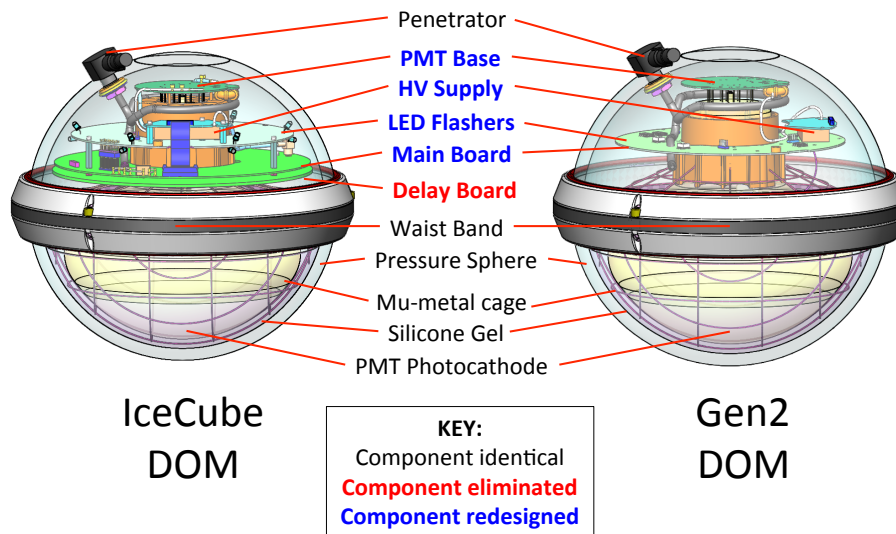
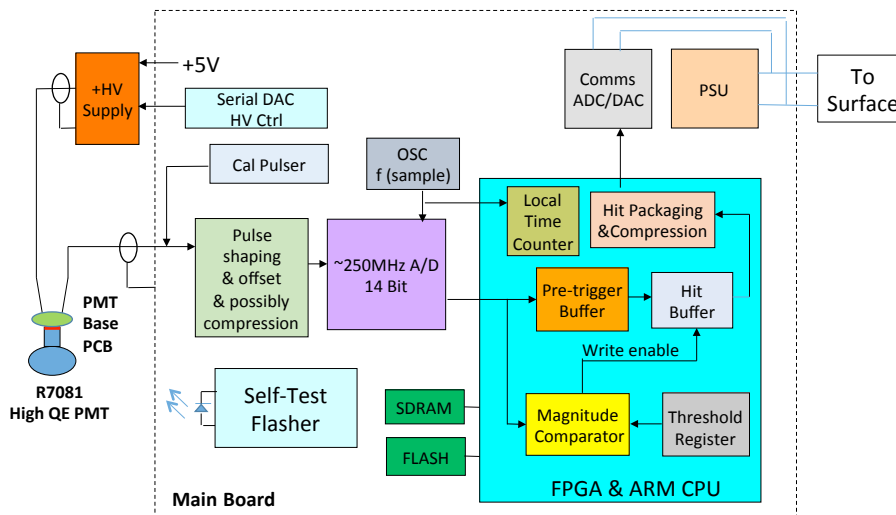Figure 1: A comparison between the current IceCube DOM (left) and the Gen2 DOM (right).

Figure 2: Block diagram of the of the Gen2 DOM mainboard.

and subsystem reviews. The 10" High Quantum Efficiency (HQE) photomultiplier tube (PMT) is readout through an analog front end that shapes the signal, performs anti-alias filtering, centers the unipolar PMT pulse into the bipolar ADC window, and drives the input of the digitizer. The PMT remains the same as used in IceCube ([6]), the Hamamatsu R7081-02. Alternate arrangements of smaller PMTs ([7]), dual PMTs with high transparency windows ([8]), or custom-constructed wavelength-shifting optical modules ([9]) are also under consideration, though they too would couple into a DAQ architecture similar to what is presented here.

The digitizer is an ADS4149 250MSaPS pipelined ADC drawing about 250mW of power while continuously sampling the analog waveform with 14 bit (11.2 ENOB) resolution. This dynamic range is somewhat smaller than the 1/25 SPE to 425 SPE high-level requirement listed above.

This tension is under investigation with possible solutions including dual channels (high and low gain or anode and deep dynode tap), analog signal compression, or a loosening of the requirements. This is a deadtime-free system with the local triggering based on the digital output of the ADC. The FPGA takes the continuous waveform data and allows flexible triggering based on a simple voltage threshold or a number of samples over threshold. For IceCube-Gen2 array use we plan compression and/or feature extraction of single, and perhaps multiple, photoelectron hits within the onboard programmable logic.

A second version of the Digitizer Daughter Card (DDC2, see Fig. 3) for lab testing has been produced and is being operated in concert with a commercial evaluation kit for the FPGA chosen for this design. The readout noise for the combined analog front end and digitizer is consistent with the specification sheet for the ADS4149 (see Fig. 4) with intrinsic RMS noise of just over one bit.
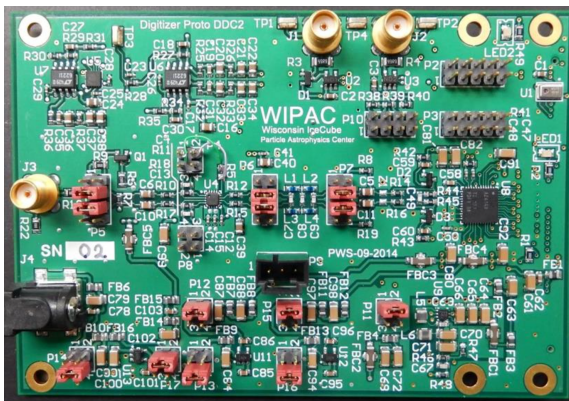

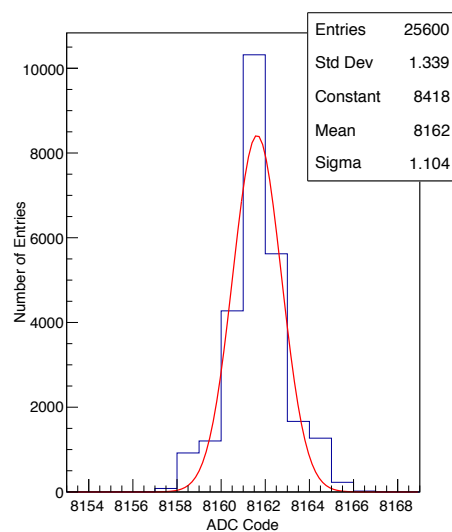Figure 3: The prototype Digitizer Daughter Card (DDC2).

Figure 4: Baseline ADC readout in the DDC2 (terminated).

As an alternative to the commercial PMT high voltage supplies tested for and used in the IceCube DOM, we have designed a prototype custom high voltage supply based on the UMHV ultra-miniature HV supply from HVM Technology (see Fig. 5). Power consumption ranges from 90 to 180mW depending on output voltage ($75M\Omega$ load). Stability and ripple characteristics are still under investigation.

Communications and absolute system timing are conducted over a minimum of 1.5km (top of the array to the surface) up to a maximum of 3.5km (in IceCube, from 2.5km depth and across the array) of copper quads. The timing system (RAPCAL) is carried over from IceCube and consists of reciprocal transmission and reception of test pulses coordinated with GPS timing at the surface [1]. Communications consist of dedicated logic-controlled ADCs and DACs, and are discussed below.

Figure 6 shows a block diagram representation of the firmware which was developed to read-out the DDC. The ADC-FPGA Interface module divides the incoming Double Data Rate (DDR) 250 MSaPS ADC data stream into four parallel Single Data Rate (SDR) streams, each running at 62.5 MSaPS. Dividing the data stream in such a way allows the design to easily meet all synchronous timing requirements, while making only modest tradeoffs in resource utilization and de-
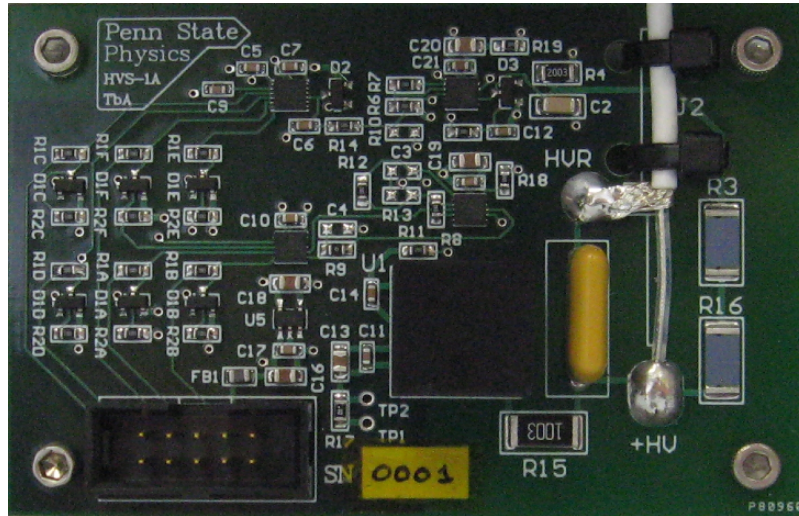
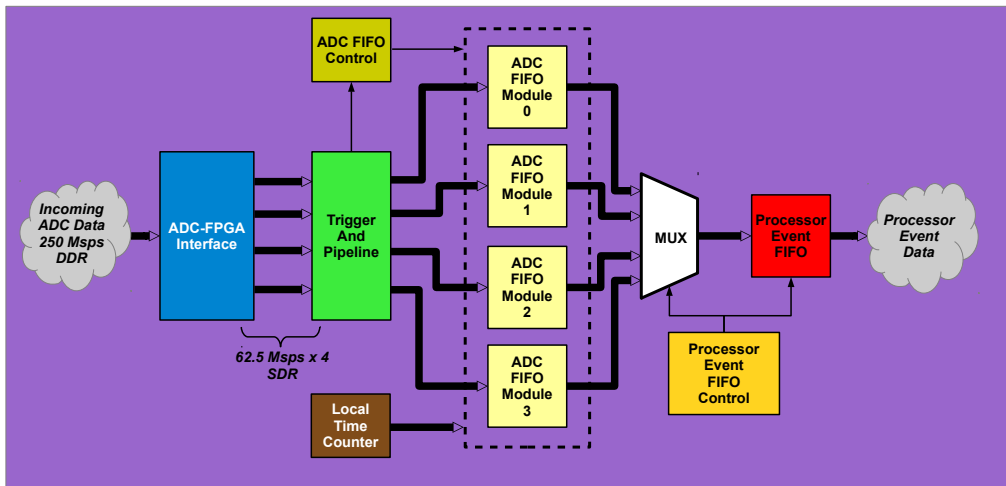Figure 5: Prototype high voltage supply (HVS) daughterboard.

Figure 6: Block diagram for the DOM firmware.

sign complexity. The Trigger and Pipeline module examines the data stream for the occurrence of any of a number of user-programmable trigger conditions, signaling the ADC FIFO Control module to begin filling the ADC FIFOs with event data when the active trigger condition is satisfied. A 48-bit timestamp generated by the Local Time Counter module is also stored with each event. Data on the output side of the ADC FIFOs is sequentially re-ordered by the Processor Event FIFO Control module and presented to the FPGA's processor for formatting and transmission to the user.

The DOM design also allows for ancillary sensor systems (provided they are low average data rate) such as cameras for inspecting the refrozen hole ice near the detector, acoustic sensors for 3D-imaging of ice fracturing, or novel radio detector systems (*e.g.*, [4]). This general interface includes 5VDC, 100mW power and an SPI or I2C local communications protocol along with handling of data through the remainder of the DAQ.

The DOMs are to be permanently embedded into the South Pole glacial ice, so their long-

term reliability must be high. The IceCube DOMs had a better than 99% survival rate in the ice, with the small number of failures typically occurring during or shortly after deployment. We will follow the program of extensive design verification and testing at the component, subsystem, and system levels. Most passive components are of automotive or military reliability specification. For example, the high voltage modules have been deployed in about 100,000 night vision goggle units used worldwide in a wide range of environments. Whenever possible, proven components and processes will be used.

3. Data Acquisition (DAQ)

The readout of the DOMs consists of two layers: a hardware DOM communications board with power and timing, and the computers that construct the triggers, filter data, and archive events. We focus on the DOM communications hardware, which in IceCube consists of a PCI interface and communications card (DOR) hosted with other DOR cards in a DOMHub that also includes the downhole power supply, timing connection, and a networked single board computer. The Gen2 design is backwards compatible with IceCube to allow for the replacement of the DOR/DOMHubs in time for both power savings and a smaller footprint in the IceCube Laboratory (ICL).

The communications for the Gen2 design are handled with a Communications Daughter Card (CDC); see Fig. 7. The essential features of the communications channel are the arbitrary firmware definition of the in-channel encoding supported by protection circuitry, DC bias for DOM power, and general purpose ADCs and DACs bridging cable distance. Full duplex power consumption for this circuit is less than 200mW which is less than a sixth the power of a typical (AD9869) modem chipset. Multiple CDC boards would live on a carrier card (backplane) with shared power supplies (CDC and downhole DOM), GPS timing connection, and mechanical mounting. See Fig. 8 for a diagram with existing IceCube patch cable connectors matched up with the new CDCs.
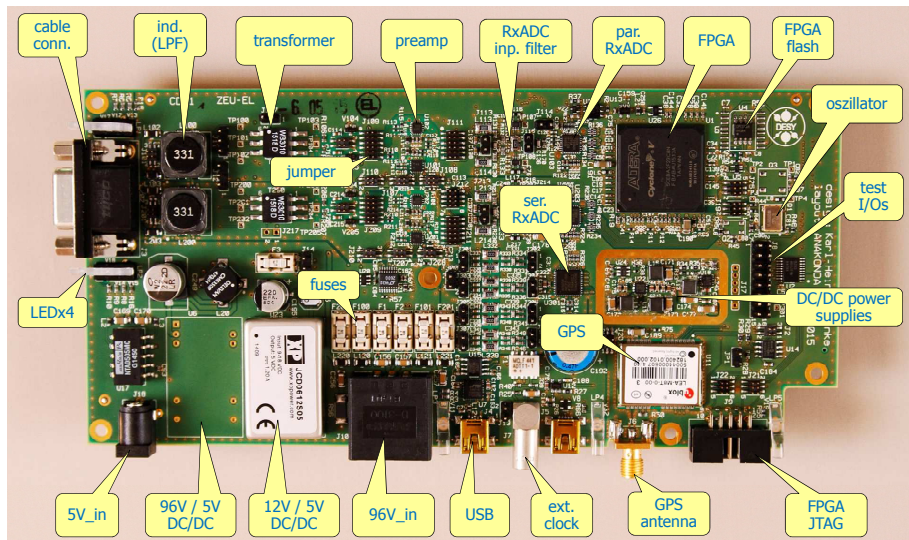

Figure 7: The Communications Daughter Card (CDC) prototype board.

In addition to compressing the physical layout of the DOM readout electronics which is important if $O(100)$ strings are added to the IceCube detector to avoid dramatic increases in counting
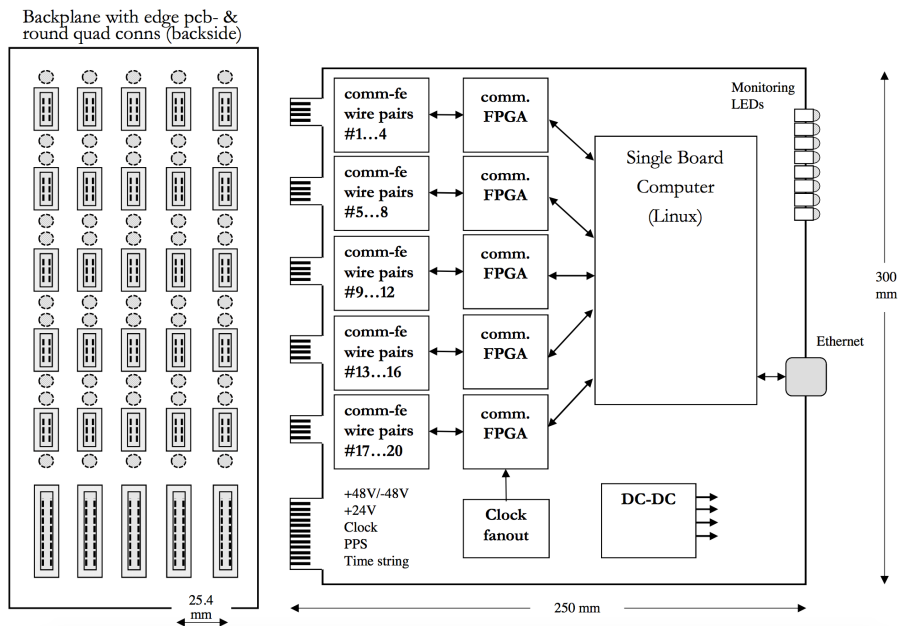
Figure 8: Readout architecture supporting a string of DOMs on a single card.

house space, strings at a significant distance from the counting house can be better managed with a String-Hub which resides outdoors (in an insulated vault) near the top of the string. For such remote installations, data transfer will be over fiber-based Ethernet and timing maintained through the use of the White Rabbit ([10]) protocol to the top of the string and RAPCAL down the string.

4. System Construction, Integration, and Deployment

The IceCube DOMs were built and tested at three distinct production facilities (DESY, Stockholm, and UW-Madison) ahead of shipment to the South Pole. All DOMs received extensive end-to-end testing including thermal stress and thermal soak in the Northern Hemisphere. DOMs will be transported in custom boxes that enable easy cable connections without removing the housing from the box. Final testing is performed before unpacking and preparations for deployment. Nonconforming materials are shipped back to the north for possible repairs.

Optical modules are deployed off of a custom Ericsson built cable consisting of cable quads, strength member, and outer jacketing. For the higher density PINGU strings, some differences in attachment method are foreseen. Fig. 9 shows a comparison of the mechanical string/cable to DOM mounting hardware. The mounting approach, with the string temporarily relaxed during DOM connection, also allows for the attachment of "special devices," non-DOM detector elements which might include, for example, direct dark matter detectors or ice optical propagation study devices (e.g., [5]).

5. Conclusions

Gen2 IceCube DOMs and DAQ components are well past the conceptual design stage and hardware is being prototyped and tested. These efforts aim to shorten the development time line
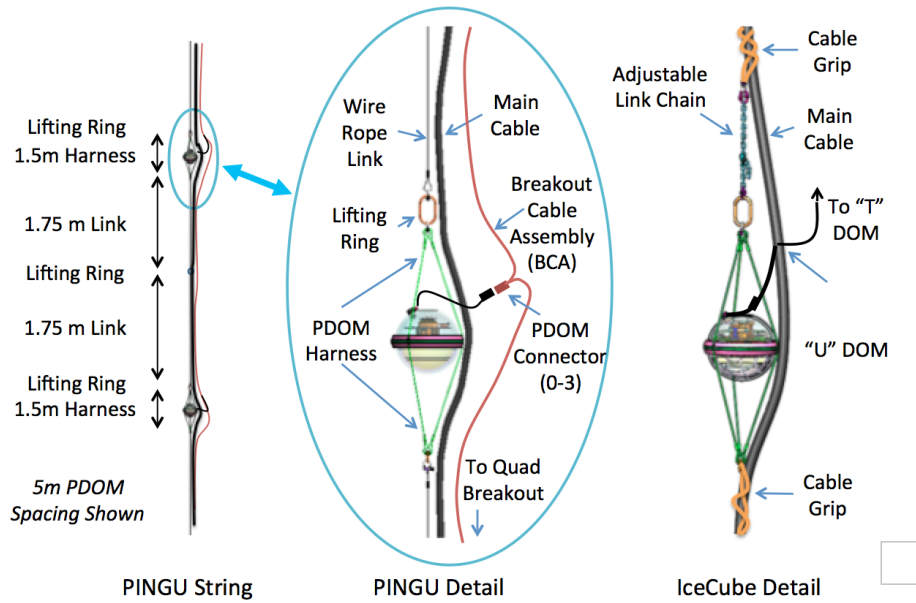
Figure 9: Current and planned DOM mounting strategies.

for both PINGU and the IceCube High Energy Array detector systems, leveraging prior successful developments while also taking advantage of more recent electronics developments.

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