PROCEEDINGS OF SCIENCE

New electronics for the surface detectors of the Pierre Auger Observatory

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The surface detector array of the Pierre Auger Observatory consists of 1660 water Cherenkov detectors that sample the charged particles and photons of energetic cosmic ray air showers at the ground. In the framework of the planned upgrade of the Auger Observatory, AugerPrime, new electronics has been designed for the surface detectors. The electronics upgrade includes higher sampling frequency, increased dynamic range, increased processing capability, improved timing with up-to-date GPS receivers, and a better calibration and monitoring system. It will also process the data of the additional scintillator detectors planned for the upgrade.

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1. Introduction and design objectives

The surface detector of the Pierre Auger Observatory, located near Malargüe, Mendoza, Argentina, consists of an array of 1660 water Cherenkov detectors. The Auger Collaboration is planning an upgrade of the detector that includes the addition of a scintillator-based surface detector (SSD) atop each water Cherenkov detector (WCD), together with an upgrade of the surface detector electronics (SDE) to both improve the performance of the existing detector and provide an interface to allow the scintillator detectors co-located with the surface detector stations to make use of the data processing and communications infrastructure of the stations. The SDE records the tank signals, makes local triggering decisions, sends timestamps to the central data acquisition system for the global triggers, and stores event data for retrieval when a global trigger condition is satisfied. Because of the small bandwidth (1200 bits/s) available to each tank, the station must operate semi-autonomously, performing calibrations and taking action in response to alarm conditions at the station level. The current SDE was designed 15 years ago using the technology available at that time. Evolution in processors, power consumption of electronics components, and timing systems makes it possible today to design and implement a higher performance electronics system for the surface detector array. The design of the current detector and its electronics is discussed in [1].

The design objectives of the SDE upgrade are to improve the data quality through faster sampling for ADC traces, better timing accuracy, and increased dynamic range, and to enhance the local trigger and processing capabilities using a more powerful local station processor and FPGA. We will also improve calibration and monitoring capabilities of the surface detector stations. Backwards-compatibility with the current data set will be maintained by retaining the current time span of the PMT traces and providing for digital filtering and downsampling of the traces to emulate the current triggers in addition to any new triggers. The design objectives also aim for higher reliability and easy maintenance. An important feature in the design of the upgraded SD electronics is a facility for interfacing not only the SSD but also any other additional detectors.

The upgrade will be implemented as a single board called the Upgraded Unified Board (UUB). The proposed upgrade comprises the role of the original the Unified Board (UB) and its front-end daughterboard in the current electronics. The interface board to the power system, the Tank Power Control Board, will not be upgraded, and the interface to the communication system will also remain unchanged.

2. Front-end electronics

The upgrade to the front end includes an increase of the sampling rate to 120 MHz from the current 40 MHz. The dynamic range will be increased by modifying the amplification scheme for the existing three large 230 mm XP1805 PMTs, adding a fourth small PMT (SPMT) to extend the dynamic range for large signals near the shower core.

The amplification of the XP1805 PMTs is modified to match the new dynamic range requirements and higher sampling bandwidth. The signal from the anode of the PMTs is split and the high-gain channel is amplified by using a dual-channel low-noise ADA4927 Operational Amplifier (OA) yielding an amplification of about a factor of five. Signals are filtered by a 5-pole lowpass filter using discrete passive inductors and capacitors. A second amplification stage is implemented

by using another ADA4927 OA to obtain a total amplification of 30 dB corresponding to a voltage amplification factor of about 32 for the high-gain channel. The low-gain channel is buffered and filtered. The signals are digitized by commercial 12 bit 120 MHz differential-input D9628 FADCs, which achieve this performance with low power consumption, an important consideration due to the 10W station power budget. The pulse response of the PMT, when expressed in terms of bandwidth, is ∼70 MHz. This is well matched to a 120 MHz FADC and associated 60 MHz Nyquist filter. A block diagram of the design is shown in Fig. 1.

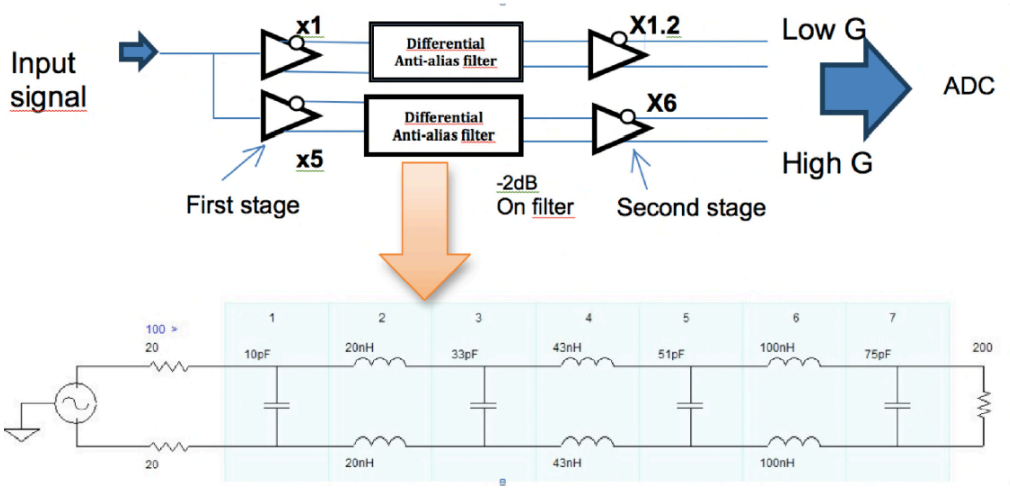

Figure 1: Block diagram of the front-end electronics.

The large PMTs in the WCD deviate from linearity for peak currents in excess of ∼50 mA. Conservatively assuming a maximum current of 40 mA, the corresponding maximum signal in the WCD before saturation, for an operating gain of 3×10^5 and a single vertical equivalent muon (VEM) peak signal of ∼100 photoelectrons, is ∼600 VEM. This is well-matched via standard 50 Ω termination resistors to the 2V input range of the front end digitizers. The full XP1805 signal range of 600 VEM is then conveniently mapped into a full 17-bits digital range by using the high-gain channel for single VEM resolution, and the low-gain channel for larger signals, each spanning 12 bits with 7 bits of overlap. In such a configuration a single bit in the high-gain FADC corresponds to an anode current of ∼0.3 μA. The WCD dynamic range is further extended by another 5 bits using the SPMT signal, the gain of which is tuned to have a signal 32 times smaller with respect to the anode, corresponding to 600×32 VEM. The SPMT gain and its overlap with the larger PMT signals can be modified, and the overall dynamic range can comfortably exceed 40 kVEM.

The global dynamic range for the WCD PMT signals is shown in Fig. 2. The signal from the large PMT, operated at the current gain of 3×10^5, is split into an amplified *HighGain* range for single muon resolution and a *LowGain* range for measurements of shower signals. Events closer to the core have a larger signal that is collected by the small PMT and input into a dedicated *VeryLowGain* range. The dynamic range scheme will allow moving the trigger threshold two bits higher and increasing the current dynamic range by a factor of 32 and up to 20 kVEM. The muon peak will be in channel 200. An improved LED system will be used to aid in calibration of the system.

Range	Intent	Dynamic Range																					
bits		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22
HighGain	VEM	AnodeX32																					
LowGain	Showers						Anode																
VeryLowGain	Cores											SPMT											
Ipeak (mA)		0.0006					0.02		0.08			1.2						40					
Vpeak (mV)		0.03					1		3.9			64						2000					
Ipeak SPMT (mA)												0.02						1.25				40	
Vpeak SPMT (mV)												1						64				2000	
Npart (VEM)		0.01					0.3		1.2			10						600				20000	

Figure 2: WCD dynamic range. The maximum signal before saturation corresponds to 20k particles with the operating settings specified in the text.

3. Timing

Synchronization of the detectors is provided by disciplining a local clock using the Global Positioning System (GPS). For the upgraded electronics we have selected the I-Lotus M12M Timing GPS Receiver manufactured by I-Lotus, LLC (Singapore) [2]. The M12M Timing receiver is designed to be functionally compatible with the Motorola Oncore UT+ GPS receiver that is currently used within the Auger SDE Unified Board. Choosing a compatible unit means that fewer and simpler modifications to the basic time-tagging system design are needed. Specifically, the M12M provides the same 1 pulse per second (PPS) timing output with serial control and data. The specified intrinsic device accuracy after the applied "granularity correction" (the so-called "negative saw tooth") is about 2 nanoseconds. This accuracy is very good relative to the UUB specification to achieve better than 5.0 nanoseconds RMS accuracy.

The fundamental architecture of the time-tagging firmware module parallels the time-tagging design concept used in the original UB and is implemented in the UUB board FPGA. The on-board software for initialization of the time-tagging modules, GPS hardware control, and timing data is implemented on the original UB as a framework, forking changes and modifications as needed for the new UUB.

4. Slow control

A slow control system similar to that of AERA (the Auger Engineering Radio Array), incorporating a separate micro-controller (MSP430), will be used. There are sixty-four 0 to 5 V analog inputs, 16 logic IO's and eight 0 to 2.5 V analog outputs. The module also provides a USB serial connector. There are currently several free channels for test purposes and for additional detectors

such as the SSD. Additional water temperature and pressure sensors will also be implemented. Fig. 3 shows a block diagram of the slow control.

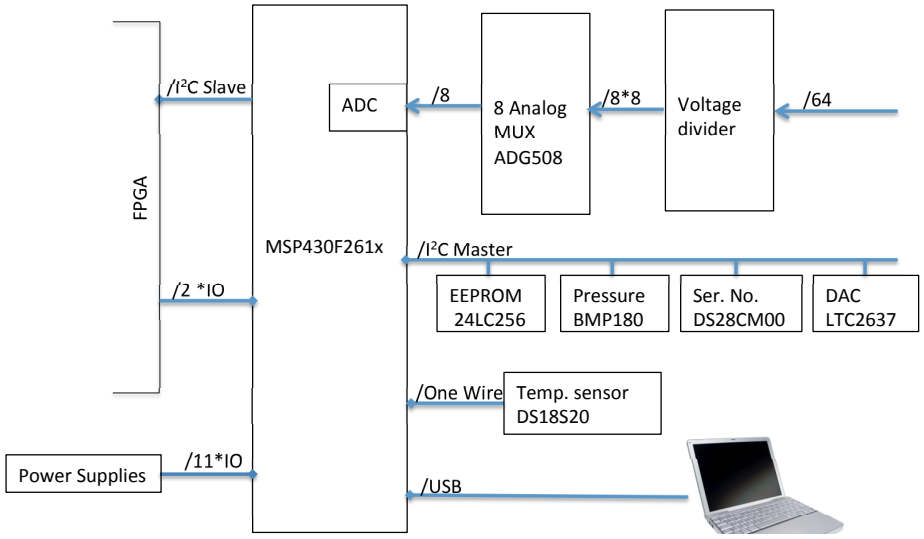

Figure 3: Slow control block diagram.

The slow control software provides access to more than 90 monitoring variables. These include currents and voltages of the subsystems of the UUB, environmental sensor values and PMT currents and voltages. Also the PMT high voltages are controlled by the slow control. For maintenance there is a human interface implemented via USB serial connection. In case of trouble, the microcontroller can be instructed by the COMMS to perform a complete UUB reset. Care is taken in monitoring the solar power system, and in the case of battery under-voltage, some parts or all components of the UUB may be switched off.

5. Upgraded Unified Board

The functionality described is implemented on a single board, called the Upgraded Unified Board. The architecture of the UUB includes a Xilinx Zynq FPGA with two embedded ARM Cortex A9 333 MHz micro-processors, 4 Gbit LP-DDR2 memory and 2 Gbit Flash memory (storage memory). The general architecture is shown in Fig. 4.

The processor manages the front-end electronics, slow control, LED controller, GPS receiver, clock generator, memory and various connectors. Two digital connectors are provided for future additional detectors. These connectors provide 8 differential lines, each of which can be individually defined as input or output in the FPGA. An example of an allocation that might be selected is: Trigger out, Clock out, PPS out, Busy in, Data in, Sync in, Data out, Sync out, etc. Moreover, this connector will provide unregulated +24 V, switched, limited, with a current monitor. The addition of accessible trigger IN/OUT and GPS 1 PPS signals will simplify time synchronization with future detectors. High speed USB interfaces and direct connection to the trigger FPGA will allow interfacing a variety of additional detectors.

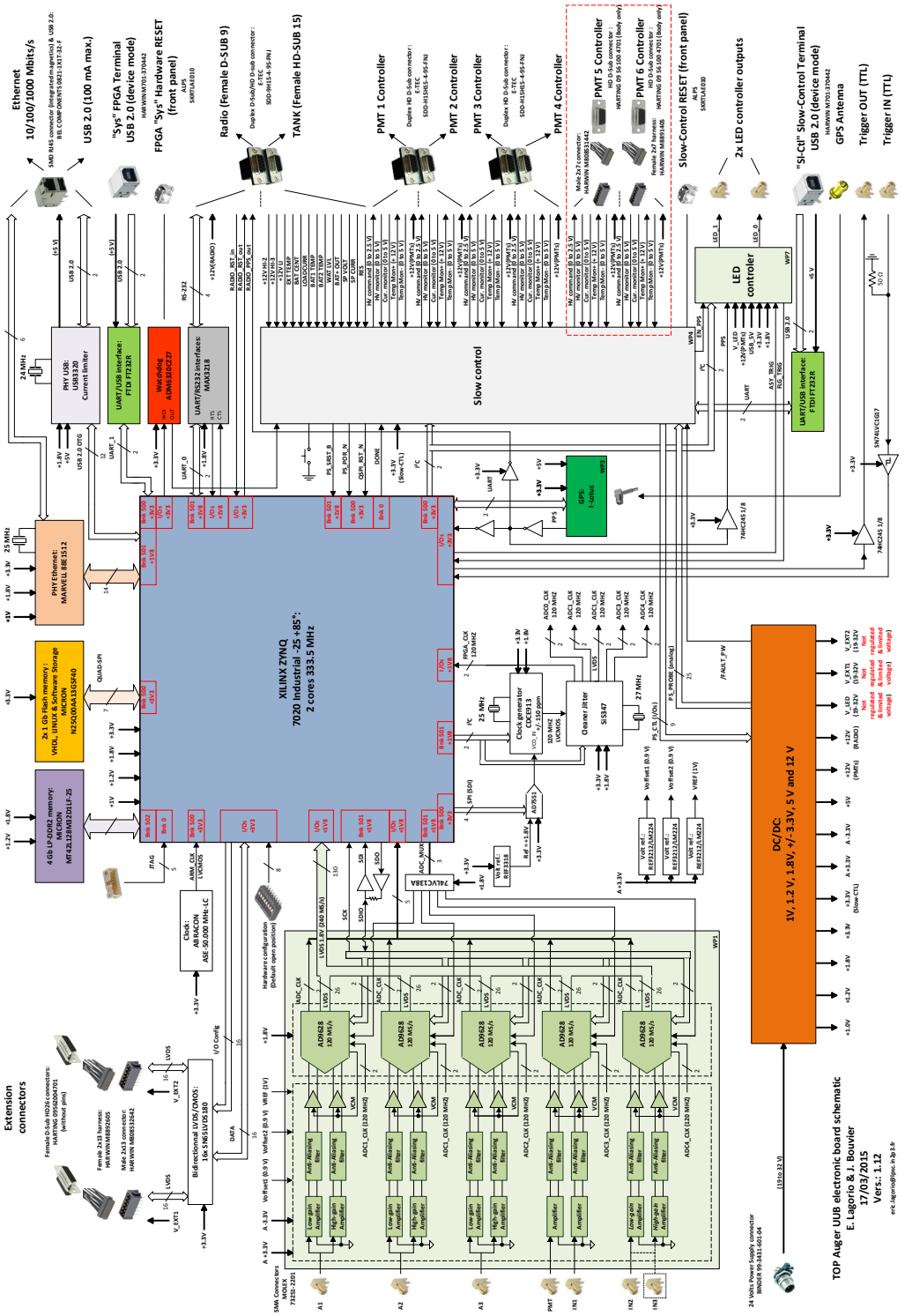

Figure 4: Architecture of the Upgraded Unified Board.

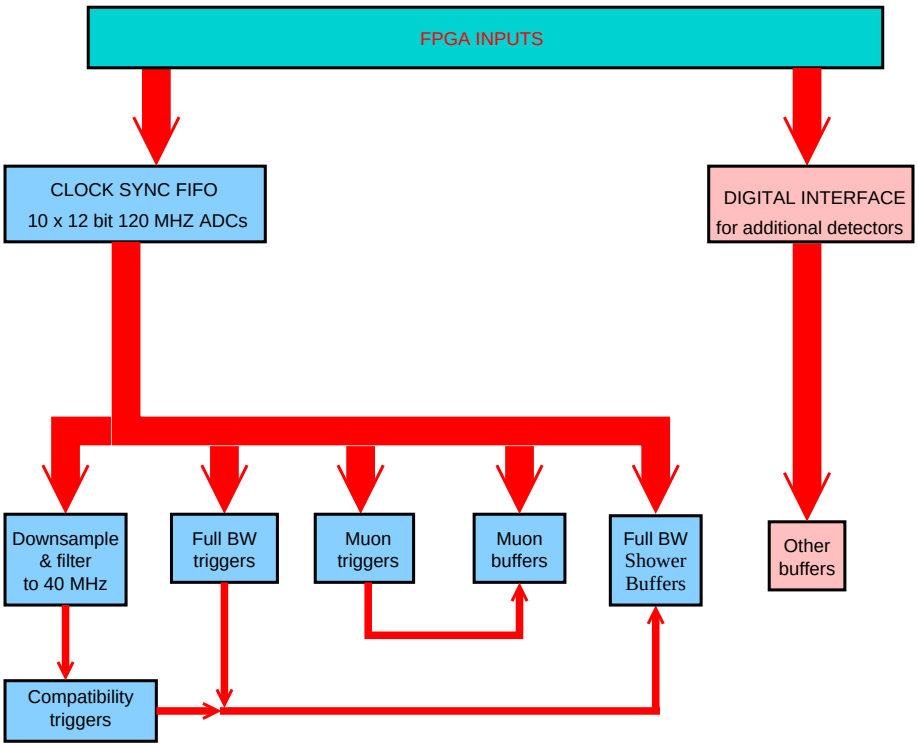

Figure 5: Conceptual diagram for local trigger.

The estimated peak power consumption (including radio and PMTs) is about 16 W. This is similar to the peak power of the current electronics running with an average power below 10 W. More accurate estimation of the power consumption will be done with the integrated prototype.

The design is being implemented on a 10 layer PCB board having the same size as the current UB board ($340 \times 240 \times 1.8$ mm). Global specifications for the components are: availability until 2020, operating temperature range from -20 to $+70^{\circ}$C, and preferably surface-mounted packaging. A conformal coating will be used to protect the UUB board. The UUB will be installed in the current RF-enclosure, only the front panel will be changed. This will allow a smooth mechanical integration of the electronics kit between the radio and the tank power control board under the current weather enclosure.

6. Local trigger and data acquisition system

The existing UB software will be ported to Linux and will be implemented in the FPGA. The data acquisition will be simplified by extending the use of FPGA firmware. The trigger and time tagging functionalities will also be implemented in the FPGA. The upgraded CPU will be >10 times faster than the current one, with a commensurate increase in memory. This will allow much more sophisticated processing in the local station.

The current local triggers (threshold trigger, time-over-threshold trigger (ToT), multiplicity of positive steps (MoPS) trigger, etc.) will be adapted to the 120 MHz sampling rate. The increased local processing capabilities will allow new triggers to be implemented such as asymmetry based

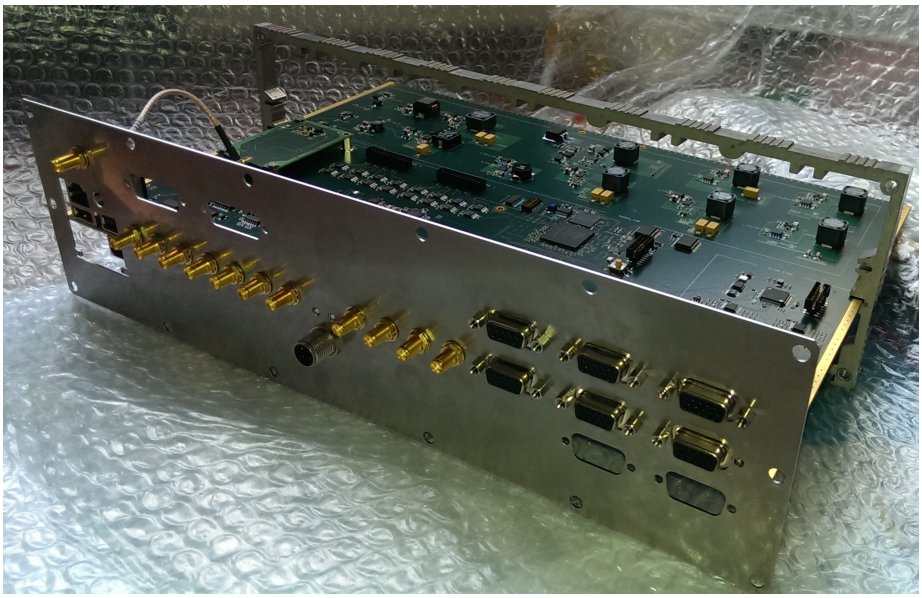

Figure 6: A prototype UUB attached to its front panel

triggers, and combined SSD and WCD triggers. The current muon memories and scalers will be retained. GPS synchronized LED pulses will be implemented which will improve calibration and monitoring of the detectors. The trigger scheme includes the ability to downsample and filter the data to the current 40 MHz rate which will facilitate the detectors to run with new electronics emulating the current detectors. This will allow deployment of new electronics during the maintenance of the current system without disturbance to the data taking. Fig. 5 shows a conceptual diagram of the local triggers.

7. Conclusion and Outlook

The upgraded Auger electronics will provide much higher performance in computing power, memory size, timing and sampling frequency. It integrates also an extra SPMT to extend the dynamic range, and will support the PMTs of the SSD. Initial prototypes are now undergoing testing (Fig. 6). About ten electronics prototypes are scheduled for deployment at the Observatory in early 2016. Together with the new SSD they will record physics data to verify the expected performance and pinpoint possible problems. We plan to complete the upgrade over the next three years.

References

[1] A. Aab *et al.* (The Pierre Auger Collaboration). *The Pierre Auger Cosmic Ray Observatory*. 2015. *Nucl. Instrum. Meth. A*, in press. [arXiv:1502.01323]

[2] "i-Lotus GPS" `http://www.ilotus.com.sg/m12m_timing_oncore`