

Real-Time Data Acquisition and Processing System Design for the ITER Radial Neutron Camera

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The Radial Neutron Camera (RNC) of ITER is a collimated multichannel neutron detection system intended to characterize fusion plasma neutron source. The RNC diagnostic plays a primary role in the ITER Program for advanced control measurements and physics studies. It also acts as backup system by providing machine protection and basic control measurements. The aim of ITER is to prove the viability of fusion as an energy source and to collect the data necessary for the design and subsequent operation of the first electricity-producing fusion power plant. The expected ITER pulse duration is up to 500 s in the inductive scenario. The demanding ITER operating conditions require a real-time Data Acquisition and Processing (DAQP) system that will acquire analog signals from the RNC detectors (e.g. scintillators, CVD diamonds, fission chambers) providing digital data through high performance networks to the ITER database. Two DAQP systems are expected to be used as prototypes for preliminary tests of performance: one based on PCI Express Extensions for Instrumentation (PXIe) and another one based on Advanced Telecommunications Computing Architecture (ATCA). The ATCA based system, with an architecture capable of withstanding a sustainable throughput of the order of 0.5 GB/s of data per channel, will be presented. The system features high performance Field Programmable Gate Arrays (FPGA) for every two 12 bits channels, sampling up to 1.6 GSPS and high performance host computers for every 4 channels through $\times 16$ PCIe 2.0 links. The criteria used for the choice of the components of both systems, ATCA and PXIe take into account: i) data throughput; ii) real-time data reduction; iii) compression, and iv) pulse processing. Finally, the expected data throughput performance of both architectures will be discussed.

First EPs Conference on Plasma Diagnostics - 1st ECPD

14-17 April 2015,

Villa Mondragone, Frascati (Rome) Italy

1. Introduction

The Radial Neutron Camera (RNC) of ITER is a collimated multichannel neutron detection system intended to characterize the fusion plasma neutron source. The RNC Diagnostic is now at the system level design phase. During this phase, the need for the procurement of critical prototypes must be justified. Prototypes that present technical challenges to be addressed before the construction of the final prototype are tagged as critical. Data acquisition electronics was identified as belonging to this critical group.

The RNC diagnostic, to be installed in the equatorial port plug 1, plays a primary role in the ITER Program for advanced control measurements, providing the neutron emissivity profile. It also acts as a backup system by providing machine protection and basic control measurements [1]. The proposed RNC measurement requirements [2] as well as the ITER demanding conditions urge for a high performance and high availability Data Acquisition and Processing (DAQP) system. Providing measurements in real-time during operation is mandatory for control and machine protection, either if the diagnostic acts as primary or backup. The expected ITER pulse duration is up to 500 s in the inductive scenario [3].

The RNC Concept Design Review foresees 28 Lines-Of-Sight (LOS) divided into In-Port and Ex-Port. The In-port LOS aims at covering the plasma edge while the ex-port LOS aims at covering the plasma core. Each LOS is expected to have at least 3 different detectors, to explore the widest range of measurements that can be provided by the RNC. The candidate neutron detectors, also identified as critical components, are: i) scintillators (with and without neutron / γ discrimination), ii) Chemical Vapour Deposition (CVD) diamonds, iii) fission chambers.

1.1 RNC Instrumentation & Control Project Overview

The ITER plant system I&C includes: i) plant control system, which provides local data acquisition, control, monitoring, alarm handling, logging, event handling and data communication functions; ii) plant interlock system, when a diagnostic provides investment protections functions, and iii) plant safety system, when a diagnostic provides nuclear and occupational safety functions. The RNC is defined to have only a plant control system [1]. The RNC plant control system may comprise the Plant System Host (PSH), Fast Controller (FC) and Slow Controller (SC). The SC used for measuring and activating slow Input/Output (I/O) channels (i.e. detector temperatures, magnetic fields, voltages and currents from detectors power supply) is not considered in this paper. The PSH provides asynchronous communication between the RNC plant control system and Control, Data Access and Communication (CODAC) System through the general purpose Plant Operation Network (PON). The PSH is in charge of command dispatching, state monitoring, data flow and configuration functions. The RNC control system architecture features one PSH.

The base of the ITER instrumentation for FC systems is stated in several living documents [4][5][6]. These documents define some criteria and requirements to follow during the definition of the architecture of the DAQP system acting as FC. Each RNC plant local control system will interface with ITER central I&C system through well-defined networks, remotely operated via CODAC System [4]. These networks are defined as CODAC Networks and includes High Performance Networks (HPN), which will be more detailed in the following section.

2. RNC Preliminary Fast Controller architecture

The RNC FC aims at acquiring the fast analog signals provided by the different types of RNC detectors, which are typically pulses with different amplitudes and time duration. The three main factors demanding a high performance FC are: i) the proposed RNC real-time measurement requirements for basic and advanced control, to provide fusion power density and neutron and alpha source profiles, respectively; ii) the availability of all data acquired from sensors to ITER central I&C Systems, with timestamp and without the support of local data storage; and iii) final stringent factor, the huge data production resulting from the expected ITER long pulse duration. In conclusion, the FC must be able to perform event detection, data processing, including event discrimination and data reduction in real-time, providing a system architecture with enough bandwidth for continuous data throughput. In addition, possible data throughput problems may occur: i) concerning all data acquired from a diagnostic, in an event base from the I/O chassis to host (CPU/Network chassis) and from host to the ITER data archiver; and ii) concerning real-time measurements for control purposes to High Performance Computers (HPC). Moreover, the expected sustained event rate is up to 2 MHz. Nevertheless, peak event rate above 1 MHz must be tested with real-time compression methods to reduce data.

Figure 1 depicts the proposed RNC preliminary FC architecture. The proposed architecture follows the ITER Plant Control Design Handbook (PCDH) rules [4]: i) the only physical interconnection between plant system I&C and central I&C systems is provided by seven networks; ii) FC shall be based on PCI Express (PCIe) I/O bus system, meaning that the I/O and the CPU/Network chassis are linked through a suitable PCIe link; iii) plant I&C computing and network resources shall provide sufficient margins to allow to have additional functions and increased data rates (scalability).

The ITER CODAC documentation defines seven network interfaces with different purposes and different performances. The PON uses a 1 GbE interconnection, while a set of specialized networks, the HPN, may use more demanding interfaces. RNC preliminary architecture design only uses 3 of the available HPN: i) the Synchronous Data Network (SDN) on a 10 GbE interconnect; ii) the Time Communication Network (TCN) which carries a Precision Time Protocol (PTP version 2, IEEE-1588-2008) allowing the client hosts to be synchronized with an accuracy of 50 ns Root Mean Square (RMS) to the ITER time, and iii) the Data Archiving Network (DAN), which must support the data production of the diagnostic (scientific data) using 10 GbE interconnection. The scalability of the DAN communication channel must be explored by the use of several parallel 10 GbE channels to sustain the high data rate production of the diagnostic. The content of this paper assumes that each 4 acquiring channels, subjected to 1 MEvents/s and to event width well defined with 128 points, will need 1 DAN link. If the event rate increases per channel and/or the number of samples per pulse width increases, more DAN links will be necessary per 4 channels.

Concerning SDN and DAN connectivity the market presents a dual port 10 GbE Adaptor for PCIe $\times 8$ solution, to be mounted on the host chassis. The number of 10 GbE links is limited by the number of $\times 8$ PCIe slots available on the host computer, which implies that one HPC is used per host. IO proposes a PCI Industrial Computer Manufacturers Group (PICMG) 1.3 based Personal Computer (PC) for this function. Therefore the RNC number of host computers will depend on the PICMG 1.3 PC PCIe slot capability and on the number of channels to acquire.

The PCIe connectivity can span from $\times 4$ to $\times 16$ lanes per link, which will be I/O chassis standard dependent. This will be discussed in the next section.

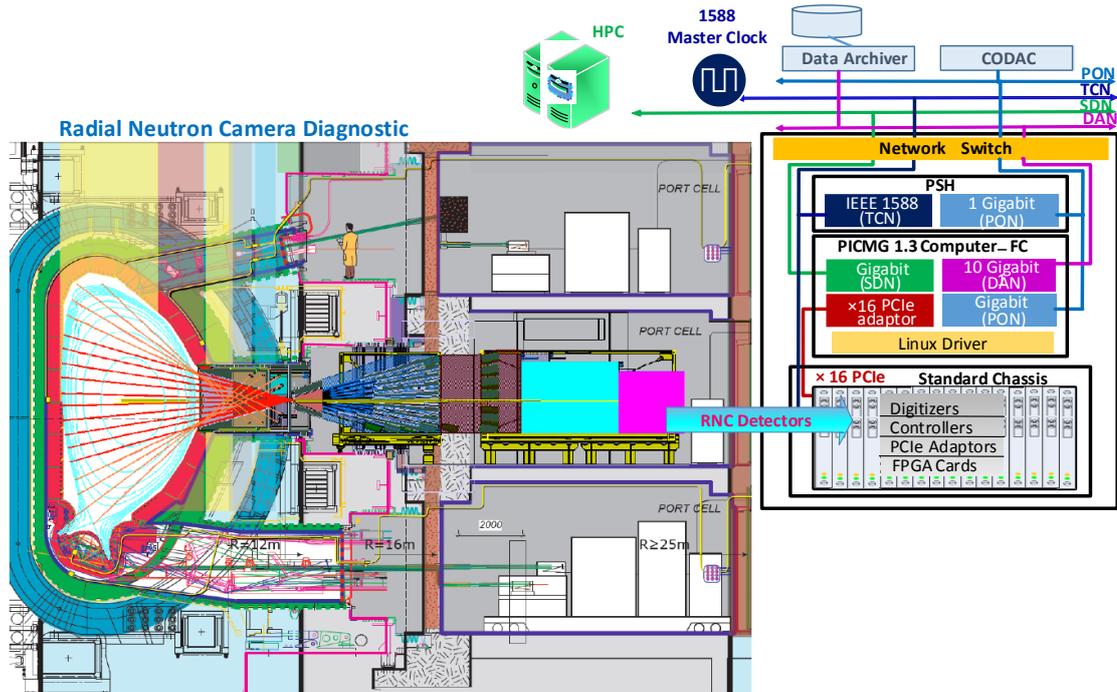


Figure 1: RNC Fast controller architecture.

3. DAQP system

The key features to be addressed to define the data acquisition system (digitizer) are the detector pulse width (and rising time duration) and the capability of providing pulse height spectra and particle discrimination.

Regarding the first feature, the pulse width (Full Width Half Maximum (FWHM)) for fission chambers and diamonds detectors typically spans from 10 ns (diamonds) to 200 ns (fission chambers), depending on the type of preamplifier used. Scintillators have a short pulse width (close to the lower end of the above range) but they feature a longer decay time of the pulse (few hundreds of ns) which allows for n/γ -separation. The minimum pulse width must be guaranteed by the system digitizer data acquisition rate, being a good practice of a DAQ system to have the capability to sample at least 5 times the $1/\text{FWHM}$ of the target pulses. The acquisition frequency shall span from 400 MHz to 1.6 GHz. The former is adequate to avoid any loss of information for scintillator [7][8]. The latter complies with the requirement of providing sufficient margins to allow additional functions and increased data rates, as well as exploring oversampling techniques to increase channel resolution. The second feature is linked to the digitizer resolution that, based on previous experience [9], should be in the range from 12 to 14 bits.

Concerning the processing capability of the system, at these high acquisition rates only powerful Field Programmable Gate Arrays (FPGAs) are foreseen to manage and handle such an amount of data. Therefore an FPGA blade with the latest products in the market is essential for the DAQP system. These elements must be based on the standards referenced in section 1.1. To address all needs of the RNC diagnostic two standards are evaluated: PCI Express Extensions for

Instrumentation (PXIe) and Advanced Telecommunications Computing Architecture (ATCA). Section 3.1 describes the ATCA DAQP prototype in more detail and section 3.2 compares PXIe and ATCA architecture data throughput performances.

3.1 ATCA DAQP Prototype

Figure 2 depicts the ATCA prototype, featuring: i) a 6-slot shelf subrack sharing a common backplane with dual-star serial gigabit communication links; ii) a shelf manager for hardware management enabling system high availability features; iii) an ATCA controller, carrying up to 4 Advanced Mezzanine Card (AMC), PCIe-switching and timing-hub card (ATCA-PTSW-AMC4)[10][6]; iii) a Rear Transition Module (RTM) with PCIe external cable interface to a $\times 16$ PCIe 2.0 switch[6]; iv) two Xilinx® Kintex-7™ FPGA based AMC, supporting I/O expansion adopting the FPGA Mezzanine Card (FMC) ANSI/VITA57 standard, v) one FMC module featuring 2 channels 12 bits sampled @1.6 GHz internal clock synchronized with master clock, AC or DC coupled; and iv) one FMC module featuring 2 channels 12 bits sampled @ 1 GHz, AC or DC coupled.

The 1.6 GHz FMC permits oversampling from 800/400/200/100 MHz, gaining up to 2 bits of resolution, while the 1.0 GHz FMC permits oversampling from 500/250/125 MHz, gaining up to 3/2 bits of resolution [11].

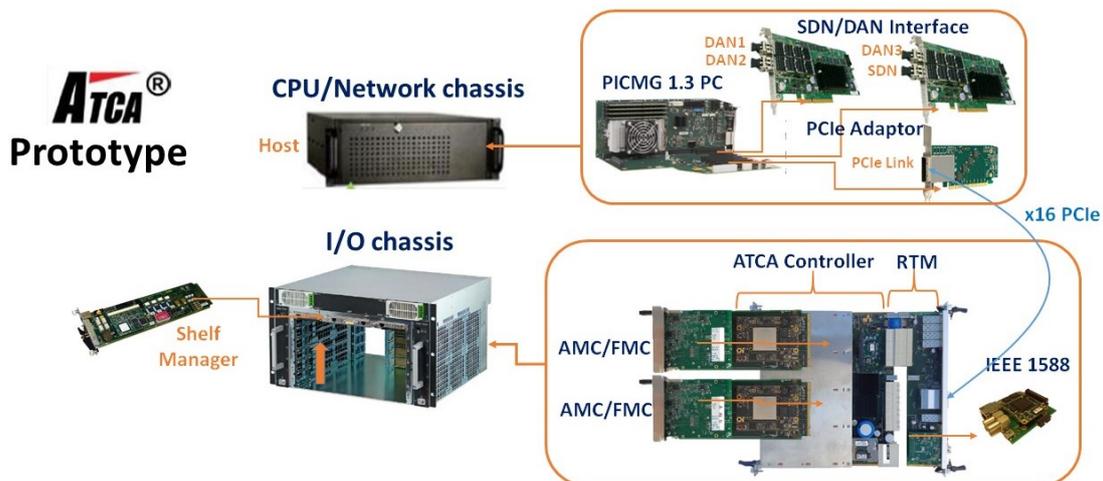


Figure 2: ATCA DAQP prototype.

3.2 ATCA vs PXIe Prototype

Three FC guidelines defined by IO [4][5] are: i) PCIe and Ethernet will be used as I/O intercommunication; ii) PICMG 1.3 based systems will be used for their CPU power and PCIe connectivity in mixed, interconnected systems; iii) Separated I/O and CPU/Network chassis is the preferred solution in the ITER I&C System. These guidelines are followed by both standard architectures. Therefore, both systems will be based on the same host, a PICMG 1.3 HPC, featuring a PCIe adaptor and 10 GbE links. The ATCA architecture backplane allows a $\times 16$ PCIe 2.0 link between the ATCA controller and the host. This connection allows, theoretically, up to 8 GB/s of data throughput (this figure must be tested with the prototype). On the other hand, the PXIe maximum slot bandwidth only offers $\times 8$ PCIe 2.0 interconnection limiting the data throughput between I/O chassis and host to 2.7 GB/s [12]. PXIe based prototype will count on

two types of digitizers, one featuring 2 channels 12 bits sampled @ 800 MHz and another one featuring 4 channels 14 bits sampled @ 1 GHz.

4. Prototype Motivation

The main reason for the construction of these prototypes is the acknowledgment of technical risks which could impact on the RNC FC final architecture. Two main types of risks were identified, respectively addressing the DAQP system architecture performance, and the FPGA and host of DAQP system processing power (related to real-time Algorithms).

The risks in the first case are: i) data loss due to inability to process high event rate peak; ii) data loss due to the inability to flush the enormous amount of data produced by the RNC digital acquisition system. For the first risk the correspondent project impact would be a possible failure to provide real-time measurements. Some effort must be made to acquire at event rates allowing data reduction without loss of data: this can be done, for example, by using adjustable collimator to reduce the incoming flux on the detectors. The project impact regarding the second risk would be a possible failure to send raw data to data archivers. This can be tackled by evaluating the feasibility and performance of data compression methods, which may be implemented in the host system as a first approach, and study the number of possible DAN links per host.

The risks in the second case are: i) inability to perform real-time processing which can lead to the possible technical failure to achieve n/γ discrimination; ii) inability to perform real-time inversion, leading to possible technical failure to achieve real-time inversion (≤ 10 ms) performance requirement. For both risks some effort shall be done on research and development for simpler (i.e. faster) algorithms to perform each task.

4.1 DAQP Prototype Testbench

The prototypes will acquire signals from a suitable signal generator to demonstrate the feasibility of the solution. This generator must be capable of simulating the signal source at the maximal expected performance: event rates between 0.2 and 2 MEvents/s and two different pulse decay times. Due to the random nature of the real detector signals, a signal generator able to simulate the real time structure of the expected events would be very advantageous to check the performance of the acquisition system in case of multiple pile-up events. Moreover, the Frascati Neutron Generator (14 MeV neutrons) will be used for final validation tests using different types of detectors.

Figure 3 depicts an architecture of DAQP prototype based on ATCA (similar for PXIe) with the key components and data links identified as potential bottleneck: (i) PCIe link from data acquisition module to system host; (ii) ethernet link between High Performance Host Computer (HPHC) and High Performance Data Management Computer (HPDMC); (iii) ITER Data Archiver simulated by storing the data

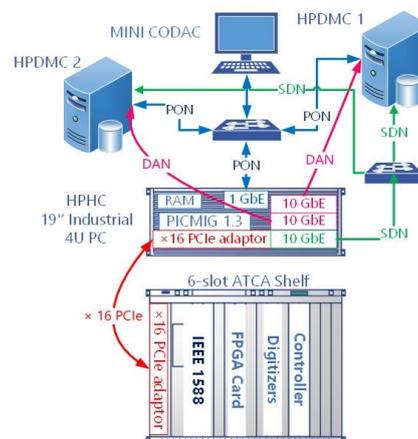


Figure 3: DAQP testbench.

received by the HPDMC in a high bandwidth storage system; (iv) computing power and data compression algorithm in the HPHC aiming at reducing the data to be transferred and stored.

The common testbench for testing the different components includes: i) programmable data size of 260 bytes for each event (timestamp 4 bytes, 128 event length of 2 bytes of data) or 132 bytes in the case 64 samples/event; ii) Direct Memory Access (DMA) transfers with predefined packet-size from FPGA to host; iii) acknowledgement of possible losses during transfers and data validation; iv) host software to manage the high data rates through the PCIe links.

The result of the tests will lead to the correct choice of the standard architecture for final RNC FC.

Acknowledgments

The work leading to this publication has been funded partially by Fusion for Energy under the Contract F4E-FPA-327 SG03. This publication reflects the views only of the author, and Fusion for Energy cannot be held responsible for any use which may be made of the information contained therein. IST activities also received financial support from “Fundação para a Ciência e a Tecnologia” through project grant UID/FIS/50010/2013.

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