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Upgrade of the ATLAS Tile Calorimeter for the High luminosity LHC

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The Tile Calorimeter is undergoing preparations for the high luminosity program of the LHC beginning in 2026, requiring a major replacement of on- and off-detector electronics. All digitized signals will be transferred directly to the off-detector electronics, where the signals are reconstructed, stored, and sent to the first level of trigger at a rate of 40 MHz. The planned upgrade will also contribute to the reliability and redundancy of the system. A hybrid demonstrator module has been developed using the new electronics while conserving compatibility with the current system. The Demonstrator is undergoing extensive testing and validation is planned through a testbeam study in October 2015 and insertion in ATLAS during Phase I.

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1. Motivation

The Tile Calorimeter (TileCal) is the hadronic calorimeter covering the central region ($|\eta| < 1.7$) [1] of the ATLAS detector [1] at the LHC. It is a sampling calorimeter consisting of alternating thin steel plates and scintillating tiles. Wavelength shifting fibers coupled to the tiles collect the produced light and are read out by photomultiplier tubes. An analog sum of the processed signal of several photomultipliers serves as input to the Level 1 (L1) trigger. Photomultiplier signals are then digitized and stored on-detector and only transferred off-detector once the L1 trigger is confirmed.

Phase II of the LHC promises to bring a high instantaneous luminosity in 2026, requiring TileCal electronics to withstand a much higher radiation environment and demanding a large increase in data transfer rates. Many components of the current TileCal system will also become obsolete on this time scale. To facilitate this upgrade a redesign of the on-detector Front-End (FE) and off-detector Back-End (BE) electronics is envisioned. Fully digitized signals will be provided to the L1 Trigger, replacing the limited analog signals and providing finer granularity. The pipeline memory will be moved off-detector, allowing more efficient, non-radiation hard components to be used but requiring a large increase in bandwidth. The FE electronics and power supplies will be divided into smaller functional units, increasing modularity and allowing for efficient extraction and repair of electronics drawers during short openings of the detector. The increased modularity will be supplemented with a increased redundancy of the components, increasing reliability in case of isolated malfunctions.

To prepare for commissioning of the Phase II electronics a demonstrator module is being developed and tested for early use in the detector. The Demonstrator will include all Phase II electronics as well as additional functionality for communicating with the current TileCal system. Test beams are planned to ascertain the reliability of the new system and early insertion of the Demonstrator into the ATLAS detector is planned.

2. Design

The Phase II upgrade will provide detector signals to the ReadOut Buffers (ROB) and L1 Trigger system through several stages of the FE and BE (Figure 1). PMT signals are conditioned and digitized by the Front-End Boards (FEB) and Mainboard (MB), then gathered through the Daughterboard (DB). Digitized signals are sent off-detector to the Tile Trigger PreProccesor (TilePPr) where the signals are reconstructed and distributed to the L1 Trigger.

The FE Electronics [3] are housed in rectangular, insertable modules called superdrawers. Each superdrawer will be made of 4 mechanically independent minidrawers, capable of individually detaching from the superdrawer to ease extraction and repair. A minidrawer is capable of serving up to 12 PMTs, and consists of 12 FEBs, a MB, a DB, and an High Voltage (HV) board.

Each FEB serves an individual PMT and provides amplification, shaping, and calibration of the PMT signals. Three FEB options are under investigation for use in Phase II, testing FEB

[1] The ATLAS coordinate system is right-handed, with the x-axis pointing to the centre of the LHC ring, the z-axis following the beam direction and the y-axis pointing upwards. The azimuthal angle $\phi = 0$ corresponds to the positive x-axis and ϕ increases clockwise looking into the positive z direction. The pseudorapidity η is an approximation for rapidity, y, in the high energy limit, and it is related to the polar angle θ as η = - ln tan $\frac{\theta}{2}$.

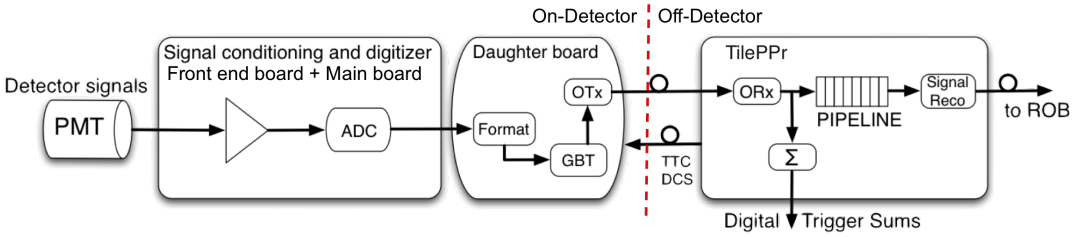


Figure 1: Cartoon of Phase II TileCal electronics, showing the pathway of detector signals to readout. Taken from [2].

configurations similar to the current versions or using custom ASIC chips. The Demonstrator uses a version similar to the current TileCal FEB, providing analog trigger outputs needed by the current L1 trigger. Each FEB option allows for calibration of the electronics, PMT gain, and scintillator response through two methods: a known charge injected at the PMT connection point and a slow charge integrator of the PMT readout for monitoring a cesium source or "minimum bias event" current.

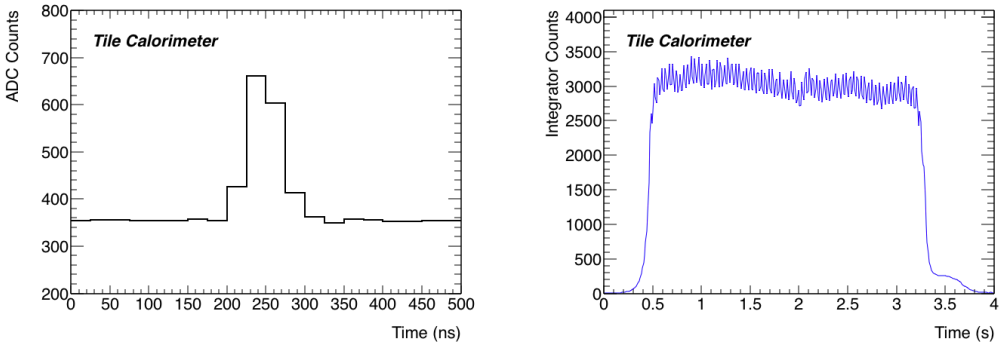
The MB interfaces with all 12 FEBs, providing signal digitization (if necessary) and tuning the sampling clocks to account for different signal transport lengths and forwarding synchronized signals to the DB. Point of load regulators handle two independent +10V voltage lines from the Low Voltage Power Supplies (LVPS), regulating to 9 different voltages for powering the entire Minidrawer. This design provides for a redundant +10V source in case of LVPS failure while limiting on board faults to a minimum functional unit of 6 PMTs. The DB interfaces the digitized signals from the MB to the TilePPr through 2 multi-gigabit Active Optical Cable modulators. Two Kintex-7 FPGAs are responsible for uploading fully digitized signals at a rate of 10 Gbps and receiving data streams encoded in the GBT protocol for configuration and timing. The TilePPr[4] interfaces the front end electronics to the L1 Trigger and ROB, storing digitized signals from up to 32 minidrawers at a time.

3. Performance

A functional demonstrator module has been assembled and is currently undergoing testing. Each component undergoes radiation testings to simulate various effects of radiation: the expected Total Ionizing Dose (TID) during Phase II, the Single Event Effects (SEE) of a high radiation environment, and the particle induced displacement damage effects, or Non-Ionizing Energy Loss (NIEL). Automatic scrubbing is implemented in all FPGAs and Triple-Mode redundancy is developed to counter any single event upsets in the DB.

Performance of the Demonstrator is primarily measured through the three calibration systems. The Charge Injections System (CIS) test the electronics directly, injecting a known charge into the FEB electronics to mimic a PMT signal. CIS tests show good control and linearity in the High Gain and Low Gain fast readout channels of the Demonstrator. The LASER calibration system tests the PMTs and electronics by flashing laser pulses of known intensity into the PMTs, allowing calibration of the PMT gains and trigger timing (Figure 2 a). The Cesium Scan

calibration system moves a Cesium-137 source through the modules to measure the response of the scintillator+PMT+electronics system on a millisecond time scale. The slow integrator sums the PMT response on a millisecond time scale for use with the Cs scans and for monitoring the beam luminosity through the PMT current from minimum bias interactions. Cesium Scans have been performed on the Demonstrator system (Figure 2 b), showing a comparable response of the Demonstrator system to current superdrawers. These extensive tests have shown the Phase II electronics working as expected and the readiness of the Demonstrator superdrawer for insertion into the ATLAS detector.



(a) (b)

Figure 2: Calibration plots showing a triggered LASER pulse of several hundred GeVs (a) and integrator response over time to a Cesium Source in Extended Barrel Cell D-6 (b), with characteristic sharp peaks as the source passes each of the 75 individual scintillator tiles. Taken from [2].

4. Conclusion

The Tile Calorimeter HL-LHC Upgrade has been designed and a proof of concept demonstrator module has been produced. Control and calibration tests are successfully implemented in the Demonstrator and legacy communication systems have been interfaced. Test beams for calibration and testing Front-End strategies are scheduled for October 2015, with Run II insertion planned during December shutdown of 2015 or 2016.

References

[1] ATLAS Collaboration, *The ATLAS Experiment at the CERN Large Hadron Collider*, JINST 3 (2008) S08003.

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[3] F. Tang *et al*, Upgrade analog readout and digitizing system for ATLAS TileCal demonstrator, in proceedings of *Nuclear Science Symposium and Medical Imaging Conference (NSS/MIC), 2013 IEEE*, 10.1109/NSSMIC.2013.6829443 (2013)

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