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Readout scheme for the Baby-MIND detector

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A readout scheme has been designed for the plastic scintillator bars of the Baby-MIND detector modules. This spectrometer will measure momentum and identify the charge of 1 GeV/c muons with magnetized iron plates interleaved with detector modules. One challenge the detector aims to address is that of keeping high charge identification efficiencies for momenta below 1 GeV/c where multiple scattering in the iron plates degrades momentum resolution. A front-end board has been developed, with 3 CITIROC readout chips per board and up to 96 channels. Hamamatsu MPPCs type S12571-025C photosensors were chosen for readout of wavelength shifting fibers embedded in plastic scintillators. Procurement of the MPPCs has been carried out to instrument 3000 channels in total. Design choices and first results of this readout scheme are presented.

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1. Introduction

The Baby MIND detector is a muon spectrometer designed to measure the charge of outgoing muons from neutrino interactions occurring in a neutrino target further upstream as part of the WAGASCI experiment [1]. A new front end board (FEB) has been designed and is reported in this paper.

2. Baby-MIND detector modules

The Baby-MIND detector modules are based on plastic scintillator bars, with embedded wavelength shifting (WLS) fibers. The fiber ends are instrumented with silicon photomultiplier (SiPM) photosensors. The selection and optimization of materials (plastic scintillator, optical glue, WLS fiber) and geometries (bar size, custom optical connectors) is described in [2].

2.1 Scintillator bars

The scintillator slabs are polysterene-based with 1.5% of paraterphenyl (PTP) and 0.01% of POPOP, similar to the plastics used for the T2K SMRD detector counters [3]. The surface is etched with a chemical agent (Uniplast) to create a 30-100 μm layer acting as a diffusive reflector. A 2 mm deep groove is machined along the length of every bar into which a wavelength shifting fiber (WLS) from Kuraray (200 ppm, S-type) of d = 1.0 mm is embedded with either a silicon grease (TSF451-50M) for test purposes or an optical cement (ELJEN-EJ500) to improve optical contact between the scintillator groove surface and the fiber. Connectors glued to either end of the bar align the fiber ends with the photosensors, Figure 1.

Two types of modules using the same sensing technology but with different geometrical layouts are under development. Nominal parameters for the type 1 geometry are bars of 90 cm long, 0.7 cm in height and 1.0 cm in width. Over 9000 of these bars were manufactured and tested by the INR with results reported in these proceedings [4].

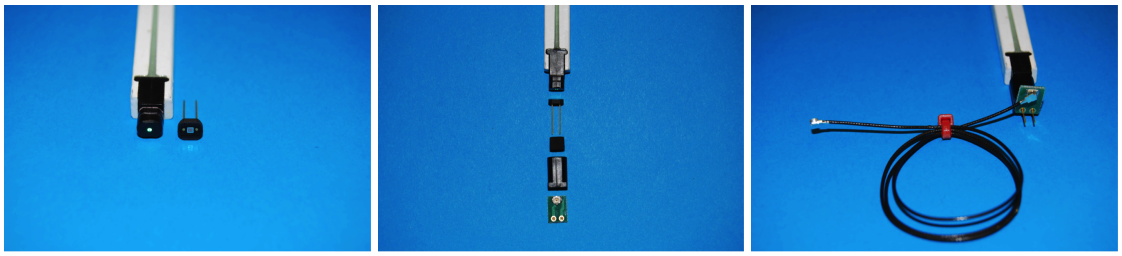

Figure 1: Photosensor connectivity. The figure on the left shows the polished fiber end, with a photosensor placed next to it for scale. The figure in the center shows the components that slot into each other to produce the figure on the right.

2.2 Photosensors

The photosensor type chosen for the first phase of operation during which only a subset of the total number of channels will be instrumented is the S12571-025C from Hamamatsu. It has an active area of 1 $\times$ 1 mm^2, 1600 cells of size 25 $\times$ 25 μm^2, a geometrical fill factor of 65 %, gain

of 5.15×10^5, quoted PDE of 35% not including crosstalk or after pulse. Recommended operating voltages for the specified gain of 5.15×10^5 and measured dark counts by the manufacturer are reported in Figure 2 for 3000 such devices procured in 2015. The spread in operating voltages is well contained, with an RMS of 0.14 V for a mean of 67.51 V. A more relevant figure of merit given the requirement to use as many of the delivered photosensors is the total range of operating voltages which is well within the range of values that can be set with internal DACs on the readout chip as described in the next section.The mean dark count of 83.34 kHz and narrow spread fall well within manufacturer specifications that indicate typical and maximum dark counts of 100 kHz and 200 kHz respectively.

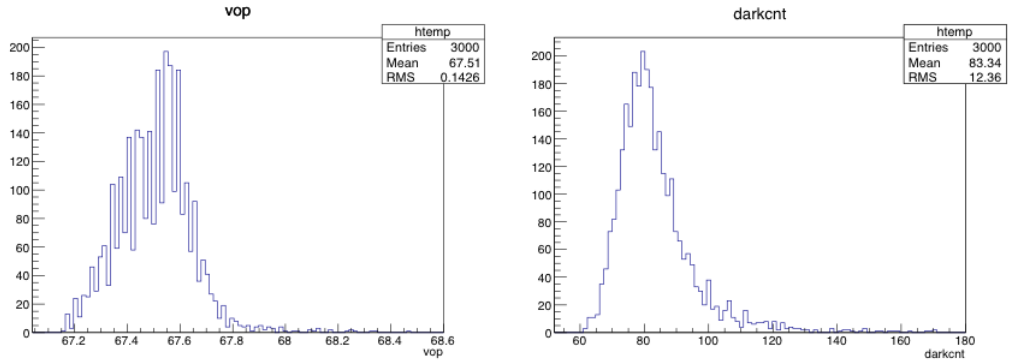

Figure 2: Measured properties of the 3000 Type S12571-025C photosensors delivered by Hamamatsu Q1 2015: left) operating voltage in [V], right) dark counts in [kHz].

3. Electronics readout scheme

Muon spectrometers of the MIND-type are generally designed to record hits with high efficiencies in environments where particle rates are modest. Having identified the CITIROC [5] as a potential readout chip for the SiPMs instrumenting the detector planes, compatible with operational requirements, the readout scheme was developed around it.

3.1 General electronics chain

In defining the readout scheme, the main scenario considered was operation in a particle beam line. Concerning timing, the two main characteristics of such an operation are the generation by systems external to the detector of:

- a spill gate (enable signal): the accelerator producing the particles does so in bursts with a well defined bunch or pulse structure. The spill gate is effectively a "detector enable" signal, indicating which fraction of time during a given period particles are likely to impinge on the detector.

- an external trigger: components in the beam line usually include one or more fast trigger systems that send a trigger to detectors downstream signaling the passage of a particle to be recorded.

Detector planes are read out by Front End Boards (FEB) which sample and records hits. Several FEBs are chained in series, sending data to the back-end VME Read out Boards (VRB), from the communicating FEB to the VRB through the entire chain, Figure 3. All dynamic beam line signals and slow control configuration parameters are sent by the VRB to all FEBs in a chain at the same time (propagation and repeater delay from board-to-board excepted), with each intermediate FEB acting as a repeater with a concurrent access protection mechanism. It is planned to instrument 4000 channels on the Baby MIND spectrometer. Up to 96 channels can be connected to each FEB, with between 4 and 8 FEBs per VRB.

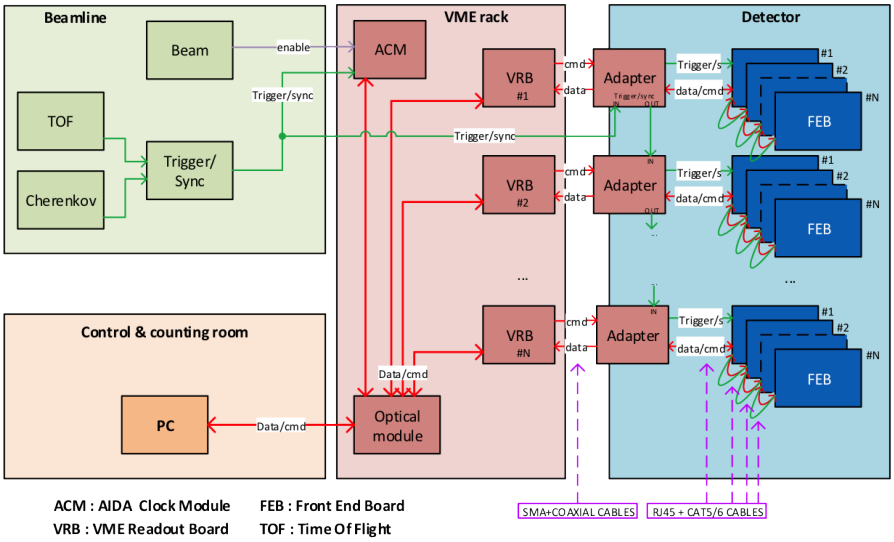

Figure 3: Overview of the electronics chain for the Baby MIND detector.

3.2 Operation in a beam line

The initial beam line considered was one derived from the CERN-SPS, in slow extraction mode providing charged particles at a rate of 1 kHz during a 10 s spill, with a 20 s gap between spills, Figure 4. A basic configuration is one where the detector planes record hit time and amplitude locally on the Front-End Boards during the 10 s spill, and send data to the back-end data acquisition system during the 20 s gap between spills. Requirements such as buffer sizes on the FEBs and transfer speeds were drafted from these assumptions.

Multiple hits on a detector plane are likely for a given particle trigger, however the probability of having multiple hits on the same channel within a plane is considered to be low (<0.1%). This low channel occupancy justifies the selection of the CITIROC chip. Although this ASIC has a limited bandwidth due to the multiplexing of its analogue outputs as described in the next section, it is adequate for the purposes outlined here. The challenge comes from extracting analogue information for a channel that records both the passage of a parent muon, and its decay electron up to 10 μs later. This scenario is addressed by sampling at a much higher frequency the digital trigger outputs of the ASIC: the analogue information for that second particle is lost, but the hit is recorded.

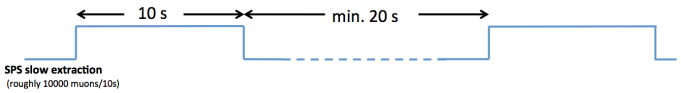

Figure 4: Charged particle beam structure for a slow extracted beam at the CERN-SPS.

3.2.1 CITIROC chip

The CITIROC chip is a 32-channel fully analogue front-end ASIC dedicated to the gain trimming and read-out of SiPM sensors. It is designed in 0.35 μm SiGe technology from AustriaMicroSystems. It is an evolution of the EASIROC chip which was available since 2010 and used in a variety of experiments such as PEBS, MuRAY, at JPARC and in medical imaging. The EASIROC is derived from the SPIROC chip which was developed for hadron calorimetry foreseen for the International Linear Collider.

The chip integrates a 4.5 V (2.5 V slow control bit setting) range 8-bit DAC for individual SiPM gain adjustment by modification of their operating voltage, Figure 5. The analogue core is sensitive to positive SiPM signals. For each channel, two parallel AC coupled voltage preamplifiers ensure the read out of the charge from 160 fC to 320 pC (i.e. 1 to 2000 photoelectrons with SiPM Gain = 10^6, with a photoelectron to noise ratio of 10), providing high gain (HG) and low gain (LG) paths. Two variable shapers are used to reduce noise; each of them has an adjustable peaking time from 12.5 to 87.5 ns to allow the user to minimize the noise depending on the final application. A trigger path that can be switched between either the low or high gain preamplifiers is composed of a 15 ns peaking time fast shaper followed by two discriminators. One discriminator provides trigger and hit information, with a programmable mask to block unwanted channels, the other provides accurate time information. An internal 10-bit threshold common to all 32 channels can be set for each of the two discriminators with a minimum level of 50 fC (1/3 p.e. with 10^6 SiPM gain). Fine trimming of each channel's discriminator is also possible with a 4-bit DAC. Power consumption is 5 mW/channel and unused features can be powered OFF.

The 32 analogue channel paths are multiplexed into one output each for HG and LG. Low and high speed multiplexer modes lead to sampling durations of 54 μs (600 kHz/ch readout) or 6.4 μs respectively (5 MHz/ch readout). Because it is not possible to access analogue channels individually, the high speed mux mode sets the sampling rate requirement for the ADC which is external to the CITIROC. The accessible individual trigger outputs are sampled at much higher rates of up to 400 MHz by the FPGA located on the FEB.

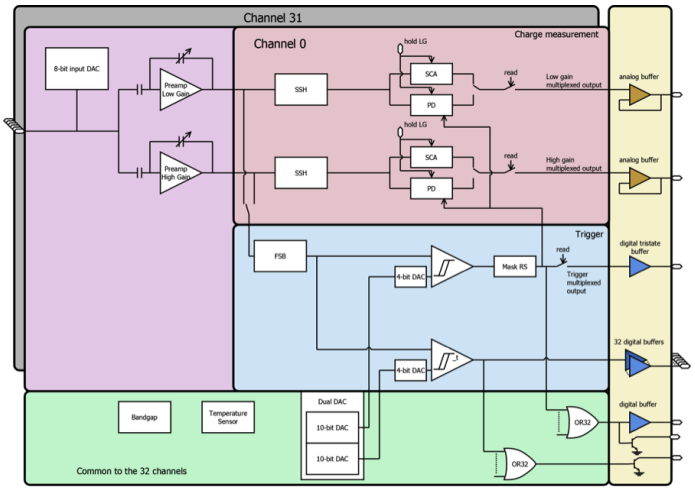

Figure 5: CITIROC block diagram.

3.2.2 Front End Board architecture

The FEB architecture optimizes the functionality of the CITIROC ASIC by coupling an FPGA to it which:

- acts as a Time-to-Digital-Converter (TDC) by sampling the ASIC individual trigger outputs for time measurements with respect to the beam line external trigger mentioned previously,
- samples the ASIC multiplexed HG and LG analogue signal paths through a multi-channel ADC.

The FEB block diagram is shown in Figure 6. The current version of the FEB is designed to read out one plane with 84 SiPMs. The FEB consists of three CITIROC chips, a 12-bit 8-channel ADC for the digitization of the analogue outputs of the CITIROC (HG and LG $\times$ 3 chips, temperature, humidity), an FPGA for time-stamping of CITIROC trigger outputs and digital signal processing, high-speed serial link transceivers, low and high voltage converters. The first front end board prototype was manufactured in March 2015, Figure 7. Of the 32 channels per CITIROC, only 28 are connected to coaxial connectors on the edge of the board. The remaining 4 ASIC channels are accessible for debug or other purposes but their connectors are located in the middle of the board.

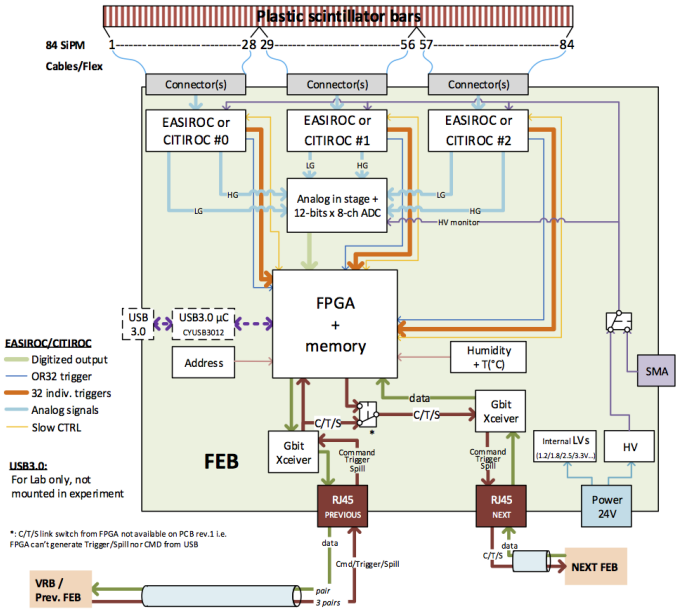

Figure 6: Baby MIND readout scheme with an 84-channel implementation per Front-End Board. Up to 96 channels can be connected to one FEB.

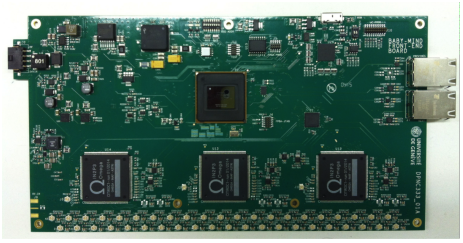

Figure 7: First prototype of the Baby MIND Front End Board.

3.3 FPGA firmware

The FPGA mounted on the first prototype board is of the ALTERA ARIA5 family, type 5AGXBA7D4F31C4N. Production boards will employ a cheaper variant from the same family. The main FPGA firmware functional blocks are organized according to three distinct clock domains running at 400 MHz, 100 MHz and 50 MHz (Levels L0, L1, L2) with some overlap between levels within blocks. They can be broadly summarized as follows, see also Figure 8:

- **Timing block:** each of the 96 trigger channels on the FEB must be independently recorded versus the time with a 2.5 ns counter resolution within a 10 μs window triggered by the trigger signal. The FEB internal global trigger may be selected between either 1) the external trigger signal entering the FEB via the RJ45 connector or 2) an internal trigger generator with a programmable period of 5 μs to 10 ms with a resolution of 1 μs. These two options provide functionality for different scenarios, operation with beam synchronization for single(1)/multiple(1) FEBs and cosmic measurements on single(2)/multiple(1) FEBs. A fu-

ture version of the firmware foresees broadcasting of the internal generator from one FEB to several FEBs.

- **Analog block:** an ADC State Machine manages the 6 (HG & LG) multiplexed analogue outputs from the 3 ASICs. A Threshold State Machine is implemented to control baseline computation and event validation. These state machines used in combination distinguish between baseline cycles and hit cycles. The former cycle type is used to periodically monitor, compute and store baseline values for each channel independently, the latter is used to process the analogue hit amplitude comparing it to one of several threshold modes.

- **Readout block:** counters for timing and data synchronization are attributed here, and the readout of the analog block is managed here before data are loaded into the FIFO ready for processing by the communication block.

- **Slow-control block:** manages configuration of ASICs, FPGA and ADC.

- **Data communication block:** an Encoder and Decoder work within this block to process data and commands using a cyclic redundancy check CRC-16. TX and RX FIFOs operate within this block, their data pushed into the next block.

- **Physical communication block:** manages communications with external devices. Two modes are available on the FEB for interfacing with external devices, a USB3.0 mode and a Gigabit mode. In USB3.0 mode the L2-RX and L2-TX FIFOs are directly accessible from the USB3.0 microcontroller for read and write. In Gigabit mode data and commands are transmitted over the gigabit transceivers from the L2-RX and L2-TX FIFOs.

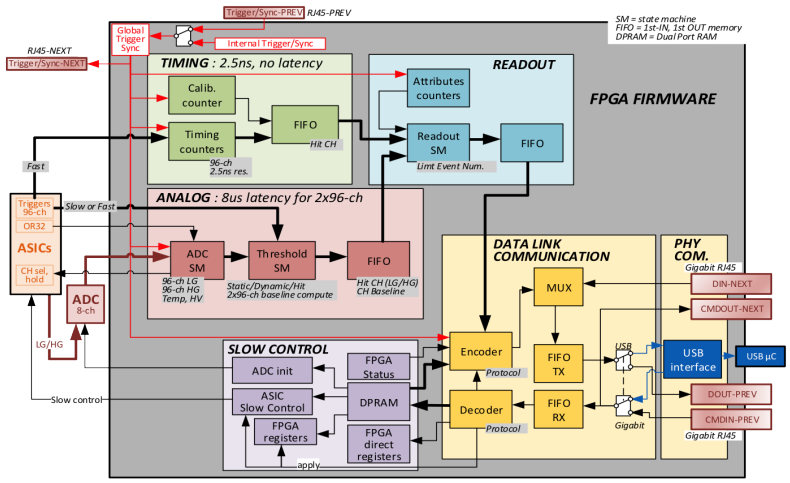

Figure 8: Sketch showing the main blocks of the FPGA firmware.

3.4 Hit cycle specifics

The ADC State Machine starts the ADC readout cycle when the 'sync' signal is asserted. This signal can be selected by a FPGA configuration bit according to either:

- **CAL mode**: the "internal global trigger" for use in calibration or free running mode.
- **ACQ mode**: the OR96 trigger signal (an OR of the three OR32 outputs from each ASIC) for use during analog data acquisition synchronized with the ASIC triggers.

Although all analogue channels are sampled by the ADC, only the enabled LG and HG channels are pushed to the Threshold State Machine.

Different threshold modes can be selected within the Threshold State Machine when the comparison is required:

- **STATIC mode**: all ADC values are compared to a common fixed threshold used for all channels. If the ADC value is above threshold, it is pushed into the L1-FIFO and accessible for readout.
- **DYNAMIC mode**: the ADC value is compared to the independent channel baseline computed and added to a common fixed threshold used for all channels. If the ADC value is above the combined baseline + fixed threshold, it is pushed to the L1-FIFO and accessible for readout.
- **HIT mode**: if the channel has been hit (i.e. value set on slow trigger MUX output of ASIC) then the ADC value is pushed into the L1-FIFO and accessible for readout (only available from CITIROCv2).

Whatever threshold mode is selected, the ADC value resulting from the comparison phase can be limited to 10 ADC hits (from L1-FIFO) for the readout frame, along with 10 time hits (from L0-FIFO) when the "LIMIT10" mode is enabled. In this case, since the channels are read sequentially, only the 1st 10 channels hit are pushed into the L2 FIFO, other channel events are lost. A "channel event limit per trigger" function can limit the number of time hit events pushed into the L0-FIFOs to 1 per global trigger. This also applies to ADC L1-FIFOs and is implemented to reduce the data bandwidth of the readout system.

4. Results with the CITIROC ASIC

4.1 CITIROC parameters evaluation

With the firmware for the Baby MIND FEB under development, a CITIROC evaluation board supplied by Omega Microelectronics was used to test and validate the full chain of components including final scintillator bars equipped with WLS fibers, S12571-025C photosensors, custom pcb and coaxial cables for connectivity. This testing phase was also useful in determining a reference set of slow control parameters for the CITIROC ASIC. Parameters studied were:

- Calibration of the system: resolution of individual photo-electron peaks,
- Assessment of the dynamic range,
- Light yield estimate for the scintillator bars,
- Extraction of CITIROC configuration parameters.

4.2 Channel assignment

With one CITIROC chip instrumenting a maximum of 32 channels, the test setup was designed to return as much information as possible to cover the study programme outlined above. Eight scintillator bars where studied in detail, each of these read out from both ends. The remaining 16 channels were assigned to scintillator bars read out from one side only for coincidence measurements, 8 of these parallel to the 8 scintillators under study, and two groups of 4 bars perpendicular to the 8 scintillators under study, Figure 9.

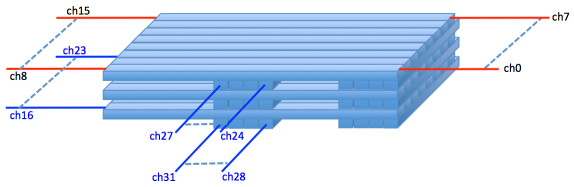

Figure 9: Configuration of scintillator bars and corresponding CITIROC channel numbers.

4.3 Resolving individual photo-electron peaks

The optimization process for combination of MPPC gain (via setting of the operation voltage), and CITIROC pre-amp gain was not foreseen to provide a final set of parameters. As can be seen from Figure 10, the photo-electron peak resolution remains acceptable for a pre-amp feedback capacitor setting of 12, corresponding to approximately 550 fF or a gain of 27.3 given the input capacitance is 15 pF.

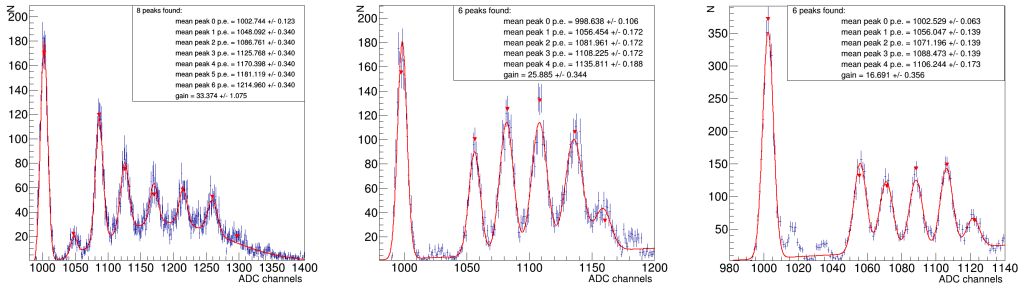

Figure 10: Photo-electron peak resolution for a S12571-025C MPPC coupled to a CITIROC chip. Digitized outputs from the high gain path are shown with different feedback capacitance values of 275 fF, 350 fF and 550 fF (settings of 1, 4 and 12 in the CITIROC slow control register and assuming a parasitic capacitance of 250 fF), yielding 33.37 ± 1.08 ADC/p.e., 25.89 ± 0.34 ADC/p.e. and 16.69 ± 0.36 ADC/p.e. respectively.

4.4 Shaper and hold delay scan

The CITIROC shaper peaking time can be set to different values as mentioned previously, in 12.5 ns steps. A "Hold" signal applied to the shaped signal determines at which point in time the shaper output is sampled. In this configuration, the OR32 trigger output from the CITIROC is routed to the FPGA which then generates the Hold signal, offset by a programmable delay that can be adjusted in steps of 1 ns. This delay between the OR32 output and the Hold signal was

varied to study the sensitivity of light yield measurements to the Hold position setting. Figure 11 (right) shows the OR32, Hold, and shaper outputs. The plot in Figure 11 (left) was obtained by changing the programmable delay, calibrating the output by measuring single photo-electron peaks for each delay setting in dark count mode, then running in cosmic ray mode to measure the light yield from the scintillator bars. The errors on light yield measurements are largely due to those from the calibration measurements. CITIROC parameters were a shaper peaking time of 37.5 ns and a pre-amp capacitor setting of 12 (550 fF). The horizontal axis chosen in Figure 11 (left) is the "OR32 delay setting" which is set by the user in the LabVIEW slow control panel. The effective hold on the shaper output is further offset by approximately 14 ns. The peak on the shaper output was measured to be 17 ns (OR32 delay setting) + 14 ns (Offset), below the specified 37.5 ns. When sampling the shaper output either before or after its peak over the range reported here, the recorded light yield does not change significantly, indicating that calibration runs with dark counts at low light levels (1 to 5 p.e. typically) are applicable for cosmic ray measurements with light yields around 80 p.e., i.e. there is some indication of a degree of linearity in the response of the shaper over a range of input amplitudes, valid for different sampling points along the shaper output.

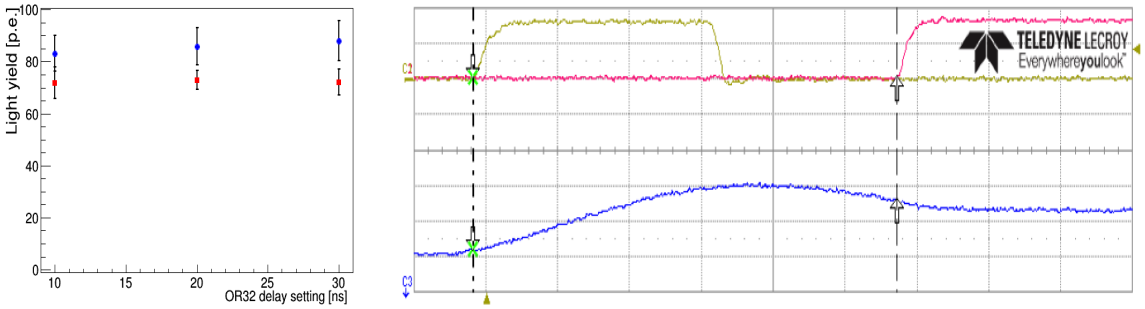

Figure 11: Shaper output scans. Left: light yield as a function of the OR32 delay setting for two channels. Right: Oscilloscope measurements of the OR32 output from the CITIROC (green), the Hold signal from the FPGA (pink), and the shaper output (blue).The voltage amplitude on the vertical scale is arbitrary, the horizontal scale is set to 20 ns/division. The cursors show the start of the OR32 signal and the start of the Hold signal. An offset of a few ns is visible between the start of the Hold signal and the stable level reached for the final value that is retained from the shaper output. In this example, the Hold signal has been applied on the falling edge of the shaped signal, rather than at its peak amplitude.

4.5 Light yields

Light yield measurements running in cosmic ray mode at 25° C in a dark room where only the channels under test Ch0-15 have their self-triggering functions switched ON confirm the high light yields reported in [4]. The sum of light yields from both ends has a mean around 170 photo-electrons, Figure 12. Large angle tracks pass the event selection cuts, leading to a range of path lengths through the plastic scintillator including longer tracks with higher energy deposition which explains the higher light yields in measurements reported here. The pre-amplifier gain was set such that the ADC/p.e. ratio was approximately 11.3. Saturation effects are visible in the l.y. plots, with a peak at 275 p.e. corresponding to the 12-bit ADC maximum range (the baseline is at approximately 950 ADC counts), though not significant, affecting 0.5% of events.

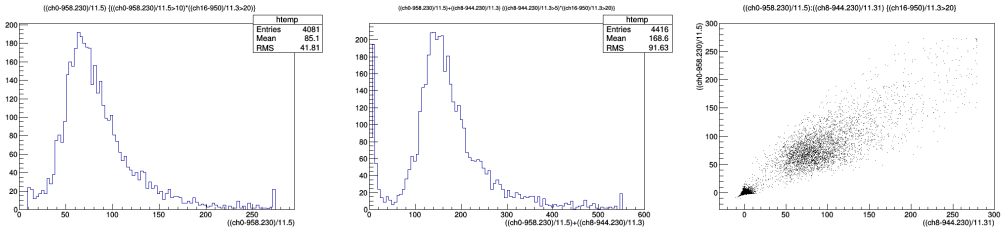

Figure 12: Cosmic ray data for one bar, read out from both ends, Ch0 and Ch8, with another bar located underneath used as coincidence, Ch16. Left) light yield from one end, middle) sum of l.y. from both ends, right) 2D plot of l.y. with one channel plotted against the other. All values are photo-electrons.

5. Summary

A new Front End Board based on the CITIROC ASIC has been designed for the readout of scintillator modules that will instrument the Baby MIND muon spectrometer. It consists of CITIROC ASICs, an ADC for the digitization of the analogue outputs of the CITIROC and an FPGA for time-stamping of trigger outputs and digital processing. Tests with a CITIROC evaluation board confirm high light yields well in excess of 100 photo-electrons when summing signals from both ends of a given bar, for the implemented combination of plastic scintillator, WLS fiber, photosensor and electronic readout scheme.

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