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ATLAS pixel upgrade for the HL-LHC

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From 2024, the HL-LHC will provide unprecedented proton-proton luminosities to ATLAS, delivering an integrated luminosity of 3000 fb^{-1} over ten years. This will present a unique opportunity to extend the mass reach into the multi-TeV region for new physics searches, and to significantly extend studies of the Higgs boson. The order of magnitude increase in instantaneous luminosity and the associated increase in hit occupancy and radiation fluence will render the current Inner Tracker inoperable. It will be replaced with an all silicon tracker to maintain tracking performance. Present ideas and solutions for the pixel detector are presented with a focus on the system layout and the recent developments of the hybrid pixel module.

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1. Introduction

The discovery in 2012 of the Higgs boson by the ATLAS and CMS collaborations was a great triumph for Particle Physics. Many physics questions, however, remain unanswered. The present detectors will run until the end of 2022 and collect data from an expected 300 fb^{-1} of integrated luminosity. Many physics questions require a significant increase in integrated luminosity, which will be provided by the high luminosity LHC, (HL-LHC). The HL-LHC, with a planned start date of 2026, has the goal of achieving an ultimate instantaneous levelled luminosity of 7.5 $\times$ 10^{34} $cm^{-2}s^{-1}$, resulting in a total integrated luminosity of 3000 fb^{-1} by 2035. The instantaneous luminosity corresponds to about an average 200 additional pp collisions per beam-crossing, a factor of four higher than the LHC ultimate design.

There are three major physics motivators for the HL-LHC; which are: a deeper understanding of the Higgs boson, careful examination of the Standard Model and explicit searches for New Physics. The increased luminosity extends the accessible mass scale of the experiments enabling physics studies well into the multi-TeV region. The large data sample will allow significant improvements in the precision of the measurements of the Higgs couplings.

The increased instantaneous luminosity leads to major challenges to the inner tracker including increased detector occupancy, higher radiation damage and higher data transmission requirements. As a consequence the inner tracker has to be re-designed to cope with these challenges while maintaining or even improving the tracking efficiency, fake rate and b-tagging capabilities of the present tracker.

This paper describes the development of the new pixel sub-detector of the inner tracking detector (ITk) for the upgraded ATLAS experiment under development for the HL-LHC.

2. Layout

The HL-LHC ATLAS inner tracking detector will be an all-silicon instrument with expanded strip and pixel systems compared to the existing inner detector. The tracker will be hermetic giving robust tracking with at least 14 silicon hits for a pseudo-rapidity coverage extending to at least $\pm$2.7 to allow good matching with the muon system, with possible extensions to $\pm$4.0, see section 2.1.

The optimal design of the ITk will be a compromise between: efficient pattern recognition and track reconstruction, cost optimisation, ease of construction and installation, as well as the ability to maintain the detector throughout its lifetime. The requirements have spawned a range of designs, each addressing particular facets of the requirements, which are now under active consideration within the ITk simulation and performance group. Presented here is the benchmark design, known as the letter of intent version (LoI)[2], with an update to use rings in the forward pixel system rather than disks.

The LoI layout has 4 pixel barrel, 5 strip barrel layers, 6 pixel disks and 7 strip disks on each end, which is shown schematically in Fig. 1, while the area and number of channels are given in Table 1.

This design was optimised to give the required tracking perfromance in terms of fake rate, hit efficiency and momentum resolution but had many deficiencies, including, for example, an engineering problem for the routing of the services through the pixel disks, a non-optimal layout

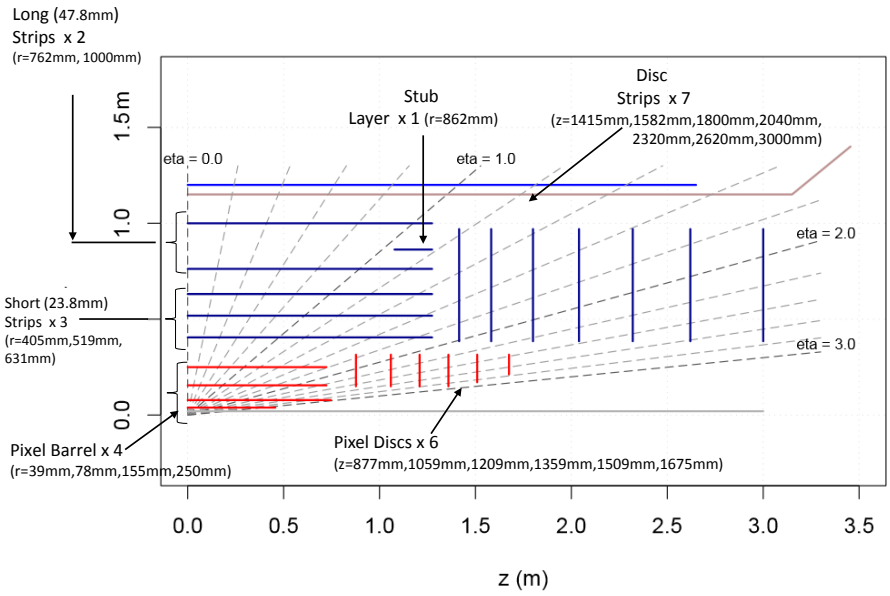

Figure 1: A cross-section of the ATLAS ITk LoI layout showing coverage of the pixel detector in red and the strip detector in blue. The rapidity coverage extends up to $|\eta| < 2.7$. The blue line outside the ITk volume represents the coil of the solenoid magnet.

Detector	**Silicon Area (m^2)**	**Channels (10^6))**
Pixel Barrel	5.1	445
Pixel Endcap	3.1	193
Pixel Total	8.2	638
Strip Barrel	122	47
Strip Endcap	71	27
Strip Total	193	74

Table 1: The surface area and channel count for different parts of the ATLAS ITk for the LoI layout

regarding the of number of silicon modules required and limitations to extend the eta coverage beyond $|\eta| < 2.7$.

The Pixel Ring layout modifies the LoI layout by replacing the solid pixel disks with a series of open pixel rings to support modules. Three types of pixel rings are defined, (inner, middle and outer), based on radial dimensions, which are placed at specific positions in Z to ensure hermiticity for tracks originating from an interaction point of $Z = 0 \pm 15$ cm. The rings reduce the active area from 3.1 m^2 to 2.6 m^2, while offering good flexibility in routing the services through the gaps between the rings. The design can also be easily extended with additional rings at higher Z and lower radii for extended rapidity coverage.

2.1 Beyond the LoI layout

A detailed review of the general requirements for the ITk layout and design, as well as further optimisation of the Pixel and Strip layouts beyond the current LoI designs is underway and due to

report in early 2016. Several variations are being examined including an increase in the number of pixel barrel layers and an extension of the pseudo-rapidity coverage.

A significant layout change since the LoI concerns the number of barrel pixel and strip layers. The expected mean number of interactions per bunch crossing has increased from ∼140, reported in the LoI, to ∼200, due to the predicted increase in the maximum levelled instantaneous luminosity increasing from 5×10^{34} to 7.5×10^{34} $cm^{-2}s^{-1}$. This has increased the average hit occupancy of the first strip barrel layer to 0.8 %, with additionally the highest hit occupancy of close to 1 % being present in the strip forward system at a radius of approximately 700 mm, shown in Fig 2. The hit occupancy is important as it places significant requirements on the design of the read-out electronics and it must be kept low to allow efficienct pattern recognition with low fake rates. The occupancy of the inner barrel region can be reduced with an additional pixel barrel layer and the removal of a strip barrel layer accompanied by a redistribution of the remaining strips layers. Additional advantages follow the use of 5 pixel and 4 strip barrel layers. These include; advantages in the on-line and off-line track reconstruction performance as the extended pixel system will have huge improvements in the seeding of a track. Better two-particle separation in high transverse momentum jets will also result. This will increase track efficiency and the rejection of fakes, improve flavour tagging in dense environments and better resolve ambiguities due to photo-conversions. A layout with 5 pixel layers and 4 strip barrel layers has been adopted as the new baseline layout, with optimized layer radii to maintain approximate cost neutrality compared to the LoI design.

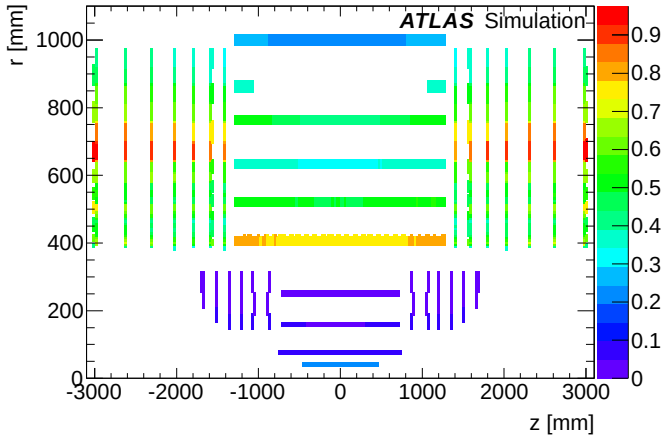

Figure 2: The expected percentage hit occupancy map for 200 pileup events for the ITk strip detector sub-system. Z scale shows percentage occupancy.

The physics program is significantly enhanced with increased pseudo-rapidity coverage with respect to the LoI layout. The main performance advantages are: extended b-tagging, L1 track capability, missing transverse energy, (E_T), resolution and in associating forward jets with a primary vertex and rejecting pileup jets. This benefits a range of physics, for example: signatures with forward jets, including vector boson scattering and vector boson fusion, and SUSY signatures requiring optimum transverse missing energy measurements and b-tagging.

The exact rapidity coverage must take into account the combined effects of: the decreased

magnetic field at large Z and small radius, the decreased lever-arm for tracks that originate in that region and the effects of increased material from the services that will be located in front of the calorimeter. Additional material in this location must be minimized, since it not only degrades the forward calorimetry resolution, but also increases the flux of secondary particles into the forward ITk, which in turn increases the neutron fluence throughout the tracker. The maximum coverage of $|\eta| \leq 4.0$ is being considered as being the best compromise between the requirements of physics and the experimental constraints.

The best method to realise the extended coverage is an active area of investigation within the ITk pixel community, with the two proposals being the Pixel Ring Very Forward layout and the Extended Pixel Inner Barrel Layers layout.

The Pixel Ring Very Forward layout is a simple extension of the baseline layout with additional pixel rings placed at higher Z and with two new ring types at radii between the innermost existing ring and the beam pipe. This solution requires many small radii rings with the detrimental increase in service count and material that this entails. An alternative to full track reconstruction in the very forward region is to reconstruct a partial track by estimating the particle's production vertex along the beam-line and its azimuthal, ϕ and polar, θ, angles. This can be achieved by using the pixel cluster size along the beam-line and its global position in a single(double) extended pixel layer placed close to the beam-pipe [3]. This is realised via the Extended Pixel Inner Barrel Layers layout, which removes the additional two inner rings and lowers the required number of modules with the accompanied reduction in services and material. The inner radius barrel layers are extended in length to cover the rapidity region of interest. The Z-position of the particle's production vertex along the beam line is given by:

$$Z = Z_{cluster} - \frac{R \times p \times (N_{col} - \delta)}{t} \tag{2.1}$$

where R is the radial coordinate of the cluster radius, $Z_{cluster}$ is the Z coordinate of the cluster center, N_{col} is the cluster size in the direction along the beam line, $\delta = 0.8$ is an empirical correction which accounts for the fact that a particle does not always cross the full length of the first and last pixels in the cluster, p is the pixel pitch in the direction along the beam line and t is the sensor thickness. The resolution in the Z-position is related to the position resolution of the first and last pixels in the cluster, i.e. $\frac{p}{\sqrt{12}}$, so that:

$$\sigma(Z) \sim \frac{\sqrt{2}R \times p}{t\sqrt{12}} \tag{2.2}$$

The effective thickness, t can be increased by using two thin sensor layers, as shown in Fig. 3. For an inner radius of R = 33 mm and a pixel pitch p = 50 μm with two layers separated by 5 mm the intrinsic resolution of $\sigma(Z) \sim 200$ μm is possible, given by equation 2.2. The azimuthal and polar angles of track can be found with an error of ~ 0.001 rad. Such precision is enough to link the pixel cluster with calorimeter objects in the forward region.

3. Major challenges of the HL-LHC pixel system

The major challenges of the HL-LHC pixel system are the expected radiation levels that the system must withstand, the data rates that are required to be transmitted off the module and those associated with the scale of the project.

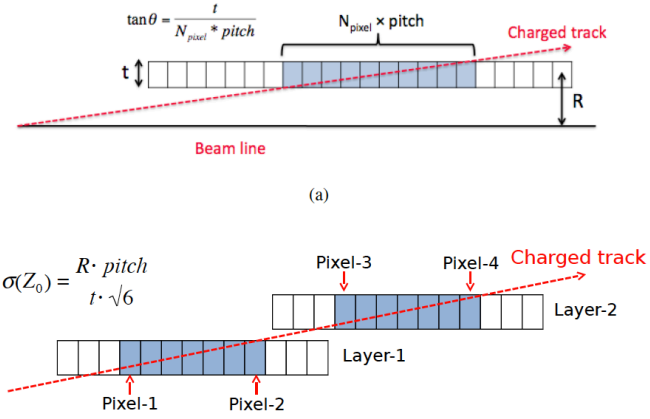

Figure 3: A schematic sketch of the one and two layer configurations of an extended barrel pixel layer

The scale of the ITk pixel system is unprecedented, with a silicon active area of over 8 m^2 for the baseline layout. The majority will be quad modules, constructed from a single silicon sensor and four (2 by 2) front-end readout chips. The front-end chip is under development, by the RD53 collaboration [4], in the 65 nm CMOS process from TSMC [6]. Assuming the read-out chip will be the same size as the FEI4 [7], used in the ATLAS IBL [8], (360 mm^2), there will be 6400 good modules in the installed system. Reasonable yields have been estimated, based on previous experience, for the various components, as: sensor wafers = 90%, front-end chips = 60%, bump-bonding and flip-chip process = 90%, and assembly construction = 95%. To realise the pixel system therefore requires: 7500 module flip-chips to be started, the bump deposition on 333 wafers (assuming 300 mm diameter wafers), and the production of 1350 6-inch diameter sensor wafers. The start of the production of the pixel system is defined by the delivery of the front-end chip, which is expected in 2018. A pre-production phase to produce 5% of the modules will follow, lasting until mid-2019. Full production of the front-end and sensor will commence at the same time starting in mid-2019. Module production starts as soon as tested components are available and continues for approximately 3 years. Module loading onto the support structures and system integration take place in parallel with module building. The ITk will be integrated into a full system in 2023 followed by a year of system testing on the surface before installation into ATLAS. Given these constraints a major effort is presently being undertaken within the ITk pixel community to identify sufficient low cost, high yield, high volume pixel module assembly vendors to build the system.

3.1 Radiation levels

The radiation background has been simulated for the various ITk layouts under study using the FLUKA particle transport code [9] and the PYTHIA8 event generator [10]. Accurate fluence and dose predictions require an accurate modelling of the geometry and material in FLUKA. The simulations report the 1 MeV neutron equivalent fluence distribution inside the system as this is required to model the damage to the silicon sensors, and the total ionizing dose as this is required to predict the front-end chip performance. The simulation of radio-activation is also performed, as

this is an important input into the design of the system as it dictates procedures for cavern access and detector installation and maintenance. The simulation of the charged particle fluences allow an estimate of the hit occupancies to be made while hadron fluences for energies > 20 MeV provide an estimate of the single event upset (SEU) rate.

The 1 MeV neutron equivalent fluence distribution in the ITk for the LoI layout including the services is shown in Fig 4. This figure shows that the fluence level is reasonably flat along the beam line at low radius. A summary of the radiation background is given in Table 2, for the LoI layout with the endcap pixel rings replacing the disks, but with the LoI services. This shows the unprecedented high dose levels that the system will experience. The dose and fluences of the inner layers are, in fact, sufficiently high that these layers may need to be replaced during operation.

In the ITk strip regions the fluences are dominated by particles coming from interactions in the calorimeter, beam-line and ITk service material. Studies have shown that routing the ITk services out radially away from the beam-line as soon as is feasible is beneficial in reducing radiation backgrounds, including activation. Radiation modelling is an important part of the studies of the pseudo-rapidity coverage of the ITk as material at high Z and low radius increases the radiation levels in the ITk and must be within acceptable limits.

Radiation damage to the silicon sensor increases both its required bias voltage and reverse current, which leads to increased power dissipation. Failure to adequately cool the sensor leads to the sensor warming up due to self-heating, increasing the current and resulting in a positive feedback that results in thermal run-away. Power from the front-end chip causes an additional temperature rise in the sensor and adds to the cooling requirement. Additional cooling implies extra material in the pixel tracker volume, which must be minimized. The power dissipated from the front-end chip must therefore be minimized by design.

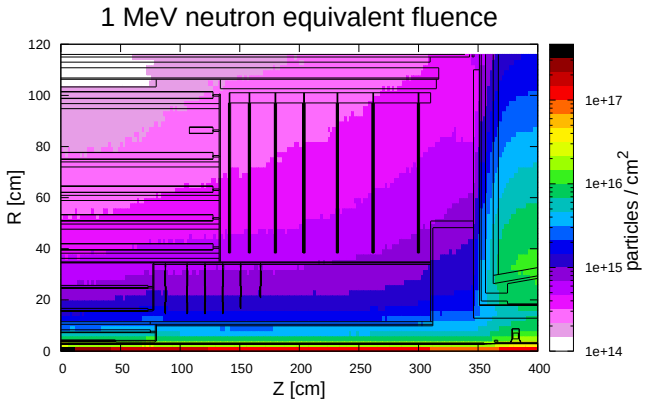

Figure 4: The simulated 1 MeV neutron equivalent fluence distribution in the ITk for the LoI layout [2] for a luminosity of 3000 fb^{-1} of 14 TeV minimum bias events.

3.2 Data rates

The pixel system will have to deal with a huge data rate. The bandwidth requirements for the off-module data transmission are driven by the trigger requirement to allow an average level-0

Pixel structure	Dose (MRad)	Fluence (1 MeV neq 10^{14} cm^{-2})
Inner Barrel	780	134.6
4^{th} Barrel	43	9.4
1^{st} Inner ring	95	17.0
Last inner ring	113	16.1
1^{st} Outer ring	44	8.2

Table 2: Simulated radiation backgrounds in the ITk pixel system for the endcap ring layout and a coverage of $|\eta| < 2.7$ of the ITk, for a luminosity of 3000 fb^{-1} of 14 TeV minimum bias events.

Pixel structure	Module type	Rate per module (Gbps)
Barrel L1	2 chip	5/chip
Barrel L2	Quad	2 x 4
Barrel L3	Quad	5
Barrel L4	Quad	2.5
Inner ring	Quad	2.5

Table 3: Simulated data rates in the ITk pixel system for the endcap ring layout. Assumes that data on a quad module is multiplexed together on the module before transmission.

trigger accept rate of 1 MHz with a latency of 6 μs. The pixel detector will be fully readout at L0 independent of the region of interest and level 1 trigger rates. Simulation shows that the hit rate for the inner barrel pixel layer will be 2 GHzcm^{-2}, for a mean number of interactions per bunch crossing of 200. Assuming an FEI4 chip size results in an output data rate of around 5 Gb/s per chip for the innermost barrel layer and 2.5 Gb/s per quad-module for the outmost barrel layer and the inner most ring, summarized in Table 3.

Such high data rates impose an additional design requirement on the new front-end chip, in addition to the radiation tolerance and low power consumption mentioned above. The high data rate also imposes a design requirement on the data transmission off-chip to the counting house. Due to radiation hardness, space and accessibility, the optical components are not placed in the pixel volume but further outside and therefore the data will be transmitted electrically off the chip and out of the pixel volume over a length of up to 6 m. Investigations on how to transfer such a large amount of high-speed data out of the detector providing an appropriate bandwidth with minimal material is going on.

4. The pixel module

The pixel module is the basic building block of the pixel system. The baseline HL-LHC design is built around the well understood hybrid pixel module concept. The new front-end chip, that will be used throughout the pixel system, will have a pixel size of 50 μm x 50 μm to maintain reasonable hit occupancies in the high track density environment on the inner layers, have sufficiently fast data transmission and low power operation. It will provide a lower noise and threshold (about 1000 e$^-$) than the previous chips, but requires a sensor capacitance (leakage current) less than 100 fF (10 nA) per pixel to achieve this. It will be designed, according to guidelines from RD53 [4] [5],

to achieve predictable performance after a dose of 500 MRad. The chip will operate after a dose of 1 GRad, but the radiation damage models carry a higher uncertainty and performance depends strongly on the exact operating and irradiation conditions. As such the inner layers are designed to be replaceable.

The sensors have a range of requirements depending on their location and are discussed in detail in sub-section 4.1. The interconnect challenges are low cost and high yield of the outer radii and the lowest possible material for the inner radii; highlights of recent developments are given in sub-section 4.2.

4.1 Sensors

The sensor technology of choice is a high resistivity p-type substrate with n-type pixel implants which allows under-depleted post-irradiation operation and removes the requirement for a patterned backside implant, minimizing sensor production costs. Operation under-depleted lowers the sensor power dissipation, reducing the system cooling requirements and therefore material. To further reduce material and dissipated power, the sensor thickness is kept to a minimum.

The outer radii layers dominate the area and therefore cost of the pixel system. Cost reduction is the main development driver. The largest possible wafer size reduces sensor cost per unit area. The traditional sensor suppliers use 6-inch diameter wafers, while production on 200 mm diameter wafers is being investigated with CMOS vendors. Advantages of using a CMOS vendor includes; higher throughput and lower cost, and ability to include multiple metal layers, poly-silicon resistors and capacitors. These features allow resistive biasing networks and in-pixel AC coupling capacitors to be used, which block the large post-irradiation DC current from the readout chip, reducing its design complexity. Prototypes from high resistivity p-type substrates produced by LFoundry and Infineon [11] are being evaluated and show encouraging results. Sensor thickness between 150 and 200 μm is a reasonable compromise between cost and material for the outer radii, thinner sensors cost more due to low yield or complex processing methods. Sensor production is well understood with modules produced from several suppliers that demonstrate the technical requirements [12].

Active CMOS sensors in high voltage technology (HV-CMOS) are also being investigated for the outer layers. The sensor, with in-pixel amplification, giving a smart sensor, is capacitively coupled to the standard front-end chip [13]. The key development to enable CMOS sensors for the ITk is charge collection via drift in a depleted region due to the use of the high voltage process. Such sensors have all the benefits of standard sensors fabricated by a CMOS vendor with the additional benefit of capacitively coupling the sensor to the front-end, reducing interconnect complexity and price. As the sensitive region is only few tens of micrometres thick the sensor can also be significantly thinner.

For the inner most radii radiation hardness, power dissipation and amount of material are the main development drivers. Two sensor options are under development; thin planar and 3D sensors. Thin planar sensors have the benefit of a reduced applied bias to obtain the high electric fields required to maximise charge collection, which reduces the power dissipation from the sensor and therefore lowers the cooling requirements needed to prevent thermal run-away. Planar sensors have been processed as 150 μm thick free standing wafers at Micron Semiconductor Ltd [16], as 50 μm devices by Advacam [17] with the use of a support wafer utilizing wafer bonding, and as 75 μm thick devices using a potassium hydroxide wet etch at HLL [18]. Additionally better material usage

is obtained by reducing inactive material at the sensor's perimeter. Thicknesses as low as 200 μm have been shown on standard planar sensors, while the Advacam wafer bonding process allows side wall doping and a near fully active sensor [17] [18]. The in-pixel detection efficiency has been observed to fall after a high radiation dose due to a lowering of the electric field in the vicinity of the bias dot [19], required for pre-assembly testing of the sensor. Research to overcome this has focused on the routing of the bias rail and minimizing of the bias dot size, and also the development of poly-silicon bias resistors to replace the bias dot [20].

3D sensors have been successfully installed in the ATLAS IBL[19] and are an option for the highest radiation areas of the ATLAS ITk. The 3D sensor requires a significantly lower bias voltage, even compared to 100 μm thick planar sensors, and therefore dissipates less power, which is extremely benefical for the high radiation levels of the inner two layers. At high track incident angles 3D sensors have smaller clusters than planar sensors and are therefore preferred in the high rapidity region. The major areas of development are the reduction of the inter-electrode spacing and smaller column diameter (reducing from 10 μm to 5 μm) to be compatible with the smaller pixel size and higher radiation hardness requirements; and lower sensor capacitance (less than 100 fF per pixel) required by the front-end design to manage noise. To achieve this improved electrode column etching aspect ratios are required or thinner sensors are produced (the same aspect ratio leads to narrower columns) [21]. A thinner detector, while technically challenging, also reduces sensor capacitance as this scales with thickness for a 3D sensor.

4.2 Interconnect

A pixel module consists of the sensor, front-end electronics, and the electrical interconnect between the two. The interconnect is receiving a significant amount of attention for the ITk. Modules in the inner radii must be of minimum thickness, which is a challenge to standard micrometre sized solder ball interconnect technology, while module cost reduction, dominated by the interconnect cost, is the main driver for the outer regions while maintaining low front-end chip thickness. To meet these demands several potential vendors are under investigation and it is expected that three of more will be required for the production.

The interconnect process first requires a solderable metal to be deposited on the exposed aluminium pads of the sensor and readout chip, typically as a post-process stage. Solder balls are deposited on one or both of the wafers, with a preference for the larger readout wafer to reduce cost. The wafers are diced and brought together on a high-precision flip-chip machine to achieve the required alignment of the pixel elements on the two die. The solder can be reflowed on the flip-chip machine or more typically with tin solders the assembly is placed unsupported in a reflow oven in a reducing atmosphere. Flip-chip costs are reduced with the use of the largest wafer sizes, the largest single sensor, presently a quad module $\sim$ 40 x 40 mm^2 and the use of large front-end chips.

The front-end chip consists of a thick substrate silicon wafer (750 μm thick for the FEI4 chip), covered by a thin epitaxial layer (for the CMOS implants) and several metal and dielectric layers (up to 16 μm thick) to connect the various CMOS elements together, known as the back-end-of-line (BEOL) layers. The BEOL layers are deposited at elevated temperature and cause a significant stress in the wafer due to the difference in the coefficient in thermal expansion, CTE, between these layers and silicon. The as delivered wafer is flat due to the mechanical strength of the thick silicon

substrate. To minimize mass the substrate is thinned and the chip bows. At room temperature a 100 μm thick FEI4 chip with bumps has a 100 μm bow [22], measured from corner to centre. A standard solder ball interconnect process requires the wafer to be heated to $\sim$250 °C to reflow the solder. At this temperature the bow in the chip swaps sign and equals 180 μm. Such a large bow prevents the 20 μm high solder bumps making an electrical connection between the senor and readout chip (The sensor does not bow significantly due to the lack of a thick BEOL layer). The pixel assembly will therefore have many disconnected pixel elements typically at its perimeter.

To overcome this the readout chip can be held flat during reflow or the solder reflow temperature can be reduced with the use of indium solder bumps. Two approaches to maintain flatness have been investigated, these are; the use of a temporary thick support wafer bonded to the backside, and a permanent deposition of BEOL layers on the backside of the chip to match the stress from the front side. The ATLAS IBL module was hybridized at IZM [23] using the wafer support process. The wafer was first thinned to 150 μm, then a thick glass wafer was glue-bonded onto the backside of the thinned readout chip wafer. The front-side was processed with electroplated under-bump metallization (UBM) and micro-bump deposition. The sensor wafer also receives UBM, before both parts are diced, and the known-good parts are picked for flip-chip and soldered. Finally, the glass carrier chip is released by laser illumination after flip chip assembly from the module followed by final X-ray and optical inspection. This processed resulted in a high interconnect yield (bump failure rate of $< 3 \times 10^{-4}$), but is slow due to the laser removal step applied at the die level.

The backside BEOL stress compensation layer is under development at CEA LETI [22]. The micro-bumps are processed on the front side of the wafer which is then front-side bonded to a handling wafer. The wafer is thinned to 100 μm. Two layers are deposited on the back side. The first is a $\sim$2 μm layer of high stress dielectric to produce a similar stress as the front side stack at room temperature. This pulls the die flat at room temperature, but has little CTE mismatch with silicon and does not compensate the bow at elevated temperatures. To achieve this a second $\sim$4 μm layer of Al(1%Si) is deposited which reduces the bow at reflow temperatures. The wafer is removed from the handle wafer and diced and flip-chipped in the standard process. Pixel assemblies with high bump yield have been produced and when fully developed this processes is expected to enable higher module through-put than the glass handle wafer technology.

Indium solder bumps were used to make approximately half of the pixel modules in the current ATLAS detector. The indium solder process offers a reduced solder reflow temperature of 90°C [24]. The die still bows and has to be mechanically held flat in the flip-chip machine during the soldering process and only released when the temperature is lower than 50°C. This method has produced high yield assemblies with 100 μm readout chips, however the throughput at the flip-chip stage is compromised due to the time to allow the assembly cool before removing from the machine.

The development of interconnect processes to enable thin module production is an active area of research and over the next year significant number of modules will be produced at a number of vendors to qualify them for production in terms of bump bond yield and device throughput.

5. Conclusions

The development of the new ATLAS inner tracking detector (ITk) for the HL-LHC era is

progressing well. The layout of the tracker to maximise physics return from the expected 3000 fb^{-1} integrated luminosity, is almost complete. A new large area pixel sub-detector is planned that will meet the challenges of an order of magnitude increase in the hit rate, resulting in increases of a similar scale in; module occupancy, data rates and radiation levels. The development of the hybrid pixel module, the basic building block of the pixel system, is presented. Developments of the readout chip to deliver a 50 μm x 50 μm pixel, to cope with the occupancy, are discussed. Sufficient sensor charge collection after the maximum radiation dose has been achieved. The main developments for low cost sensors for the outer radii and thin and low power sensors for the inner radii are presented. The interconnect of readout and sensor is discussed as one of the major areas of development to produce low cost, low mass pixel assemblies on the scale required for the ITk. The major challenges to deliver the pixel sub-detector for the ALTAS ITk are shown to be progressing in a timely fashion to enable installation for the start of the HL-LHC programme.

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