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ATLAS strip detector upgrade for the HL-LHC

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Beginning in 2024, the HL-LHC will provide unprecedented pp luminosities to ATLAS, resulting in an additional integrated luminosity of around 2500 fb^{-1}over ten years. To withstand the much harsher radiation and occupancy conditions of the HL-LHC necessitates a complete replacement of the present inner detector. The new all-silicon tracker design is driven by the performance requirements that cannot be met by the present inner detector. The sensors are designed with finer granularity than the existing tracker to meet the challenges of very high pile-up and to be able to reconstruct tracks in the core of multi-TeVjets. In addition, the replacement tracker has to be much more radiation hard and the readout links need to provide much greater bandwidth. Present ideas and solutions for the strip detector and current research and development program will be discussed.

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1. Introduction

The next major upgrade phase of the Large Hadron Collider (LHC) is currently foreseen to be completed in 2024 [1]. It is called the High Luminosity-LHC (HL-LHC), and it aims to increase the integrated luminosity to about ten times the original LHC design luminosity, resulting in an additional integrated luminosity of around 2500 fb^{-1}over ten years. These data will improve the precision of the measurement of the Higgs properties and enhance the sensitivity to search for new physics.

2. Overview of the phase II ATLAS tracker

2.1 The challenge in HL-LHC operation

As shown in Fig. 1 (a), silicon micro-strip sensors in the upgraded ATLAS experiment at the HL-LHC will be exposed to particle fluences of up to 2×10^{15} n_{eq}/cm^2. Another challenge in HL-LHC operation is that the number of pile-up interactions per crossing will be increased to 140, which is about ten times larger than for the current LHC. The existing ATLAS inner detector (ID) cannot maintain the tracking performance due to this huge increase in the channel occupancy. Therefore, a completely new ATLAS inner tracker is needed for the HL-LHC data taking. The sensors are designed with finer granularity than the existing tracker to meet the challenges of very high pile-up and to be able to reconstruct tracks in the core of multi-TeVjets.

2.2 Baseline layout for new ATLAS tracker design

The new ATLAS inner tracker will be an all-silicon tracker. As shown in Fig. 1 (b), the Letter of Intent design has sensors arranged in cylinders in the barrel region, with four pixel layers followed by three short-strip layer then 2 long-strip layers. The forward regions will be covered by six pixel disks and seven strip disks. Strip layers are double-sided with axial strip orientation on one side. Sensors are rotated by 40 mrad on the other side, giving the second coordinate measurement [2].

The biggest change to the current inner tracker is the replacement of the TRT with 47.8 mm long silicon strips. The outer active radius is slightly larger, improving momentum resolution. The number of strip modules and readout channels will be increased by one order of magnitude compared to current strip detector in this baseline design. In order to improve the granularity, smaller pixels and 23.8 mm long inner strips in barrel are included in this layout. The lengths of the strips in the innermost layers and disk sectors are significantly reduced compared to the current detector.

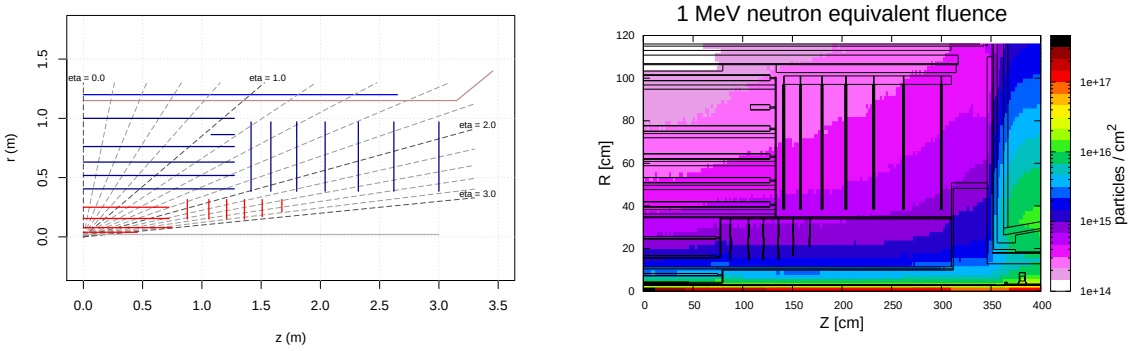
2.3 Expected Performance of the new ATLAS inner tracker

Fig. 2 (a) shows the expected hit occupancies as a function of *r*-*z* with 200 pile-up events. Due to the high granularity and large number of readout channels, the hit occupancies are less than 1% for the whole inner tracker region.

The expected momentum resolution in the future ATLAS tracker shows a significant improvement compared to the current detector, due to more precise hit positions measurement and a longer lever arm.

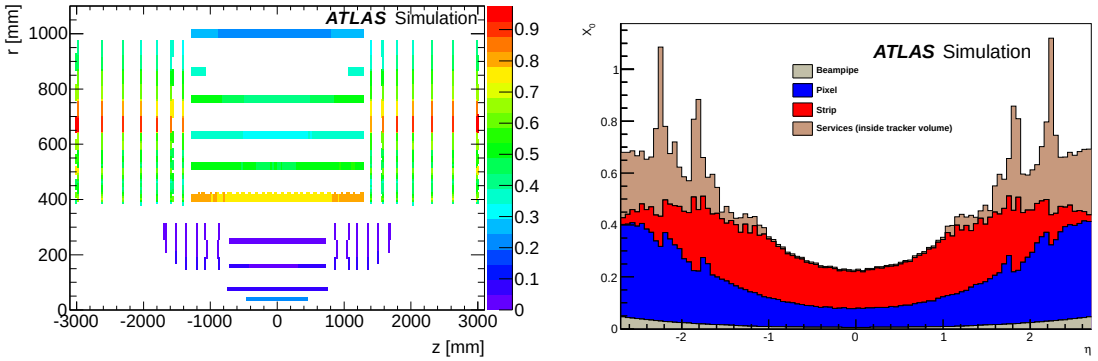
The tracking efficiencies for muons in the presence of 140 pile-up events have been found to be close to 100% in new ATLAS tracker. The longer barrel with respect to the current inner detector also moves the difficult transition region to higher $|\eta|$.

To improve tracking performance in general, amount of service material inside the tracking volume has been minimised. As shown in Fig 2, the expected material distribution in the new ATLAS tracker is significantly lower with respect to the current ID. For example, the current ID contributes $> 1.2\ X_0$ for all regions with $|\eta| > 1.36$, while the new tracker remains below $0.7\ X_0$ up to $|\eta| = 2.7$, excepting a few small regions.



(a) (b)

Figure 1: (a) The Letter of Intent layout for the future ATLAS tracker. (b) *R*-*z* map of the 1 MeV neutron equivalent fluence in the Inner Tracker region, normalised to 3000 fb^{-1} of 14 TeV minimum bias events generated using PYTHIA8.



(a) (b)

Figure 2: (a)Channel occupancies (in percent) with 200 pile-up events. (b)The material in X_0 as a function of η for the Phase-II tracker layout.

3. The Layout of Strip Detector

The upgrade strip detector consists of a central barrel region between $\pm$ 1.3 m in z and two end-caps, that extend the length of the strip detector to $\pm$ 3 m. They cover $\pm$ 2.5 units of pseudo-

rapidity. The stave shown in Fig. 3 (a) is the basic building block of the barrel, which is designed to minimise material for large scale assembly and easier replacement [3]. It consists of a low-mass central stave core that provides mechanical rigidity, support for the modules, and houses the common electrical, optical and cooling services as shown in Fig. 4. A core of carbon fibre honeycomb and carbon foam with embedded cooling pipes is sandwiched between two carbon fibre facings.

The petal core, shown in Fig. 3 (b), cools and supports end-cap modules. It uses the same materials as stave cores. However there are a few difference between them. First of all, the petal core is wedge shaped, with the cooling tube approximately V-shaped. Each module in the outer three rings is cooled by a single length of tube, while the inner three modules, which have higher power densities, are cooled by two lengths of tube, similar to a stave.

Staves are arranged in concentric cylinders centred on the beam-line as illustrated in Fig. 5 (a). The staves are rotated by a small angle (the tilt-angle) away from the tangent to allow an overlap in the ϕ direction. The arrangement for endcap module is indicated in Fig. 5 (b). There are seven disks with each having 32 petals, in total 446 petals per end-cap.

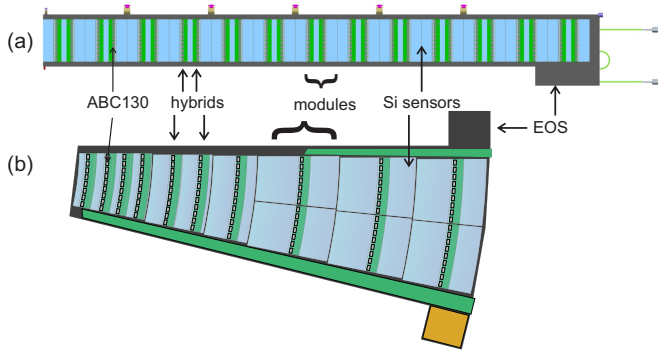


Figure 3: (a) Barrel stave components. (b) Endcap petal components

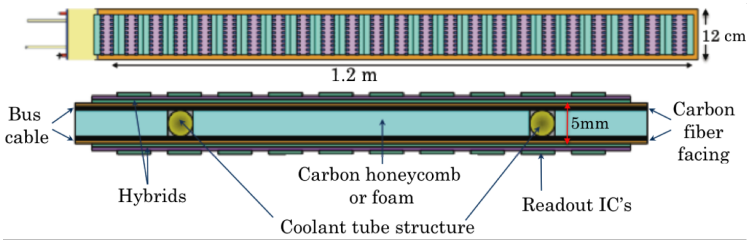
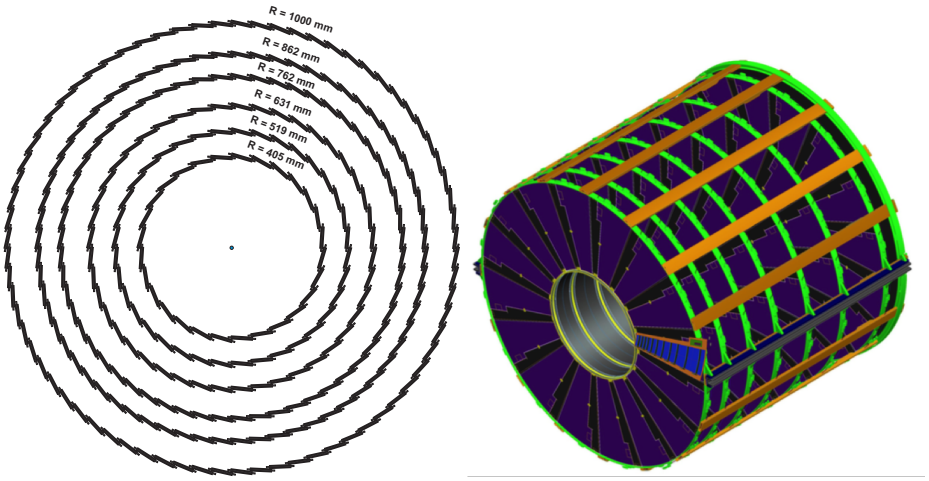


Figure 4: Cross section of a stave.

4. Silicon Sensors for Strip Detector Upgrade

The current ATLAS strip detector uses silicon strip sensors made with p-strips implanted on n-type silicon bulk (p-in-n), and it is designed to operate up to $2\times10^{14}n_{eq}/\text{cm}^2$. In order to maintain the detector performance for the full HL-LHC lifetime, new sensors are needed to operate when exposed to particle fluences of up to $2\times10^{15}n_{eq}/\text{cm}^2$.



(a) (b)

Figure 5: (a) Arrangement of staves in barrels. Staves are tilted 10 degrees (b) Arrangement of petal in endcaps

4.1 Baseline Solution: n^+-in-p type sensor

The baseline proposal for the new radiation hard sensor is called n^+-in-p type sensor. This type of sensor collects electrons and has no radiation-induced type inversion [4]. The size of the barrel sensors is 97.54 x 97.54 mm^2 to maximally utilize the area of a 6 inch wafer. There are 1280 strips across a sensor, giving a strip pitch of 74.5 μm.

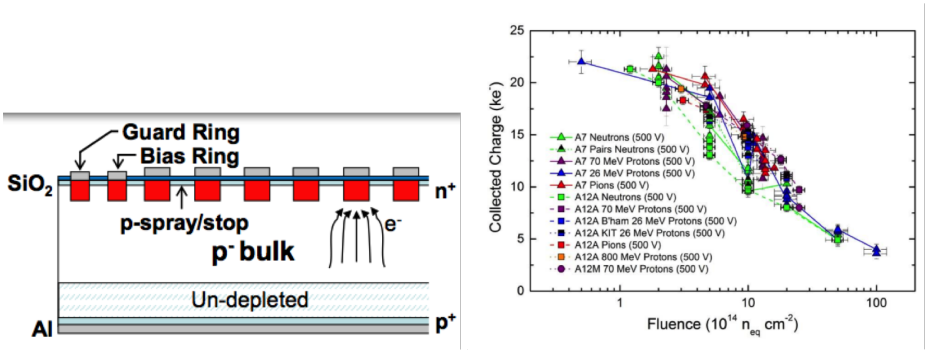
Two rounds of prototyping (ATLAS07 and ATLAS12) of such sensors have been fabricated by Hamamatsu Photonics [5, 6]. The radiation hardness of these prototype sensors have been measured. The charge collected in prototype sensor ATLAS12 as a function of the fluence after irradiation with different particles is shown in Fig 6 (b). According to these measurements, the new type of sensor can still collect about 10 thousand electrons after an integrated luminosity of 3000 fb^{-1}(which corresponds to a fluence of $2\times10^{15} n_{eq}$/cm^2). The signal-to-noise ratio in this sensor at the end of HL-LHC operation is above 17.

The full depletion voltage of this prototype sensor rises as irradiation fluence is increased. When exposed to a fluence of $2\times10^{15} n_{eq}$/cm^2, the depletion voltage is greater than 1000 V. It is expected that the sensors will operate partially depleted at the end of the HL-LHC operation. The isolation between strips (the inter-strip resistance) degrades strongly with proton and gamma irradiation. However, inter-strip resistance is much larger than the typical amplifier's input impedance when exposed to a fluence of $2\times10^{15} n_{eq}$/cm^2. Therefore, the expected strip isolation is still good enough to maintain the spatial resolution of the strip detector at the end of HL-LHC operation.

4.2 Alternative Solution : CMOS Sensor

An alternative solution is to use the commercial CMOS (HV/HR) technologies for strip sensor. This type of sensor collects electrons in a deep N-well on p-type substrate as shown in Fig. 7.

CMOS sensors can provide higher granularity and reduce costs in sensor fabrication. Furthermore, CMOS-based sensors collect charge from a thin depleted region, and the bulk can be thinned down to 50 μm thus reducing material in the new ATLAS strip detector. However, it has

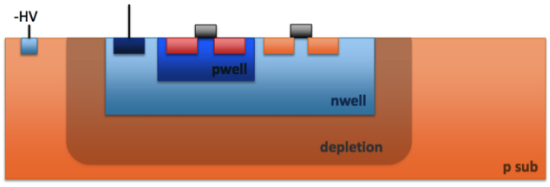


(a) (b)

Figure 6: (a) Cross section of (n^+-in-p) strip sensors in baseline design (b) Collected signal charge in prototype sensor ATLAS12 at 500 V bias voltage for minimum ionising particles as a function of 1 MeV n_{eq}/cm^2 fluence for various types of particles.

a drawback that the total collected charge from minimum ionizing particles is about one order of magnitude lower than the charge from a conventional planar sensors. A low-noise built-in amplifier on the sensor chip has been designed to improve the signal-to-noise ratio [7].

A 3-year program began in 2014 to investigate the use of CMOS sensors in ATLAS strip detector upgrade. The goal of the of the first year is to characterize basic sensor and electronics properties as well as architecture. The main goal in year two is to manufacture a large scale sensor with close to full functionality, to evaluate its radiation hardness and to characterize hit efficiency, charge collection speed and signal-to-noise ratio. The goal in year three will be to make a full module prototypes with full scale sensors and readout electronics.

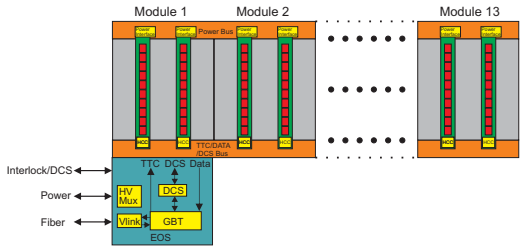


(a)

Figure 7: Cross section of a CMOS-based sensor for ATLAS strip detector upgrade

5. Front-end electronics

The main electrical components of a short-strip stave are shown in Fig. 8 [2]. Two hybrids are designed to be mounted on each silicon sensor. Each of the hybrids contains ten ABC130 readout chips in a 130 nm CMOS process. Each hybrid has a Hybrid Controller Chip (HCC) that interfaces the ABC130s to the End of stave card (EOS). Trigger, Timing, and Control (TTC) signals are sent from the EOS to each HCC via the TTC/DATA/DCS bus. The powering is still under investigation and studies are being conducted both on DC-DC and serial powering. The high voltage will be multiplexed with powering on a single line per stave with switches.



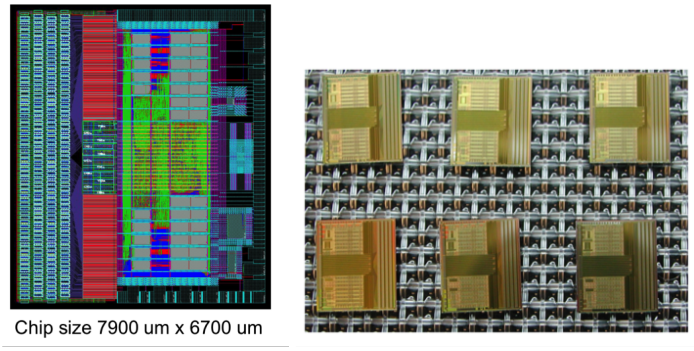
(a)

Figure 8: Overview of main electrical components.

5.1 Readout Chip

The first round of prototype readout chips (ABCN250 chip) used the IBM CMOS 250 nm process. It has 128 readout channels. There are individual preamplifier, shaper, comparator, memory banks for trigger latency and a derandomizer for each channel. The shaper has been designed to have less than 25ns peaking time for LHC operation.

The ATLAS strip upgrade community has designed and manufactured the readout chips for the second round of prototyping. The biggest change in the second round of prototyping was switching to use the IBM 130 nm technology. The new prototype readout chip (ABC130) has more channels (256 readout channels). The power consumption of ABC130 chip is much lower compared to ABCN250. Furthermore, the ABC130 chip has a smaller size which helps to reduce the material in tracker volume. The drawing and the photograph of the ABC130 are shown in fig. 9.

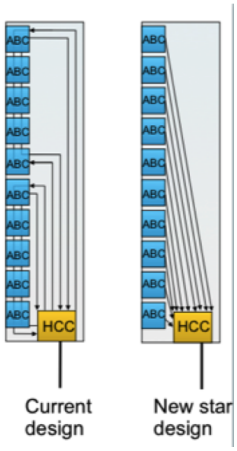


(a) (b)

Figure 9: (a) The drawing of ABCN readout ASICS chip in 130 nm CMOS process. (b) Photograph of six ABCN readout ASICS chips in 130 nm CMOS process.

5.2 The latest development in Hybrid Controller chip (HCC)

ATLAS raised the trigger rate specifications thus requiring a higher readout speed. It now requires 1MHz in L0 triggers and 400kHz in L1 triggers. In order to improve the readout speed, a new "star" architecture is in development. Fig. 10 compares the current HCC design with future HCC star architecture design. The new design has potential to reduce the size of data packets and make full use of the bandwidth of the front-end chips. Furthermore, the event building process will be done in the HCC in the new design, which helps to reduce the latency.



(a)

Figure 10: A comparison between the information flow between the current HCC design and the future HCC design.

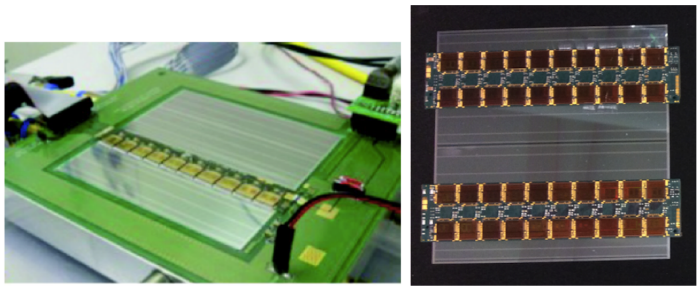
6. The Latest Development in Module Prototyping

The ATLAS strip upgrade community used the ABCN250 readout chip and the ATLAS07 n^+-in-p sensor for the first round of module prototyping. Nine different sites were involved in the first round of module prototyping. More than 200 hybrids and 85 module prototypes have been produced in the past few years. A strong world-wide community has been built up for future module development. During the first round of the prototyping modules were tested with both DC-DC and serial powering schemes. They show a similar noise behaviour with low values of around 600 electrons. After irradiation an 10% level increase of the noise was measured as expected. Since the signal collected by the n^+-in-p sensors is about ten thousand electrons after irradiation, the signal-to-noise ratio of the strip detector will still be very good at the end of HL-LHC operation.

This community is switching to the second round of module prototyping. The biggest change in this round is to replace the ABCN250 chip by the ABC130 chip. The first module with the ABC130 chip has been produced. The photographs of the modules in first and second round of prototyping are shown in Fig. 11. Since there are twice as many readout channels in the ATLAS130 chip, the number of readout chips per module in the new prototype have been reduced by half compared to the first prototype. The hybrid design is more compact in the new prototype. The power consumption of a hybrid on new module prototype with ten ABC130 readout chips is only 3 watts, and it is one order of magnitude better than the previous prototype with the ABCN250 chips.

7. Stave and Petal Prototyping

Both a full size DC-DC powered stave and a serial powered stave prototype with the ABCN250 chip has been built. A photograph of a barrel stave with ASICS in 250 nm CMOS process is shown in fig. 12 (a). The construction, shielding, grounding, powering and readout performance have also been tested. The noise of a module on a stave is similar to the noise of a single module. The drawing of a stave prototype in the next round of stave prototyping is shown in Fig. 12 (b). Besides

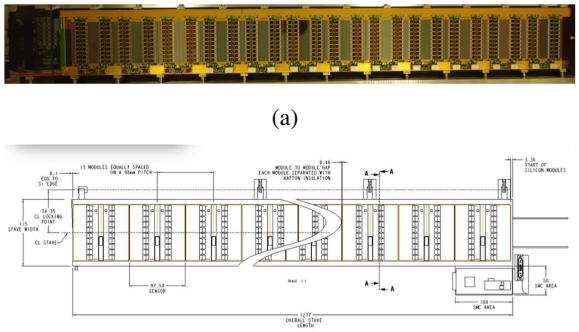


(a) (b)

Figure 11: (a) Silicon sensor module for the barrel region with ASICS in 130 nm CMOS process. There is only one of the two hybrids mounted. (b) Silicon sensor module for the barrel region with ASICS in 250 nm CMOS process.

the change due to the new ABC130 readout chip, the biggest change is the DC-DC powered stave. A novel design of the on-sensor DC-DC converter reduces the thickness of the DC-DC converter significantly.

In endcap region prototyping, a reduced-size petal (so called petalet) has been built. A drawing of a petalet is shown in Fig 13 (a). The petalet is DC-DC powered. Two different layouts are investigated for readout. The first has two upper hybrids, one on each sensor and with data and power routing on one side (the so-called Lamb and Flag). The second has a single upper hybrid bridging over both sensors with data and power on different sides (the so-called Bear). Both layouts are being studied in detail to select one for the petals. The petal sensors need radial strips (i.e. pointing to the beam-line) to give an accurate measurement of the $r\phi$ coordinate. As a result the petal sensors have a wedge shape as shown in Fig. 13 (b).



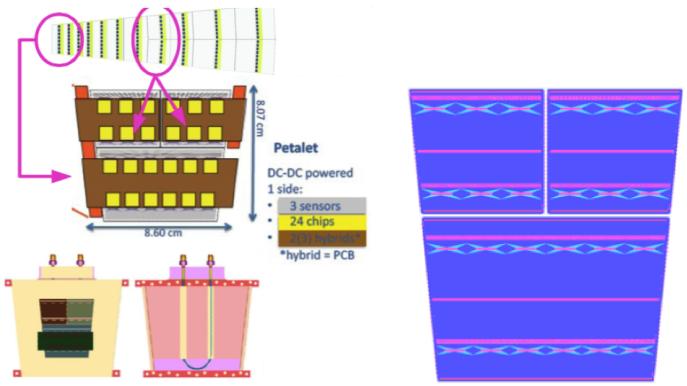
(a)

(b)

Figure 12: (a)Photograph of a barrel stave with ASICS in 250 nm CMOS process. (b) Drawing of a barrel stave with ASICS in 130 nm CMOS process

8. Summary

A new all-silicon tracker will replace the current ATLAS tracking detector for HL-LHC data taking, as driven by the tracking performance requirements. The layout, expected performance and



(a) (b)

Figure 13: (a) Drawing of a endcap petalet with ASICS in 130 nm CMOS process. (b) A endcap sensor prototype

latest status of prototyping of a new silicon strip tracker for the ATLAS experiment at the HL-LHC has been shown.

To withstand the much harsher radiation in HL-LHC, prototypes of radiation hard n^+-in-p sensors have been fabricated and tested. The tests verify the radiation hardness of this type of sensor fulfilling the requirements of HL-LHC operations. A new version of the readout chip ABC130 with the IBM 130 nm CMOS process has been fabricated, and it shows good performance in power consumption with respect to the previous version, the ABCN250. In the latest round of module prototyping, the size of the hybrid, power consumption and the number of ASICs per module have been reduced, benefitting from the new feature of ABC130 chip.

The stave (petal) is designed as the basic element of the barrel (endcap) for large scale assembly in the new strip detector. Both a full size DC-DC powered stave and a serial powered stave prototype with ABCN250 chips have been built. In endcap region prototyping, a reduced size of petal (so called petalet) has been built and tested. Both the staves and petalets show good performance in shielding, grounding, powering, cooling and readout testing.

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