

The Upstream Tracker for the LHCb upgrade

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The upgraded LHCb detector will run at an instantaneous luminosity of $2 \times 10^{33} \text{ cm}^{-2}\text{s}^{-1}$ and have 40 MHz readout. In order to cope with the higher data rate and faster readout speed the silicon microstrip detector located upstream of the dipole magnet will be replaced by the Upstream Tracker (UT). This system consists of four silicon microstrip planes, read out with a custom ASIC (SALT), which is currently being developed. Considerable progress has been achieved on the UT design. In addition a program of irradiation and test beam studies has been started. Key findings will be summarized.

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1. Introduction

The LHCb experiment is dedicated to study CP violation and other rare phenomena in the decays of beauty and charm particles at the LHC. It has produced interesting results since the first successful pp collisions in 2010. The current LHCb detector trigger and readout system is optimized to run at a nominal instantaneous luminosity of $2 \times 10^{32} \text{ cm}^{-2} \text{ s}^{-1}$, and collect 10 fb^{-1} data. The maximum readout speed is 1 MHz [1].

In order to enhance the experiment's sensitivity by an order of magnitude, the LHCb experiment will have an upgrade around 2019 and operate at instantaneous luminosity up to $2 \times 10^{33} \text{ cm}^{-2} \text{ s}^{-1}$. All detector elements will need new front end electronics featuring 40 MHz readout. In addition the trigger will be fully software based, which will allow a significant increase in efficiency especially for hadronic final states [2].

The current silicon microstrip detector, TT, located upstream of the dipole magnet in the current LHCb detector, will be replaced by the Upstream Tracker (UT) [3, 4, 5]. The UT tracker consists of four silicon microstrip planes, read out with custom SALT ASIC, currently being developed [6]. The silicon-SALT hybrid circuits are connected with near-detector electronics via low mass flex cables. UT silicon sensors will work in a high radiation environment and need to be operated at low temperature ($\leq -5^\circ\text{C}$), using cooling provided by an evaporative CO_2 system. Sensor modules are mounted on low mass reinforced carbon fiber sandwich structure called "staves," which integrate Ti cooling tubes.

Considerable progress has been achieved on the design of components required for this system, and will be described in this note. In addition a program of irradiation and test beam studies has been started. Key findings will also be summarized.

2. The UT in the LHCb tracking system

The current LHCb tracking system consists of a vertex locator (VELO) that surrounds the interaction region, the Tracker Turicensis (TT) located just upstream of the dipole magnet, and tracking stations (T) located just downstream of the magnet [1]. All three detectors are being upgraded. The relative locations and different type of reconstructed tracks are illustrated in Fig. 1. The VELO detector will use silicon pixels [7, 8, 9]. The tracking stations downstream of the magnet will be replaced with a scintillating fiber (SciFi) system [3]. The UT will use silicon strip technology with improved segmentation and acceptance.

The UT serves as a link between the VELO and T station trackers. Long tracks are constructed with matched VELO and T track segments, with or without UT hits. They are directly used in all physics analyses. By requiring hits on at least 3 out of 4 UT planes for tracks within the UT fiducial volume, ghost tracks are significantly reduced while good tracks are reconstructed with efficiency close to 100%, as shown in Fig. 2a.

In the upgraded detector all events will be read out at 40 MHz. A fully software based trigger will be used to keep interesting events for further processing. For use in the trigger algorithm tracks need to be reconstructed, and their momenta be measured. The UT detector is just before dipole magnet and there is a small magnetic field in the detector volume. A fast momentum determination may be made by simply matching VELO and UT segments. The precision is sufficient to separate

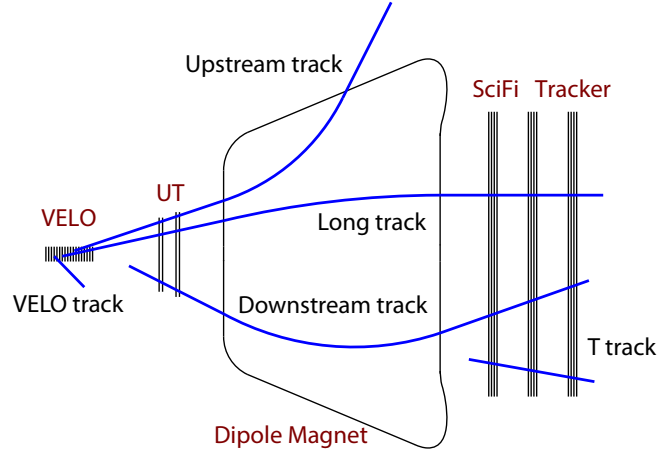


Figure 1: Locations of the detectors and reconstructed track types in the LHCb upgrade tracking system.

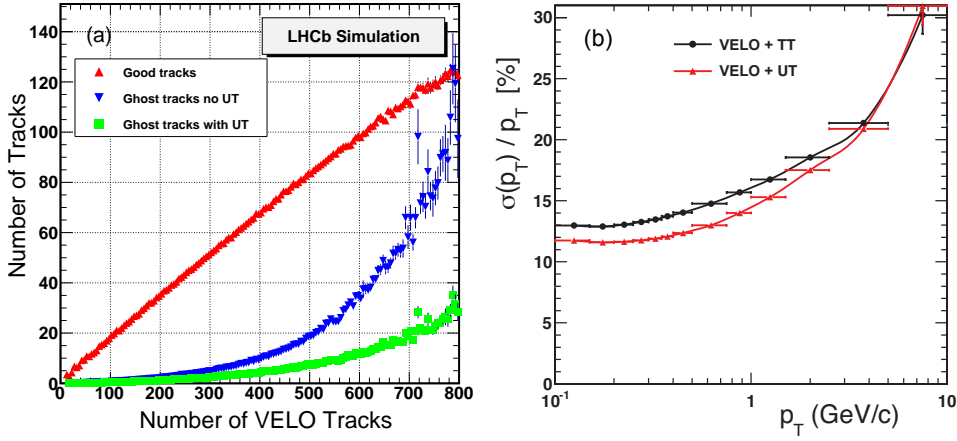


Figure 2: Simulation of inclusive b events at $\mathcal{L} = 2 \times 10^{33} \text{ cm}^{-2} \text{ s}^{-1}$. (a) Average number of long tracks in different categories as a function of number of all tracks that contain VELO-segments: good tracks, ghost tracks with or without UT hit requirement. The UT requirement is not applied to tracks out of the UT fiducial volume. The number of VELO tracks peaks at ~ 290 . (b) Track transverse momentum resolution using only VELO and UT (TT) segments.

uninteresting low momentum tracks, generally below several GeV, from high momentum tracks, as shown in Fig. 2b. With charge sign of the tracks determined and soft tracks (*e.g.* $p_T < 400 \text{ MeV}$) rejected, combinations in long track reconstruction are reduced by about a factor of 5. Thus the trigger processing speed can be significantly increased.

With much improved segmentation and coverage of the UT detector, reconstruction efficiency of long lived particles, *e.g.* $K_s \rightarrow \pi^+ \pi^-$, $\Lambda \rightarrow p \pi^-$, can be much improved. Downstream tracks which have segments only in the UT and the SciFi detectors account for a significant portion of their final decay products.

3. The UT detector geometric configuration

The UT detector has four planes (UTaX, UTaU, UTbV, and UTbX) of silicon strip sensors as shown in Fig. 3. The sensors have finer granularity comparing to TT to cope with an increased particle density. Sensor strips are vertical to have precise measurement in the horizontal direction, the direction that charged tracks bend in the dipole magnet. The middle two planes, UTaU and UTbV, are at small angles ($\pm 5^\circ$) for stereo measurements. The distance along the beam direction (Z) between the first and the last planes is 315 mm. Intervals within the four planes are to be further optimized. The detector covers about ± 255 mrad vertically and ± 310 mrad horizontally. There is a circular cut of 33.4 mm in radius in the center for the beam pipe. Due to 0.8 mm wide guard ring surrounding the sensor, the smallest detection radius is 34.2 mm, corresponding to a ~ 14 mrad azimuthal angle.

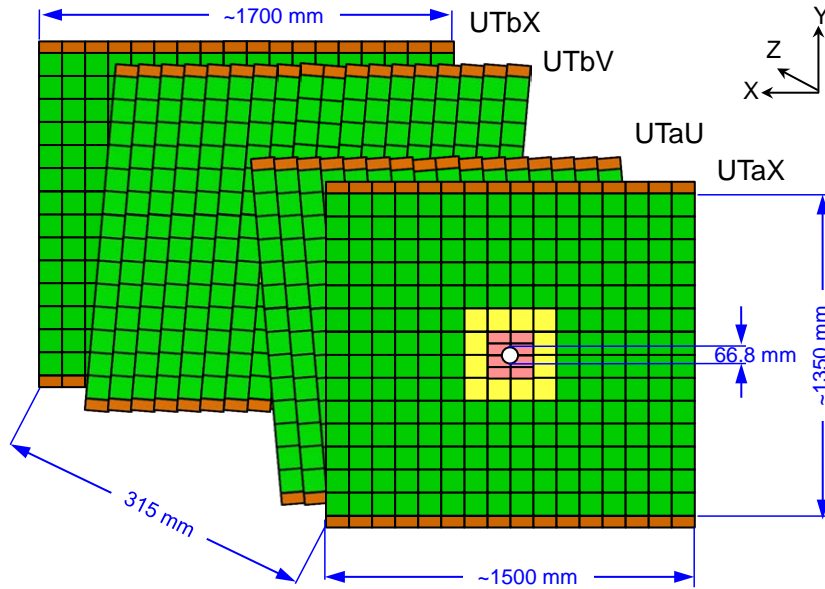


Figure 3: The UT detector has four planes made of 16 or 18 staves per plane. The four types of sensors are color coded: type-A (green), type-B (yellow), type-C (light red), and type-D (light red) with a circular cut.

Each plane is constructed from 16 columnar structure called “staves” for UTaX and UTaU, and 18 staves for UTbV and UTbX. Staves within a plane are staggered in Z and have small horizontal angular overlaps for full angular coverage. Most have 14 sensor modules per stave, mounted alternatively on the front and the back surfaces of its support structure for vertical overlaps. Central staves have 16 modules per stave due to 4 half-length sensors in the middle. A module consists of 1 sensor, 4 or 8 SALT ASICs, a hybrid circuitry, and a stiffener. More details of the stave structure and the module structure will be discussed in Section 6.

The UT has four different types of silicon sensors regarding their shapes, sizes, and strip pitches. Sensors that are closer to the beam pipe have higher segmentation, because the particle density is significantly higher at small radius than at large radius. The four sensor types are denoted

A, B, C, and D, starting from the outer sensors as shown in Fig. 3. Type-A sensors, shown as green boxes, account for $\sim 92\%$ of all sensors. The sensor overall size is $97.5 \times 99.5 \text{ mm}^2$, with a guard ring width of $800 \mu\text{m}$. It has 512 strips of $187.3 \mu\text{m}$ pitch, 97.9 mm length. Type-B sensors have the same size as type-A, but have half the strip pitch ($93.7 \mu\text{m}$), hence double the number of strips (1024). The length of type-C or type-D sensors is roughly half that of type-B sensors. The strip pitches and the numbers of strips are the same. The type-D sensors have a cut at one corner, so that a circular hole can be formed in a sensor plane, which fits the beam pipe. This maximizes the acceptance of the UT detector at small angles.

4. Silicon sensor R&D

The silicon sensors operate in a high radiation environment. For 50 fb^{-1} data collection the inner most part of the UT sensors is exposed to $\sim 5 \times 10^{14} \text{ n}_{\text{eq}}/\text{cm}^2$ (1 MeV neutron equivalent) particle fluence, or $\sim 40 \text{ MRad}$ radiation dose. This is determined from a simulation with safety factors included.

The inner sensors (types B, C, D) use the highly radiation tolerant n^+ -in-p technology, which sometimes are called p-type sensors for short [10]. Type-A sensors are in regions of relatively lower radiation level and form the majority (92%). It may use p^+ -in-n technology (n-type sensor) due to the relatively lower cost. The SALT ASIC can operate with input signals of both polarities. The thickness is $320 \mu\text{m}$ for type-A sensors, and $250 \mu\text{m}$ for types B, C, D sensors.

The UT sensor R&D program has several phases. Mini-sensors of $\sim 11 \times 11 \text{ mm}^2$ in size were extensively studied in phase I. The strip pitch of the mini-sensors is $80 \mu\text{m}$, smaller than the baseline sensors. Both p-type and n-type mini-sensors were produced. Different guard ring structures were implemented in type-D sensors around the circular cut.

The mini-sensors were irradiated in a 226 MeV proton beam at the Burr Proton Therapy Center (PTC) of the Massachusetts General Hospital (MGH) [11], up to $\sim 4 \times 10^{14} \text{ n}_{\text{eq}}/\text{cm}^2$ particle fluence. The irradiated mini-sensors were wirebonded to Beetle chips that were designed for the current silicon strip detectors [12], and read out with an Alibava DAQ system [13, 14]. The sensors were tested in an 180 GeV proton beam at CERN [15]. A TimePix3-based telescope was used to provide tracking precision of $\sim 2 \mu\text{m}$ on the detector under test [16].

The sensors were biased at different voltages, ranging from 50 V to 500 V . Signal charges were measured from hit clusters. The distribution fits well with a Landau function. The most probable value of the Landau distribution vs. the bias voltage are shown in Fig. 4.a. With increased radiation dose the full depletion voltage of p-type sensor also increases. For all sensors the charge collection efficiencies reach plateau when the sensors are biased at $300\text{-}400 \text{ V}$. There is also a gradual loss in total charge collected for p-type sensors. The signal to noise ratio for the highest irradiated sensor is ~ 15 . It is projected that after 50 fb^{-1} running the full size sensors will maintain reasonable signal to noise ratio.

Spatial resolution was also measured, at a bias voltage larger than the full depletion voltage. Resolution as a function of track impact angle is shown Fig. 4.b. At normal incidence the n-type sensor has very little charge sharing. About 87% of tracks produce only single strip hits. With increasing impact angle there is more charge sharing, thus the spatial resolution is better. The worst resolution at normal incidence is about $23 \mu\text{m}$, approximately $80/\sqrt{12}$. The best resolution

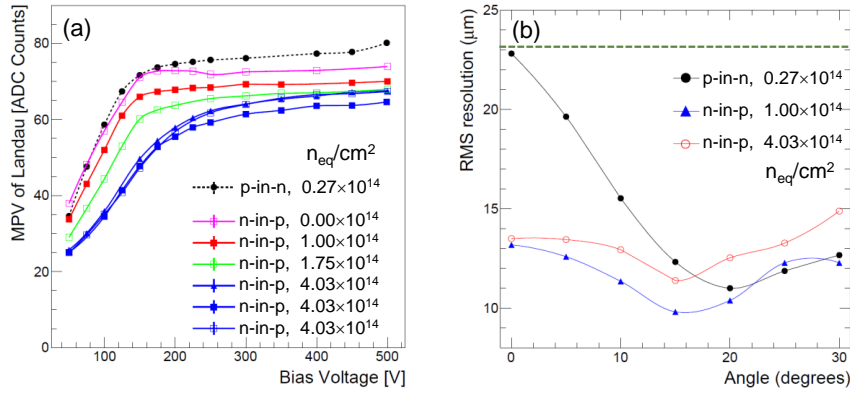


Figure 4: (a) The most probable value of the collected charge from the Landau fit as a function of bias voltage for different sensors and irradiation levels. Tracks are at normal incidence to the sensor. (b) Spatial resolution as a function of the track incident angle.

is at $\sim 20^\circ$. Highly irradiated p-type sensors have more charge sharing at normal incidence and better resolution than the n-type sensor. Comparing the p-type sensors, the one that was exposed to higher radiation exhibits worse resolution. The level is $\sim 2 \mu\text{m}$ in the worst case and is not a big concern.

Strip pitches of types B, C, D sensors are $93.7 \mu\text{m}$, and not much wider than $80 \mu\text{m}$, the pitch of input pads on the SALT ASIC. Thus the sensor strips can be directly wire-bonded to the SALT input pads. Type-A sensors, however, have much larger strip pitch of $187.3 \mu\text{m}$. A pitch adapting mechanism is needed, which is one of the main focuses during the phase II sensor R&D.

Two different embedded pitch adapters are implemented in half-width type-A prototype sensors. The prototype sensors also provide different biasing schemes: HV connection from the backside, or from the top side via bias ring with backside passivation. The IV and CV curves of type-A sensors are shown in Fig. 5. Most sensors have soft breakdown starting around 500 V. Two sensors break down at about 180 V. One of them has a deep scratch on the backside metalization layer, which can be avoided in the final production. The other is under study and the reason is yet to be determined.

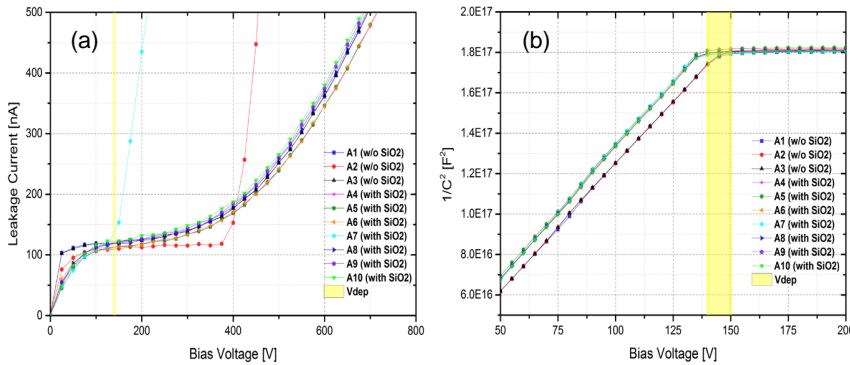


Figure 5: (a) IV curves, and (b) CV curves of half-width type-A sensors. Sensors A4-A10 are biased from top and have passivation at backside. Sensors A1-A3 are biased directly from backside.

Several type-A sensors have been irradiated at CERN IRRAD facility, with doses up to 1 MRad, the level that the inner most pitch adapters will receive after 50 fb^{-1} running. Irradiated sensors and non-irradiated reference sensors have been tested in a proton beam at CERN. The analysis is on going and will determine whether the pitch adapters function properly after 50 fb^{-1} running, and whether they introduce inefficiency near the pitch adapter. In parallel, an external glass pitch adapter solution is also being explored.

Another focus of the phase II sensor R&D is the type-D sensors (with circular cut-outs). Prototype sensors have been produced. Their IV, CV properties are similar to that of type-A sensors. The type-D sensors have been irradiated up to $5 \times 10^{14} \text{ n}_{\text{eq}}/\text{cm}^2$ particle fluence, and tested in the proton beam. The beam was focused on different areas of the sensors, so as to measure the sensor performance, especially near the circular cut. The analysis is on going.

5. Signal readout chain

The UT readout chain is illustrated in Fig. 6. It complies with the LHCb upgrade readout architecture [17, 18].

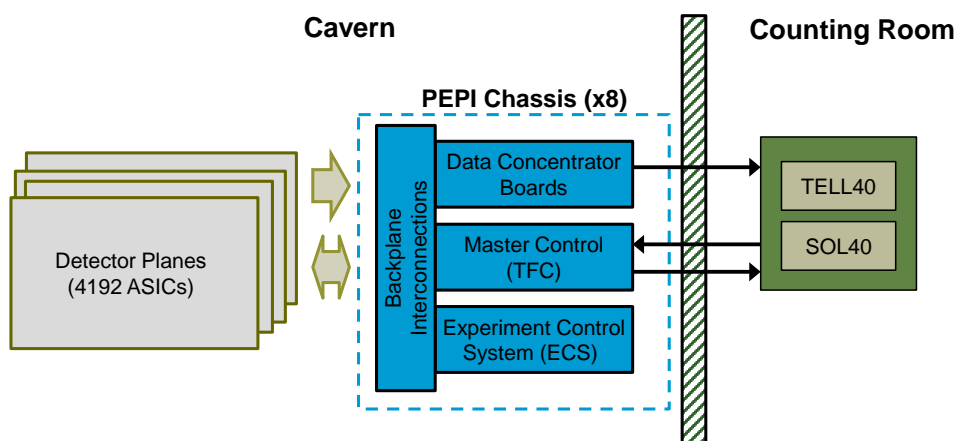


Figure 6: UT signal read out chain.

The UT silicon strips are wirebonded to the input pads of the SALT ASICs. Each ASIC has 128 input channels that have a preamplifier and a 6-bit ADC per channel. Type-A sensors need 4 ASICs per sensor to process signals from 512 strips. Type B, C, D sensors need 8 ASICs per sensor for 1024 strips. The sensor, ASICs and electronic hybrid circuitry are glued to a ceramic stiffener to form a UT module.

At the early stage of the SALT design, the IBM 130nm CMOS technology was used. Later the TSMC technology was used instead. The SALT ASICs are designed to process input signals from every bunch crossing at a 40MHz rate. The sensor strips are connected to the inputs of the ASICs through AC coupling. The dynamic range of the signals is $\sim 30,000 \text{ e}$, of both polarities. The signal peaking time is less than 25 ns, with the remainder of the signal at 25 ns after the peak of $\sim 5\%$. The spill over hits produced are about 3%, and are rejected later. Signals are sampled at the peak and digitized by 6-bit SAR (successive approximation register) ADCs. The noise performance is

expected to be $ENC \sim 1000 e@10 \text{ pF} + 50 e/\text{pF}$, with the sensor capacitance ranging between 5-20 pF.

The digitized signals are processed by a build-in DSP (digital signal processor), which contains several stages in the following order. Configuration parameters for all stages are stored in registers on the chip. At the first stage all bad channels are flagged, and are not used further. Then a pedestal is subtracted from the signal in each channel. The per channel pedestal values and the list of bad channels are obtained from special calibration runs. The common mode (CM) fluctuation of the whole chip is calculated in each event from the pedestal subtracted signals of channels that have no real signal. Once the CM fluctuation is determined, it is subtracted from the signals in all channels. After CM suppression, channels with signal over a pre-configured per chip threshold are considered real hits. Data of all hits including their channel IDs and the CM suppressed ADC values are saved in a memory buffer, to be transferred out.

The SALT ASICs send out events in a bit-stream of a pre-defined event packet format, which includes two fields: a header field and a data field. The header field contains the bunch crossing ID and the size of the data field. The data field contains all hit data. In some cases the data field is not present, *e.g.* there are no hits in an ASIC. It is required that the ASIC sends out one event packet per bunch crossing.

The SALT ASICs transfer event packets out as differential SLVS signals from build-in e-ports, each operates at 320 Mbps, *i.e.* 8 bits per 25 ns clock cycle. Multiple e-ports (3-5) will be activated per ASIC, which transmit data coherently as one lane. The number of active e-ports is determined from the ASIC data rate and configured at the construction stage.

The data transmission is not fully synchronized with the bunch crossing, due to fluctuation of the event data size. It takes longer than 25 ns for a busy event, and shorter for a no-hit event. The memory buffer where hit data are stored acts as a derandomizer to take care of the fluctuation. The number of active e-ports configured is to ensure that the average time needed is less than 25 ns. When there are not enough data to occupy all e-ports, special idle packets are generated so that the data bit stream contains packets with no interruption. This is essential to data decoding at a later stage, which relies on a complete packet to determine the starting bit of the next packet.

Four low mass flex cables per stave connect the UT modules to the electronics in the PEPI (peripheral electronics processing interface) volume. The busiest cable hosts ~ 240 signal lines, 6 sets of LV power, return and sense lines, and 4 pairs of HV power and return. The module hybrid circuits are connected along the flex cable through wirebondings. At the other end, the flex cable connects to the PEPI electronics via 400-pin MegArray connector and a pig tail cable.

On the data concentrator boards (DCB) in the PEPI volume, event data from ASICs are passively grouped into GBT frame data by GBTx chips. One GBTx chip connects to 2-4 ASICs. The data from the GBTx chips are converted from electronic signal to optical signal and sent out by versatile links to TELL40 boards in the counting room. Data are then decoded and regrouped at the TELL40 boards into multi-event packets (MEP) and sent to computers for processing.

The UT TFC (timing and fast control) data flow is similar but in a reversed direction starting from SOL40 boards. The TFC datum is an 8-bit command, one command per bunch crossing. The ECS (experiment control system) data transmission is bi-directional and at relatively low speed. The SALT and GBTx configuration data are sent out to the front end, and monitoring data are read back.

Most prototype components of the readout system have been produced, and are being tested separately. This Fall, a “slice” of the complete readout system will be constructed. All components will work together as a whole to validate the readout architecture. The slice system will also provide an avenue for realistic quality studies.

Some components of the readout chain will operate in a higher radiation environment, and need to be radiation tolerant. In particular the inner-most SALT ASICs receive $\sim 15\text{MRad}$ for 50fb^{-1} running. The dynamic logic of the SAR ADC is considered to be more susceptible to SEU (single event upset) than a static logic [19]. Hence a prototype SALT chip that includes only the SALT ADC block was tested at MGH to validate the SAR ADC design [20].

The kinetic energies of the proton beam are 226MeV and 60MeV in different runs. The lateral size of the beam is wide enough to have stable uniform particle flux on the SALT chip. The beam intensity was varied over a large range. The low intensity mimics the radiation level in the LHCb nominal running condition. The intensity was gradually increased to a factor of 1000 stronger so as to boost up the SEU statistics.

During the test, a 40kHz sine waveform signal was injected into the ADC and digitized at 40 Msps. If there is no SEU, the readout ADC values would fit well to a sine function. Any sample that deviates from the fit indicates a SEU, as shown in Fig. 7. In total about 2×10^8 ADC samples were recorded, and only a few SEU events were observed. It is projected that at $\mathcal{L} = 2 \times 10^{33}\text{cm}^{-2}\text{s}^{-1}$, there will be as low as $\sim 6.8 \times 10^{-6}$ SEU channels per bunch crossing from all ~ 0.5 million channels in the UT system.

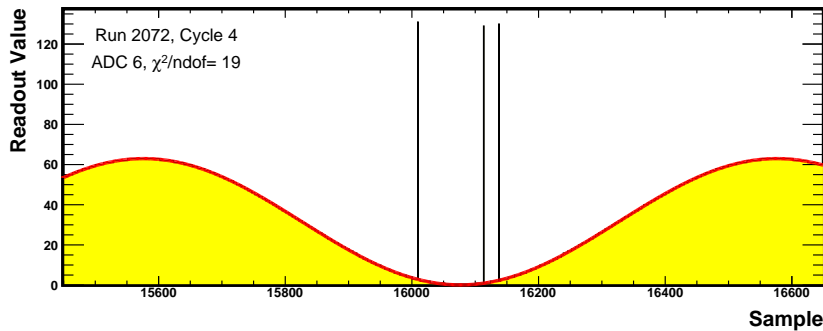


Figure 7: ADC output values fit to a sine function in red line. Three samples deviate from the fit function, and are considered to be SEUs.

The SALT chip with which we measured the ADC SEU rate was produced by IBM. Prototype SALT ASICs of 8 input channels and full DSP have been produced by TSMC. They are currently being tested. Since the TSMC technology is different from IBM, the ADC SEU rate may be different, and so it is planned to remeasure the SEU rate in the ADC and the DSP for this technology.

6. The UT mechanics and cooling

The main mechanical elements of the UT detector are staves. A staff is comprised of a bare staff, four flex cables, and 14 or 16 modules as illustrated in the right drawing of Fig. 8. The modules will be mounted to the bare staff with precision. Staves will be mounted to the UT outer support frame.

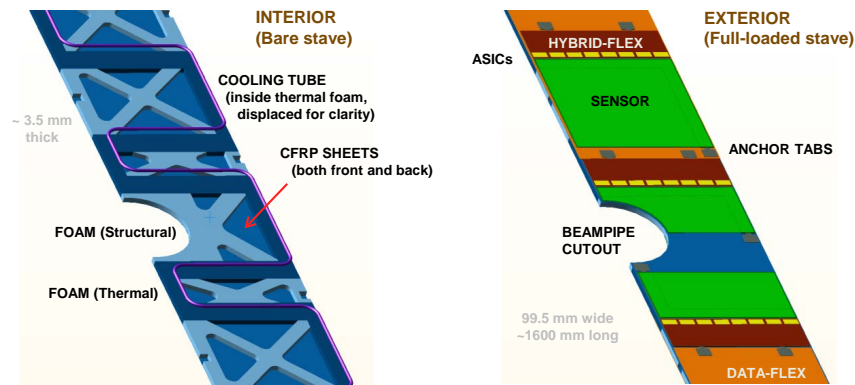


Figure 8: Structure of a central stave zoomed in the middle. (left) A bare stave with the top facing removed and the cooling tube displaced for clarity. (right) Fully populated stave with modules and data flex cables attached to a bare stave.

A bare stave is a stiff sandwich structure of two low mass CFRP (carbon fiber reinforce polymer) face sheets attached to a foam core, as shown in the left drawing of Fig. 8. Two different types of foam are used in the core: lower mass structural foam and thermally conductive foam. Embedded in the thermal foam is a snake-shape cooling tube, which runs under all ASICs for maximum cooling. All elements are attached with epoxy.

For the sensor module, there are different options. The basic requirements are to provide connection between ASICs and the flex cable, protect wire bonds during testing and handling, maximize heat transfer from ASICs to the bare stave, minimize transfer to the sensor, and isolate sensor bias from the stave facings.

Fig. 9 shows the baseline design of a module. A silicon sensor and a hybrid flex are glued to a ceramic stiffener with a mixture of thermally conducting Hysol epoxy and BN powder. The ceramic stiffener is made of $500\ \mu\text{m}$ thick pyrolytic BN. It is machined in “L” shape so that it attaches to the sensor only on two edges of 10mm width, to ensure that the sensor is not over-constrained. The hybrid flex contains an electronic circuitry to connect SALT ASICs and the flex cable, and houses electronic components that are necessary at the front end. The SALT ASICs are attached to the hybrid flex with thermal conductive epoxy. The sensor strips are directly wire-bonded to the input pads of the ASICs or via external pitch adapters if the adapting scheme is chosen.

A variation of the design is to use a $250\ \mu\text{m}$ thick AlN stiffener and have hybrid circuitry printed on top of it using thick-film technology. In this option the hybrid flex and the epoxy that attaches the flex to the stiffener are no longer needed. This simplifies the construction. However, the mechanical properties and the radiation length need to be further studied. Prototype circuitry of different options will be available soon to test with prototype SALT ASICs attached.

In construction, the flex data cables are glued to a bare stave first. Sensor modules are then attached to the bare stave and the flex cables with a reworkable epoxy of phase-change thermal interface material. In this way, should one module test bad after the full stave is constructed, the malfunctioning module can be replaced. The sensor modules will be wirebonded to the flex cables. The bonding pads on the flex cables are large enough that multiple wirebondings are possible.

When modules are attached to the bare stave the SALT ASICs are on top of the cooling tube so

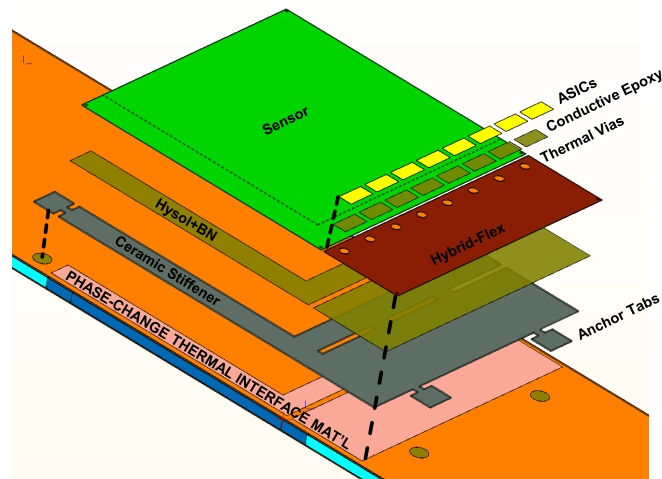


Figure 9: Structure of a sensor module with components offset for clarity.

that the heat generated by the ASICs can be taken away most efficiently. The cooling tube is made of Ti CP2 alloy, 2.275 mm OD and 135 μm wall thickness. The UT will use bi-phase evaporative CO_2 cooling, the technique developed by NIKHEF for the current VELO detector [21]. The sensors are cooled to below -5°C . The maximum temperature gradient difference on a sensor is less than 5°C . ANSYS simulation studies and thermal measurements with a prototype stave show that the requirement can be achieved with the current design.

Key components of the bare stave structure have been carefully tested in different conditions. In particular, samples of the reworkable epoxy, the structural foam, and titanium tube fittings were irradiated to the maximum dose of 50 fb^{-1} running. Ultimate shear strength of the epoxy, ultimate tensile and shear strengths of the structural foam were measured before and after the irradiation, at room temperature and low temperature. There is no change in the performance. The strengths meet the UT requirements. The titanium tube fitting was pressure-tested up to 150 bar, and no obvious leak or any other problem was observed.

7. Summary

The UT detector will replace the current TT detector, to cope with higher data rate and faster readout speed in the LHCb upgrade. It is critical in the full software trigger, reducing the long track ghost rates, and increasing the reconstruction efficiency of long live particles.

We have very active R&D program that covers Si sensor, SALT ASIC, low mass flex data cable, readout electronics, mechanics and cooling. Design of the system has achieved considerable progress. Construction and production of time consuming components such as the bare staves will start by the end of 2015. R&D on other components will continue. The goal is to have UT ready for installation in 2019.

The UT R&D work receives helps from many people out of the LHCb UT group. To them we owe a debt of gratitude. The author want to especially thank Ethan Cascio and the crew at the MGH for providing flexible and stable beam in the SALT ADC radiation test, the CERN accelerator

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