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BELLE II Pixel Detector

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The DEPFET technology is the baseline for the innermost detector of the Belle II experiment at the e^+e^- SuperKEKB collider at KEK. This technology integrates signal detection and a first phase of signal amplification in a single silicon structure with a 75 μm thin pixel array. This feature provides a very accurate position measurement, with an overall material budget of 0.2% radiation length and reduces the impact of multiple scattering for tracks with low transversal momentum. Furthermore, the physics goals of the experiment impose challenging requirements to this technology, but DEPFET with its excellent signal-noise-ratio, its lower power consumption and its non destructive readout has proven to be a suitable solution for the Belle II PXD necessities. The vertex pixel detector will consist of two DEPFET layers at radii of 14 mm and 22 mm with 8 and 12 modules respectively. The pixel sizes will vary, between 50x50 $\rightarrow$ 55 μm^2 at the fist layer and between 50x70 $\rightarrow$ 85 μm^2 at the second layer, to optimize the charge sharing efficiency. Moreover the four-fold readout in rolling shutter mode provides a readout speed of 20 μs/frame. All of these features, the sensor concept and the electronics involved will be presented in detail.

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1. The Belle II PXD.

The upgrade of Belle detector, Belle II detector, is being constructed at KEK in Tsukuba (Japan) as part of the KEKB collider upgrade (SuperKEKB). This machine is an asymmetric e^-e^+ collider, working at Ψ(nS) resonance energies. The expected instantaneous luminosity will be 40 times larger (up to 8x10^{35} cm^2s^{-1}) than its predecessor, aiming an integrated luminosity of 50 ab^{-1}. The new accelerator will collide smaller beam sizes, reducing the horizontal and vertical diameter of the beam to the range of nanometers (*Nano Beam Concept*) and the beam current will increase by a factor of two. This new scenario must cope with higher event rates and background (10 - 20 higher), and accordingly larger radiation damage, occupancy and fake hit production [2].

To deal with the increase of the beam background, the asymmetry at SuperKEKB will be smaller, using electrons with 7 GeV and positrons with 4 GeV, compared with its predecessor, which nominally used electrons with 8 GeV and 3.5 GeV for positrons. This will reduce the average separation between the B and $\bar{B}$ decay vertices by a factor of two, down to 100 μm. To cope with this new scenario, improved vertexing and tracking capabilities are needed for the Belle II detector [3].

	Belle II
Occupancy	0.4 hits/μm^2/s (< 3%)
Radiation	$\sim$20 $kGy/year$
Frame time	20 μs (cont r.o. mode)
Acceptance	17^o-155^o
Material budget	0.21% X_0 per layer
Resolution	15 μm

Table 1: Belle II PXD requirements [4][3].

The new vertex detector concept will consist on four layers of double-sided silicon strip (SVD) and two layers of highly granular DEPFET pixel detector (PXD). The PXD layers will be located at a radius of 14 mm and 22 mm from the interaction point (IP). As a consequence of the low momentum of the particles in the final state, the hit position reconstruction is limited due to the multiple Coulomb scattering, requiring an ultra-thin technology (75 μm in the sensitive area and a 525 μm thick rim providing mechanical stability) to keep the material budget below $\sim$ 0.2% X_0 per layer. The spatial resolution needed is 15 μm. To achieve this resolution and improve the charge sharing between pixels, the pixel sizes will vary from 50x50 $\rightarrow$ 55 μm^2 (Layer 1) and 50x70 $\rightarrow$ 85 μm^2 (Layer 2). The detector acceptance must cover the range of 17^o-155^o in azimuth angle [2]. The fast readout will be performed in continuous mode with a time per frame of 20 μs, keeping the occupancy below 3% [4]. Additionally, the detector technology has to be radiation hard to cope with the expected $\sim$20 $kGy/year$ (acording similations).

2. The DEPFET Module

2.1 The DEPFET Pixel

A DEPFET pixel consists on a field effect transistor (FET) placed on the top of a high resistivity n-type sideward fully depleted silicon bulk. A deep n-doping implantation, the "internal gate", located under the transistor channel (around 1 μm below) creates a minimum of potential for the electrons (Figure 1) [1]. The electrons generated by impinging particles will drift towards the surface of the device and will accumulate there. The internal gate is capacitive coupled to the transistor channel, it means that the charge located there, modulates the drain current through the pMOS transistor, which is used as a readout signal. The internal amplification g_q is defined as the drain current in pA per electron on the "internal gate". The expected value for the final sensor is of the order of $400 pA/e^-$ [6]. The readout process is non destructive. The charge located in the "internal gate" remains unaltered. In order to reset the detector and avoid the saturation of the "internal gate", an additional n^+ contact is placed in the periphery of each pixel (clear contact). By applying sufficiently high voltage, the clear contact becomes the most attractive potential for the stored electrons, forcing them to drift from the "internal gate" to the clear contact. The potential barrier between the clear contact and the "internal gate" is modulated with an additional polysilicon structure, called *cleargate* [1].

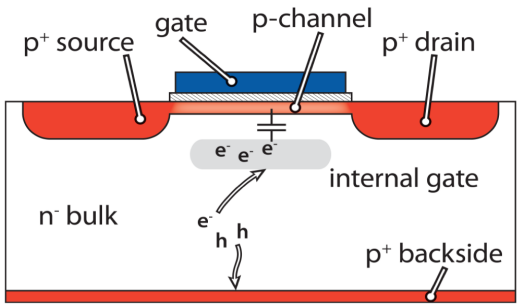

Figure 1: Section of DEPFET Pixel

2.2 Thinning Process

In the process of thin down the DEPFET sensor, since the backside is electrically active, conventional thinning techniques, like chemical-mechanical polishing or backside grinding, cannot be used. To thin the sensor down to 75 μm in the sensitive area, a special technology has been developed [7]. Two wafers are required, the sensor and the handling wafers. First the backside of the sensor wafer is processed, which is afterwards bonded onto a handling wafer. In the second step the sensor wafer is thinned from top, using conventional methods, down to the desired thickness. Then, all the processing

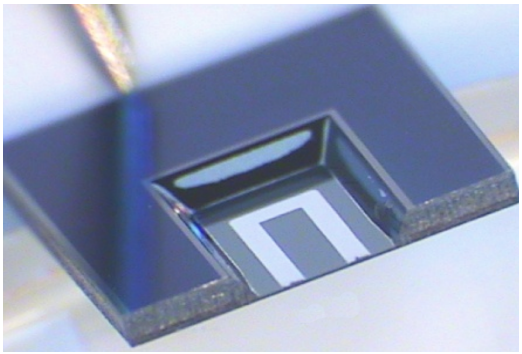

Figure 2: Thinned DEPFET sensor.

steps on the front side are carried out (implanting, polysilicon deposition, lithography, etc.). Finally, anisotropic etching is used in order to open a window below of the active area of the DEPFET. The handling wafer remains as a frame (525 μm) to provide mechanical support to the active area and the balcony to the steering chips (Figure 2). The different contributions to the material budget in the acceptance region are shown in the figure 3.

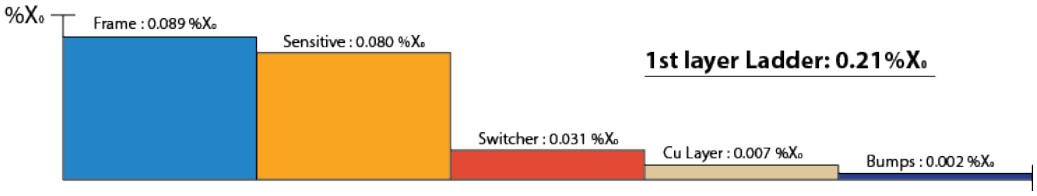

Figure 3: Material Budget Contribution [3]

2.3 DEPFET half ladder

Each half-ladder consists of an array of 250x768 pixels. The pixel size depends on the layer location and the expected tilt of the impinging particles. In the first layer, at the center of the ladder, where more perpendicular incidende is expected, to improve the charge sharing, the pixel size will be 50x50 μm^2. In the edges, where more tilted incidence is expected, the pixel size will be increased, up to 50x55 μm^2. The same strategy is applied to the second layer where the size of the pixels will vary from 50x70 $\rightarrow$ 85 μm^2 [3].

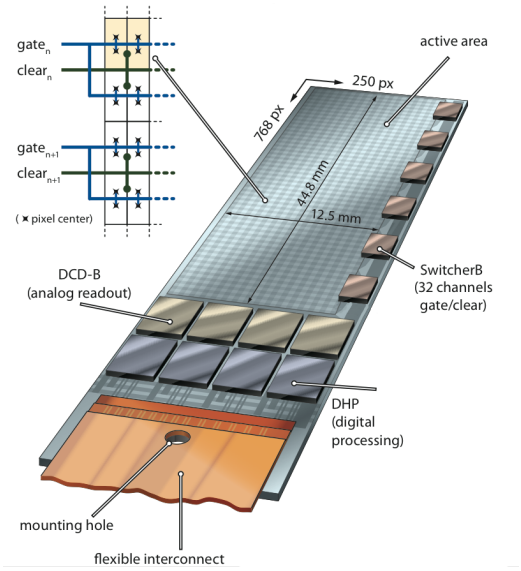

Figure 4: DEPFET half ladder

The control ASICs (Switcher) are bump-bonded at the lateral balcony, while the readout ASICs (DCD) and processors (DHP) are placed at the end of stave (Figure 4), out of the acceptance region. To achieve the required readout speed for Belle II (20 μm/frame), 4 physical rows are connected to one electrical row, these 192 electrical rows are controlled by six Switchers. Each of the switcher has 32 Gate and Clear outputs for switching the FETs on and off and to apply the Clear pulses [8] [9]. The drain current from the activated transistors go through the drain lines to the current digitizer (DCD-B). Each DCD-B contain 512 ADCs for 256 input channels. It runs at nominal speed of 320MHz and applies current subtraction and a compensation for pedestal current (2bit DAC). [10] The noise generated is in the order of 50 nA. The DCD-B

produces $\sim$ 82 Gbps/s of data and send it to the next ASIC (DHP). The Data Handling Processor (DHP) controls the switcher sequence and the DCDs. Also corrects the data by pedestal, and reduce it, applying a Zero Suppression Cut, to 5Gbps [11]. The data is transferred via a Kapton Flex, using LVDS, to the Data Handling Hybrid (DHE) consisting of a FPGA for further data processing [12].

2.4 The DEPFET PXD

A full ladder is constructed with two of these symmetric (with respect to the short edge) half ladders, which are glued together using small ceramic joints (ZnO_2). The PXD consists of 20 ladders which are arranged cylindrically around the beam pipe in two layers. The inner layer consists in 8 ladders located at 14 mm of radii and the outer layer consists 12 ladders located at 22 mm of radii (Table 2).

	Layer 1	Layer 2
Module	8	12
Radii	14 mm	22 mm
Ladder Size	15x136 mm^2	15x170 mm^2
Pixel Size	50x55 μm^2 50x60 μm^2	50x70 μm^2 50x85 μm^2
Pixels	250x1536	250x1536
Thickness	75 μm	75 μm

Table 2: The Belle II PXD.

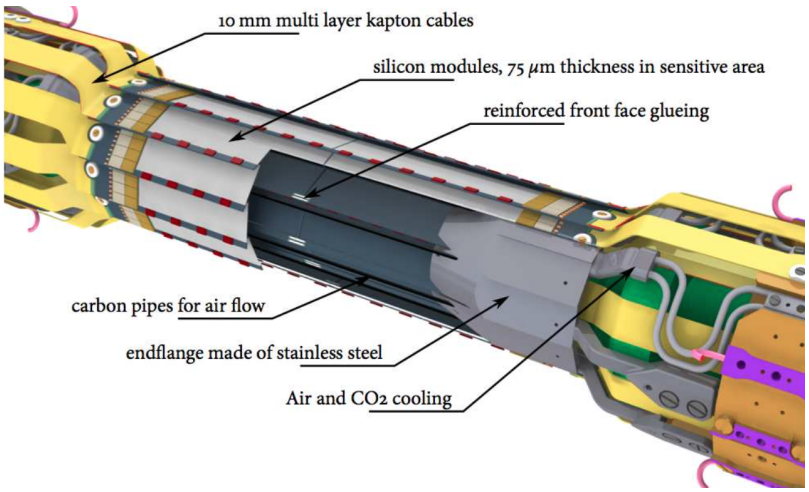

Figure 5: Schematic view of the PXD mounted.

The ladders are mounted on stainless steel blocks which also serve to dissipate the heat produced by the readout electronics. These blocks have integrated cooling channels to flow cold nitrogen to the sensors and capillaries for a CO_2 cooling system. (Figure 6).

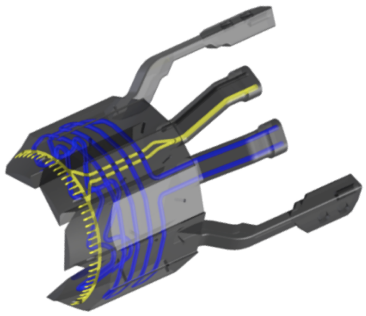

Figure 6: DEPFET half ladder

The total power consumption of one DEPFET module for Belle II is around 9W (0.5W the Switchers, 6W the DCDs, 2W the DHPs and 0.5W distributed homogeneously in the active area), adding 360W for the whole PXD detector. Finite element simulation (FEA) and laboratory measurement have proven that, the 2-phase CO_2 at -30^{o}C circulating through the stainless steel block is enough to remove the heat produced by the readout electronics. The centre of the ladders has to rely on forced convection with nitrogen flowed from the steel blocks and also using carbon fibers near to the switchers (Figure 5) [13].

3. DEPFET Performance

3.1 Test under beam

DEPFET technology has been extensively tested in several campaigns of beam test during last years. The usual locations were CERN with pions of 120 GeV and DESY with electrons between 1-6 GeV. The main goal of these campaigns is to check all the sensor aspects: charge collection, operation points, efficiency, angular scans, gate length, clear structure, etc. Also, all the system related issues: power supply and DAQ system prototypes. The following results come from the data took with a PXD6 Belle II design prototype with a pixel size of 50x75 μm^2 and 50 μm thick. The sensor matrix has 32x64 pixels and was operated with one Switcher and one DCD. For this prototype the efficiency of detection was over 99.5%. Figure 7 shows the charge collection distribution. The charge collected by the full clusters featured a most probable value over 23 ADU, and considering the intrinsic noise, which is 0.6

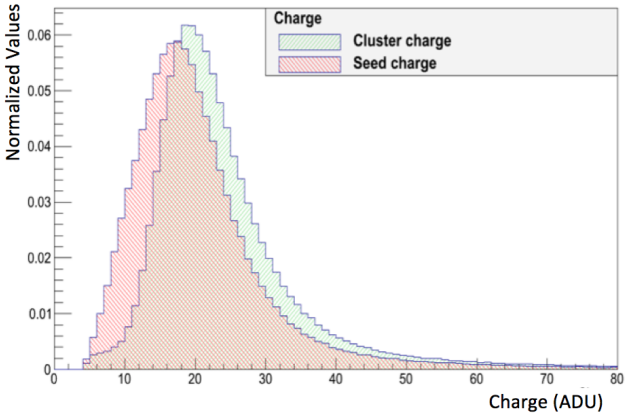

Figure 7: Charge Collection Distribution

ADU, the signal-to-noise ratio is around 40.

The sensor resolution is an important parameter that has been studied and optimized, figure 8 shows the resolution (defined as the RMS90) as a function of the zero suppression cut applied. The resolution obtained is 8.5 μm.

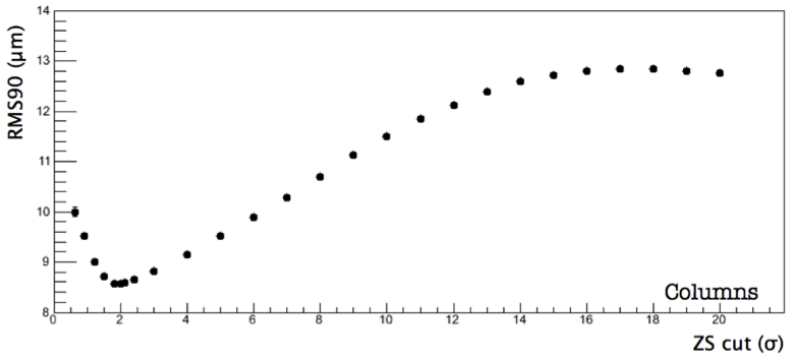

Figure 8: Sensor Resolution as a funciton of the zero suppression cut.

3.2 Gated Mode

The SuperKEKB injection scheme foresees an asymmetric electron and positron injection of 25Hz resulting in a total injection frequency of 50 Hz. The process of cooling down the new injected bunches by synchrotron radiation will take approximately 4 ms. During this "bunch stabilization" period, part of the particles hit the collimator. The secondary particles created, called as "noisy particle", will cause background occupancy. Consequently, one cannot distinguish whether the signal originates from a real event or from a noisy particle. This would generate a 20% deadtime, which is not acceptable for a proper operation of the Belle II vertex detector. Hence, further detector investigations are carried out in order to make the detector insensitive for short time periods when noisy bunches are passing. This takes approximately a few hundreds of nanoseconds. During this time, the idea is to make the detector blind. Therefore, the device is switched into the so called "gated mode operation". This is done by applying the Clear pulse and the appropriate Gate voltage (FETs are in the off-state) simultaneously, the potential distribution within the silicon bulk is changed such that newly created electrons within the bulk drift directly to the Clear contact. Meanwhile the amount of stored charge in the internal gate remains untouched, conserving the signal from real Belle II events.

To prove the feasibility of this operation mode, two experiments were performed using a laser to simulate the charge generation in the matrix. In both experiments 8 frames were took consecutively, changing the control sequence to clear the frame when is needed. The first experiment, so called "Junk charge generation", were meant to prove the blindness of the sensor. For this, the laser was pointed in the first frame, to check the matrix response. The clear process is applied after the third frame. The three next frames are operated in gated mode, during this process the laser is

pointed again. If the sensor is really blind, no signal is expected when normal mode operation is recovered (See figure 9). The second experiment, so called "Signal Charge Restore", is meant to check if the charge is conserved inside the internal gate during the gated mode. The experiment consisted in pointing the laser before gated mode operation and see the remaining charge after it. If charge is conserved a laser spot is expected after gated mode (See figure 10).

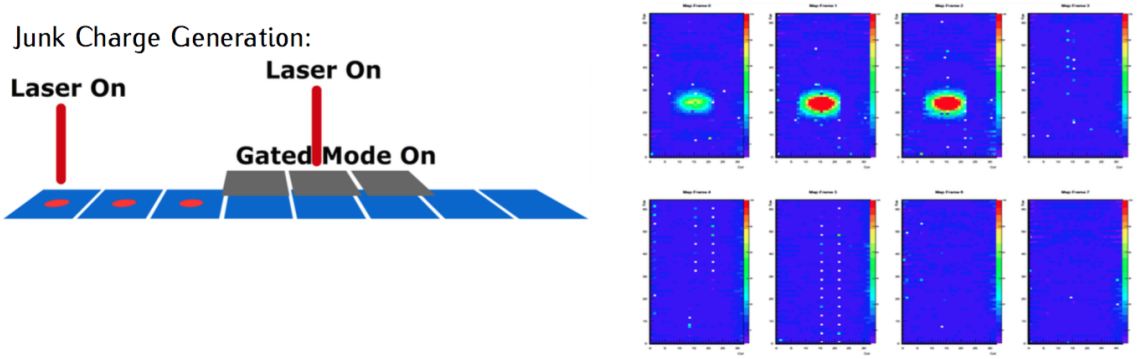

Figure 9: Junk charge generation. Experiment sketch (left), result example (right)

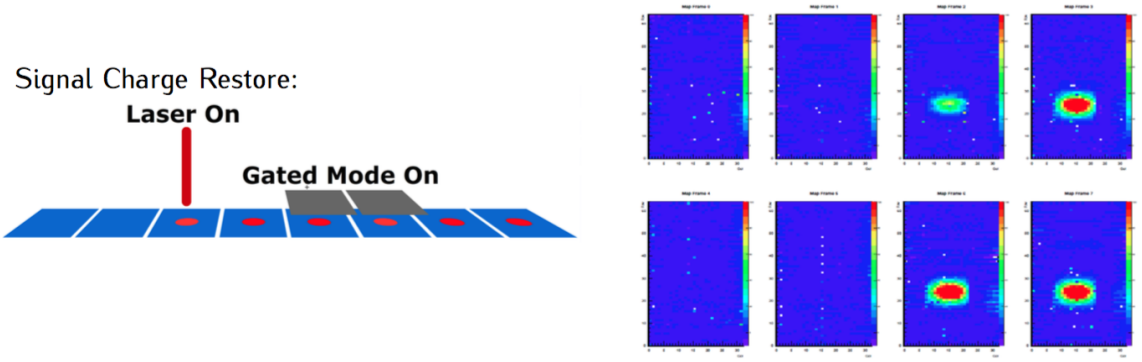

Figure 10: Signal restore process. Experiment sketch (left), result example (right)

4. Conclusions

The DEPFET collaboration is developing ultra thin pixel sensors with integrated amplification. The measurements in the laboratory and tests under beam have proved the capability to fulfill all the given challenging requirements in terms of signal-to-noise ratio, material budget, spatial resolution, and readout speed. Also the flexibility of the DEPFET technology to generate a new operational mode (Gated Mode) to avoid the dead time produced during the injection process of SuperKEKB. The pilot run is expected to be ready during summer 2015 , starting the final sprint, which will be finished in spring 2017, when Belle II PXD will become a reality.

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