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The Phase 1 upgrade of the CMS pixel detector

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The present CMS pixel detector will be replaced with an upgraded pixel system in the LHC winter shutdown 2016/2017. The design of the upgraded CMS pixel detector allows to cope with the higher peak luminosities expected in the coming years, and in particular after the next LHC shutdown. The new upgraded detector will have higher tracking efficiency and lower mass with four barrel layers and three forward/backward disks to provide a hit coverage up to absolute pseudorapidities of 2.5. In this paper the new pixel detector will be described focusing mostly on the barrel detector design, construction and expected performances.

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1. Introduction

The CMS pixel detector has shown an excellent performance during the first period of data taking at the LHC (2010 to 2012) and played a key role in many physics analyses [1, 2]. The present pixel detector was originally designed for a luminosity of $1 \times 10^{34}\,\mathrm{cm}^{-2}\mathrm{s}^{-1}$ and a pileup (number of inelastic interactions per bunch crossing) of 25 in LHC collisions with 25 ns bunch spacing. These beam parameters will be reached in the middle of the LHC data taking period 2015-2017 (with an additional increase in the center of mass energy up to the value of 13–14 TeV). The peak luminosity will keep increasing until 2018 when it will reach the value of $1.5 \times 10^{34}\,\mathrm{cm}^{-2}\mathrm{s}^{-1}$. In order to maintain efficient and robust tracking at CMS, the pixel detector will be replaced with an upgraded pixel system, referred to as *Phase 1 upgrade*, in the LHC winter shutdown 2016/2017. The design of the upgraded CMS pixel detector allows to cope with the yet higher peak luminosities after the next LHC shutdown reaching $2 \times 10^{34}\,\mathrm{cm}^{-2}\mathrm{s}^{-1}$ around 2021 and pileup of 50 or 100 at 25 ns or 50 ns bunch spacing, respectively. The new upgraded detector comprises four barrel layers and three forward/backward disks to provide a hit coverage up to absolute pseudorapidities[1] of 2.5. Since the innermost sensitive layer is closer to the interaction point compared to the current detector, faster front-end electronics needs to be developed to operate with high hit efficiency and low dead-time. In addition, improvements in the mechanical design of the detector allow to reduce the amount of material over the entire pseudorapidity region covered by the pixel detector despite the addition of one barrel layer.

The following section gives an overview on the design of the CMS Phase 1 upgrade system. The design and testing of the detector modules is discussed in Section 3. Section 4 and 5 review the readout electronics and data acquisition system as well as the power system, cooling and mechanics. Furthermore, results from testing of prototype components and the status of the production of the final system are discussed. Plans for testing and commissioning of the complete system are outlined before concluding the paper.

2. Design of the CMS Phase 1 Upgrade System

The CMS Phase 1 upgrade pixel system [3] consists of four cylindrical barrel layers at radii of 30 mm, 68 mm, 109 mm, and 160 mm and three disks on each side of the interaction region at a distance of 291 mm, 396 mm, and 516 mm. The layout of the upgrade pixel system is compared to the current pixel system in Figure 1. The detector layout is optimized to have a 4-hit coverage over the whole pseudorapidity range ($|\eta| < 2.5$) with minimal innermost layer radius improving pattern recognition and track reconstruction. In 2014, during the first LHC shutdown period, a new beampipe with a smaller diameter of 45 mm was installed at CMS. This allows for a placement of the innermost layer closer to the interaction point.

The barrel pixel detector (BPIX) is built from 1184 segmented silicon sensor modules, while 672 modules are used for the endcap disks (FPIX). This amounts to a total of 124 million readout channels. The design of the detector modules is discussed in more detail in the next section.

[1] CMS uses a right-handed coordinate system. The x-axis points to the center of the LHC ring, the y-axis points up vertically and the z-axis points along the beam direction. The azimuthal angle ϕ is measured in the xy-plane and the radial coordinate is denoted by r. The polar angle θ is defined in the rz-plane and the pseudorapidity is $\eta = -\ln\tan(\frac{\theta}{2})$.

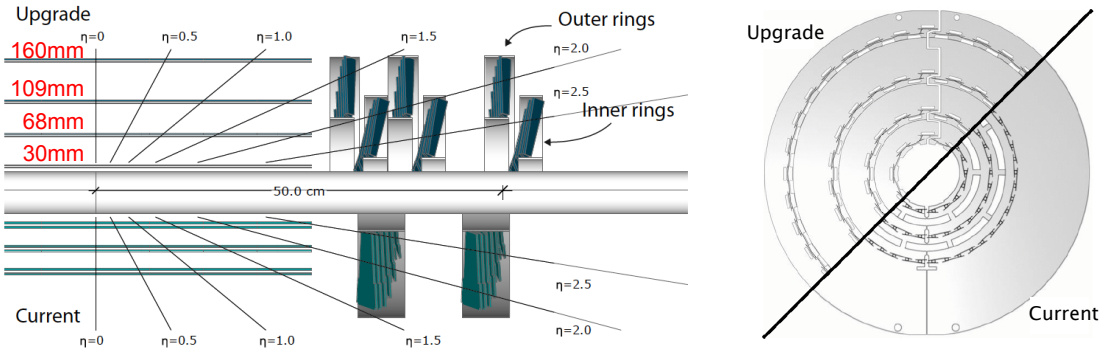

Figure 1: Layout of the Phase 1 upgrade of the CMS pixel detector compared to the current detector layout in longitudinal (left) and transverse (right) view.

The detector modules are mounted on lightweight mechanical structures built from a carbon fiber foam compound. The BPIX and FPIX detectors are each connected to four service half-cylinders that hold the readout and control circuits as well as the power lines and cooling tubes of the detector. In order to reduce material the use of a two-phase CO_2 cooling system is adopted. Furthermore, the module connectors and electronic boards on the service cylinders are shifted to higher pseudorapidities, outside the sensitive tracking volume.

The upgrade system has to fit in the same mechanical envelope as the current system and reuse existing services, power cables and optical fibers. This puts strong constraints on the design of the new system. In particular, higher bandwidth electronics is need. Since the upgrade detector has 1.9 times more channels than the current detector, the power consumption increases accordingly. The upgrade system uses DC-DC power converters to supply the necessary current to the modules while reusing the existing infrastructure. Later sections give more information about the readout and power system of the upgrade CMS pixel detector.

3. Pixel Detector Modules

The upgrade pixel detector uses a similar module design as the current one. A pixel detector module is built from a n^+-in-n planar silicon sensor with a dimension of $66.6 \times 18.6\,mm^2$ and a thickness of $285\,\mu m$ bump-bonded to an array of 16 readout chips (ROCs). Each ROC is segmented into 4160 readout channels and reads out the pulse height information for each pixel. The pixel size is $100 \times 150\,\mu m^2$ in order to achieve similar resolution in both the $r\phi$ and z direction. On the other side of the silicon sensor a high density interconnect (HDI) flex printed circuit is glued and wire-bonded to the ROCs. A token bit manager chip (TBM) controls the readout of the ROCs and is mounted on top of the HDI. In order to facilitate module production and maintenance, the same rectangular module geometry is used for barrel and endcap detectors. Drawings of the upgrade module layout are shown in Figure 2.

The innermost layer of modules being placed closer to the interaction point together with the increase in instantaneous luminosity leads to a significantly higher flux of particles in the detector. The ROC used in the current pixel detector has not been designed to operate at rates higher than

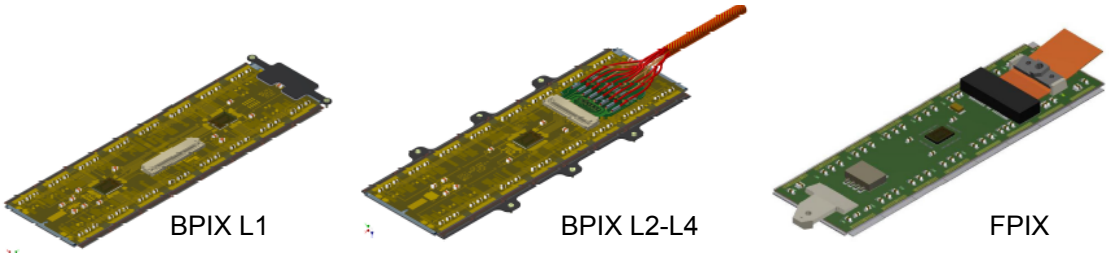

Figure 2: Layout of the pixel module for BPIX layer 1 (left), BPIX layer 2-4 (middle) and FPIX (right).

few tens of MHz/cm^2. Therefore a new ROC has been designed in order to minimize data losses due to latencies and limited buffering in high luminosity running.

The upgrade ROC [4] is manufactured in the same 250 nm CMOS technology as the present ROC. It maintains the well tested and reliable core of the present ROC and its readout architecture based on the column-drain mechanism. The design of the pixel matrix remains essentially unchanged. Modifications are only made in the chip periphery to overcome the limitations at high rate. The main changes for the upgrade chip include the adjustment of the size of the buffers to store the hit information during the trigger latency, the implementation of an additional readout buffer stage to reduce dead time during the column readout and the adoption of 400 Mbit/sec digital module readout. The latter is needed to accommodate the higher module count in the 4-layer system while reusing existing services. It comprises the addition of an 8-bit ADC, a PLL to provide the high clock frequencies and new fast digital readout links. The readout speed of the ROC itself is unchanged, but the transition from 40 MHz analog coded data to 160 MHz digital data allows faster readout of the modules. The TBM multiplexes groups of ROCs onto 320 MHz links (400 MHz after 4bit/5bit encoding), doubling the capacity per optical fiber. The modules for FPIX and BPIX layer 3 and 4 each use one link, while 2 or 4 links are used for BPIX layer 2 and layer 1 modules, respectively.

Further improvements in the design allow for lower threshold operation (below 2000 e$^-$ with noise less than 100 e$^-$) and higher radiation tolerance. A dose of about 120 MRad is expected to be accumulated for the innermost pixel layer of the upgrade system during its operation (assuming an integrated luminosity of 500 fb^{-1}). The radiation tolerance of the upgrade ROC has been tested after irradiation up to 150 MRad using a 23 MeV proton beam at the ZAG Cyclotron in Karlsruhe. The upgrade ROC shows an excellent performance and threshold and noise characteristics remain basically unchanged after irradiation.

Data-losses have been measured for pixel hit rates up to 250 MHz/cm^2 using high-rate x-ray tubes and were found to be in excellent agreement with expectations based on detailed architecture simulations. Based on the same simulation for proton-proton collision data, the data losses in FPIX and BPIX layer 2 to 4 will be less than 2%. For the innermost layer where hit rates up to 580 MHz/cm^2 are expected, a modified version of the readout chip is currently under development. The design requirements are faster hit transfer from pixels to the periphery as well as dead-time free buffer management. The submission of the chip for the first barrel layer is planned for fall this year.

A total of 240 ROC wafers is needed for the production of modules for BPIX layer 2 to 4 and FPIX. The wafer production is finished and the wafers are currently under test at PSI and FNAL. Based on the first batches of the pre-series production a yield of about 90% could be established. Module production and testing happens in different production centers in Switzerland, Germany, Italy, Finland, Taiwan and the US. The components for module production (sensors, ROC, TBM, HDI) have been mostly delivered and distributed to the production centers. A good number of pre-series modules have been produced in all centers during the last year, while the module production for the final system is currently ramping up. The aim is to finish production of the modules for BPIX layer 2 to 4 and FPIX by early 2016. The module production for BPIX layer 1 is foreseen for summer 2016.

Module testing is done in two steps. First, a so-called bare-module test is performed to check the sensor and ROC assemblies right after the bump-bonding. At this step, the power consumption of the module is verified, the sensor leakage current is measured and the basic digital functionality of the ROC is verified. Only modules passing the bare-module tests are used further to build complete module assemblies. The second step in testing is performed after full module assembly. At this stage, the module's functionality and performance are tested in detail and modules are classified according to predefined quality criteria. The testing includes the measurement of sensor leakage currents, module power consumption, ROC, TBM and pixel functionality, performance after thermal cycling, high-rate x-ray tests and energy calibration. The testing procedure takes about 7 hours. More details about the module testing can be found in [5].

4. Power, Readout Electronics and Data Acquisition

The power, readout and control circuits as well as the cooling lines are housed by eight service cylinder half shells, four serving the BPIX and four serving the FPIX detector. The mechanical structure of the service cylinders is made from layers of carbon fiber composites. Each cylinder is divided in sectors which hold the electronics for one readout group of detector modules. A readout group contains up to 39 modules. Each sector includes digital opto-hybrids (DOHs) as well as auxiliary chips (PLL, DELAY25, Gatekeeper) for the transmission of control, clock and trigger signals. So-called pixel opto-hybrids (POHs) are used for the transmission of the module readout data [6]. The change from analog to digital module readout in the upgrade system also requires the adoption of new optical links. POHs are built from four or seven transmitter optical subassemblies (TOSA), linear laser-driver and level-translator chips and have been designed specifically for their use in the pixel upgrade system. All other components used in the control and readout chain are identical to the ones used in the current system. CCU chips are used for slow control, monitoring and timing distribution.

Furthermore, pairs of DC-DC converters [7] are mounted on the service cylinders. The DC-DC converters operate at an input voltage of 10 V with an output voltage of 2.4 V and 3.3 V for the analog and the digital voltage supply of the modules, respectively, with an efficiency of about 80%. The choice of the converter output voltage takes into account the voltage drop across the service cylinder and guarantees a minimum supply voltage of 1.6 V and 2.4 V for the analog and digital nodes of the modules, respectively. Each converter can provide up to 3 A of current and a total of

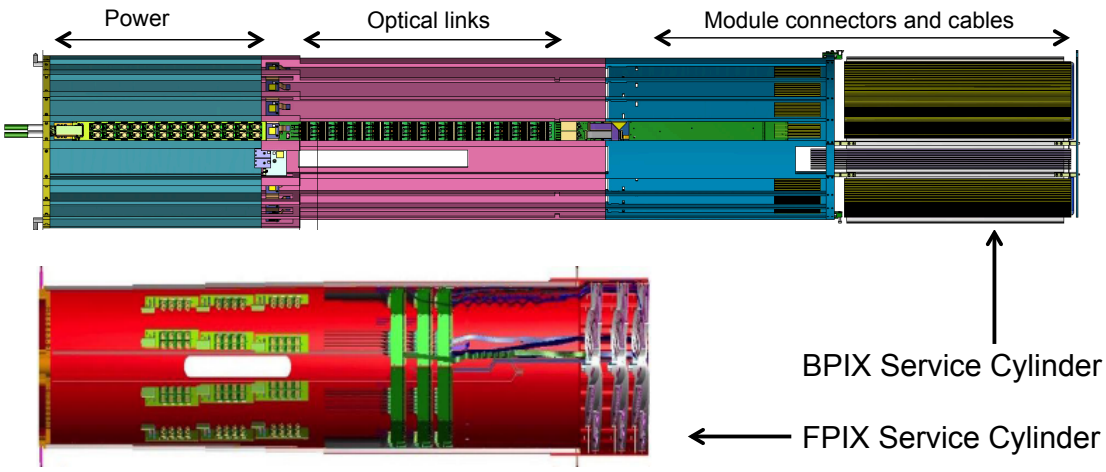

Figure 3: Schematic view of the BPIX and FPIX service cylinders. In these drawings only single sectors are equipped with power and readout electronics for better visualization.

1184 DC-DC converters is used for the full detector system. The service cylinders of the BPIX and the FPIX are shown schematically in Figure 3.

The off-detector VME-based data acquisition (DAQ) system used for the current detector will be replaced by a microTCA system with high-speed signal links providing data rates up to 10 Gbits/sec. The DAQ system to control and readout the full detector consists of 56 front-end driver (FED) modules which receive and decode the pixel hit information, two front-end controller (FEC) modules which serve the detector slow control, ten pixel front-end controllers (pxFEC) used for module programming, clock and trigger distribution and six AMC13 cards [8] providing the clock and trigger signals. The hardware development for the upgrade pixel DAQ system is well advanced and prototypes are available for demonstrator systems. The main focus is currently on the firmware development with the aim of providing full functionality for system tests by the end of this year.

5. Cooling System, Mechanics and Installation

The CMS pixel upgrade system uses 2-phase liquid-gas CO_2 cooling instead of single-phase C_6F_{14} liquid cooling as used for the present system. It differs from the current system in that the tubes are much narrower and operated at about six times higher pressure. Moreover, the cooling tubes are constructed in a complex looping structure in order to cool the components on the service cylinders as well as the detector modules. The cooling system will be operated at a temperature of $-20°C$ with the option of going to lower temperatures if needed. In the active region of the barrel part of the detector, stainless steel tubes with an inner diameter of 1.7 mm and a wall thickness of 50 μm are used. Two prototype half-barrel cooling mockups have been built and are currently being tested. First results from testing with CO_2 are very promising and the cooling system performs as expected from simulation.

For the BPIX the cooling loops form the backbone of the lightweight mechanical structure on which the modules will be mounted. The BPIX mechanics is built from a CFRP/Airex foam compound and is composed of six independent half cylinder shells. Each module is connect to an about 1 m long twisted-pair cable which carries both signal and data lines. The routing of the cables of the different barrel layers at the detector endflange is non-trivial. Therefore, a 3D printed mockup of the endflange has been made to exercise the cabling procedure with the real geometry.

The FPIX half disks consist of an inner and an outer blade assembly. The cooling loops are embedded in graphite rings and Thermal Pyrolytic Graphite (TPG) blades transport the heat from the module to the ring. Prototypes of the FPIX half disk mechanics have been produced and are currently used to develop a reliable procedure for mounting the modules on the blades.

Moreover, during the last LHC shutdown in 2014, a trial installation of the upgrade pixel system has been performed at CMS. Mockups of both the BPIX and FPIX detector systems have been used for this exercise. During the installation the detector system moves on wheels along a curved rail system until it reaches its final position in the center of CMS. The wheels are adjustable to insert the half shells away from the beam pipe and only close the detector system in the final position. The trial installation was concluded successfully.

6. Test Systems

In order to test the performance of the complete upgrade pixel system and gain experience in its operations, test stands have been set up at University of Zurich for the BPIX and at FNAL and CERN for the FPIX. The setups include a slice of the full CMS pixel DAQ together with prototypes of all components of the upgrade power system, control and readout chain as well as a number of detector modules. The main goal of the system test is to test all components of the detector system prior to full production, establish test and calibration procedures for the assembly and commissioning and eventually exercise the transition from the VME-based to the microTCA-based detector DAQ system. Pictures of the test stands at University of Zurich and FNAL are shown in Figure 4.

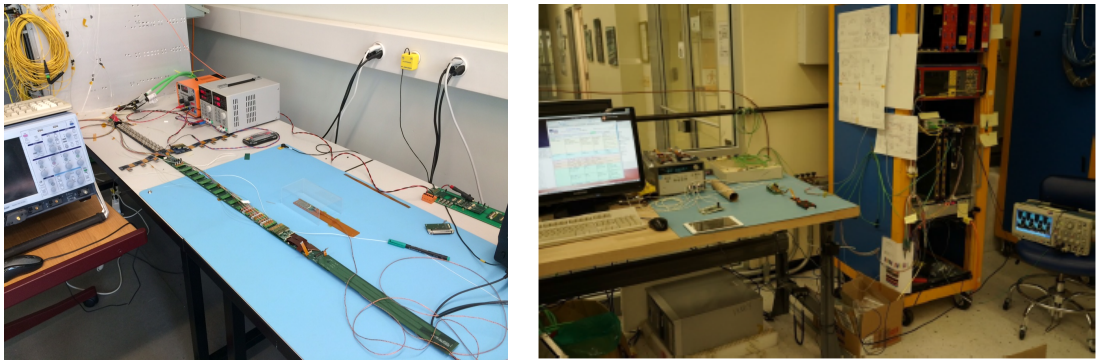

Figure 4: Pictures of the BPIX system test stand at University of Zurich (left) and of the FPIX system test stand at FNAL (right).

Furthermore, a pilot system consisting of 8 upgrade detector modules, the full readout chain and DC-DC powering for half of the modules has been installed in CMS in 2014 [9]. The installation of a pilot system allows to study the behavior of the upgrade system under real LHC conditions as well as to test the new components and their integration in the CMS detector readout system and the offline data reconstruction.

7. Conclusion

The current CMS pixel detector will be replaced by an upgrade pixel system during the extended LHC winter shutdown 2016/2017. The upgrade system features an additional barrel layer and endcap disks, reduced material budget as well as improved rate capability and lower threshold operation. The design, development and production of the module components is mostly completed, a good number of pre-series detector modules have been built and the project is now entering the production phase. Prototypes of all final components for the power and detector control and readout systems are available and are currently being tested in system tests. A pilot system consisting of 8 upgrade detector modules together with the full readout system has been installed in CMS during the last shutdown and is ready to take data.

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