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Pilot system for the Phase 1 pixel upgrade of CMS

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The CMS phase 1 pixel upgrade is planned for installation in 2016-2017, incorporating new front-end ASICs with digital 400 Mbps data links to handle a higher instantaneous luminosity of up to 2.5 x 10^{34} cm^{-2} s^{-1} and trigger rates of 100 kHz with bunch spacing scenarios of 25 or 50 ns. The new digital readout requires new back-end electronics incorporating faster optical receivers and firmware for decoding the new data format. Additionally the phase 1 upgrade is powered from DC-DC converters installed inside CMS close to the modules. To gain experience with this new readout chain and DC-DC converters under realistic operating conditions (trigger rates, backgrounds, high data occupancy, and possible single-event upsets) a pilot detector system comprising eight sensor modules, service electronics, optical links, and back-end electronics has been prepared using pre-production parts. The pilot system was installed with the present forward pixel detector in 2014 during long shutdown 1 (LS1). The pilot system will be operated concurrently with the present pixel detector in 2015-2016 to validate the data acquisition and powering design and advance online control system development for a rapid deployment of the full detector in 2017. This report summarizes the phase 1 pilot system experience leading into Run 2 of the LHC.

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1. Introduction

The current pixel detector consists of three barrel layers (BPIX) at radii of 4.4 cm, 7.3 cm and 10.2 cm, and two forward/backward disks (FPIX) at longitudinal positions of 34.5 cm and 46.5 cm and extending in radius from about 6 cm to 15 cm. The BPIX contains 48 million pixels covering a total area of 0.78 m^2 and the FPIX has 18 million channels covering an area of 0.28 m^2. These pixelated detectors produce 3-D measurements along the paths of the charged particles with single hit resolutions between 10 - 20 μm. The current pixel readout electronics was designed and optimized for the data rates and pixel occupancies expected up to the LHC design luminosity of 1 x 10^{34} cm^{-2} s^{-1} with 25 ns bunch spacing. The goal of the Phase 1 upgrade is to replace the present pixel detector with one that can maintain a high tracking performance at luminosities up to 2.5 x 10^{34} cm^{-2} s^{-1} as due to data losses in the read out chip (ROC), the present system will not sustain the extreme operating conditions expected in Phase 1.

For the CMS pixel phase 1 upgrade [1], some new concepts were introduced to the detector readout and powering such as digital readout at 400 Mbps, new Pixel Optohybrids (POHs), new front-end drivers (FEDs), which are back-end boards that decode the pixel data, and direct current to direct current (DC-DC) converters. This requires changes to the data acquisition system (DAQ), detector control and monitoring system (DCS), data quality monitoring (DQM), and offline reconstruction. The plan is to install and commission the phase 1 pixel detector with modified DAQ and DCS systems during an extended year-end technical stop at the end of 2016 and to have the new detector fully operational soon after. To be best prepared for a short commissioning period and to take advantage of the long shutdown during long shutdown 1 (LS1), a pilot system was built which consists of eight prototype modules incorporating the new readout chain, which is installed in the available space in the existing FPIX half cylinders, which host the auxiliary electronics, in 2014. A hybrid solution with new daughterboards on the existing FED is used at the beginning to readout the new fully digital pixel system, the new μTCA FED system will be used when available. The motivation of the pilot system was to learn in the actual collision environment of CMS how the readout, control, and offline systems perform with the LHC collisions of 2015. This will provide valuable experience for the operation of the new pixel detector as well as enabling an early start for the modifications that are required for the DAQ, DCS, and DQM.

The present FPIX was designed for possible installation of a third disk, thus sufficient infrastructure (optical fibers, power cables, and cooling) is available to accommodate the pilot system in these locations. The present pixel detector is using a monophase cooling with the coolant C_6F_{14} and the upgrade detector will use an evaporative cooling system based on CO_2 as coolant. Since the existing mechanical support as well as the cooling lines should not be modified to accommodate the pilot system, we are constrained to use the current C_6F_{14} cooling instead of CO_2 cooling for the pilot system. The pilot system is mounted on a spare FPIX half-disk support structure at the location of the third disk on two of the current FPIX half cylinders. The prototype modules are placed on brazed aluminum cooling channels connected to the existing FPIX cooling manifolds. Mounting eight prototype modules on the half disks gives only partial azimuthal coverage, but still allows for integration into the offline tracking software for efficiency and other studies.

The goals of the pilot system are:

- gain operational experience with the new ROC [2] and Token Bit Manager (TBM), a chip on

the pixel module that organizes the readout of the 16 ROCs, as well as digital transmission and readout with the new FED at CMS,

- get a head start on required DAQ modifications which include new FED firmware and software, as well as calibration procedures,
- study how the TBM and FED handle conditions present in CMS,
- study the performance of the new ROC in the high-rate environment of the LHC,
- test the DC-DC conversion powering,
- get a head start on required modifications to DCS.

2. Description of the Pilot System

The half-disk pilot system has four modules, each equipped with 16 readout chips, mounted on the brazed aluminum cooling channels, which are attached to the aluminum half-disk support structure. Figure 1 shows the pilot modules on the third disk along with the current FPIX first and second disk. The pilot modules are oriented perpendicular to the beam axis, covering from 6.1 cm to about 13 cm in the radial direction. The geometrical configuration is similar to the FPIX upgrade detector. The pilot modules are constructed exactly like the new FPIX modules, with a High Density Interconnect (HDI) glued to the back of the sensor module. The pre-production PSI46digV2.1 chip, which is designed for barrel layers 2-4 and the forward disks, is used. A new TBM, TBM08b, is attached to the HDI, which is the version HDIrev.C. From the HDI, a prototype 75 cm long Aluminum flexcable developed for the FPIX upgrade transmits the output signal from the TBM to an auxiliary electronic board, the prototype phase 1 FPIX Port Card, to which a POH board and supporting electronics are mounted. The output from two TBM cores is multiplexed and is then encoded in a 4-bit to 5-bit scheme for stability of the optical transmission. The 400 Mbps output of the TBM08b is transmitted by a single channel of the POH over a fiber to the downstream FEDs.

For powering of the pixel modules, since all power cables are already in place for the third disk, there is no need to use DC-DC conversion. However, since DC-DC conversion is an important element of the upgraded pixel detector it was decided to have modules of one half–disk powered by a prototype DC-DC converter [3] board using FEAST2 ASIC chips for the digital and analog power of the ROCs. This will allow evaluation of the impact of any electrical interference from the DC-DC converters inside of CMS, either within the pixel system or with other subdetectors. For maximum flexibility, two pilot system half disks were built, one powered by the conventional CAEN power supply modules (A4603), and the other one by DC-DC converters. The prototype DC-DC converter board is thermally connected to the existing cooling lines on the half-cylinder and controlled via a CCU board, which is mounted inside the half-cylinder for the pilot system.

2.1 Development

For the pilot system, prototype versions of the various new electronic circuits that will be used for the upgraded FPIX detector are used. These include the PSI46dig2.1 ROC, TBM08b, sensor

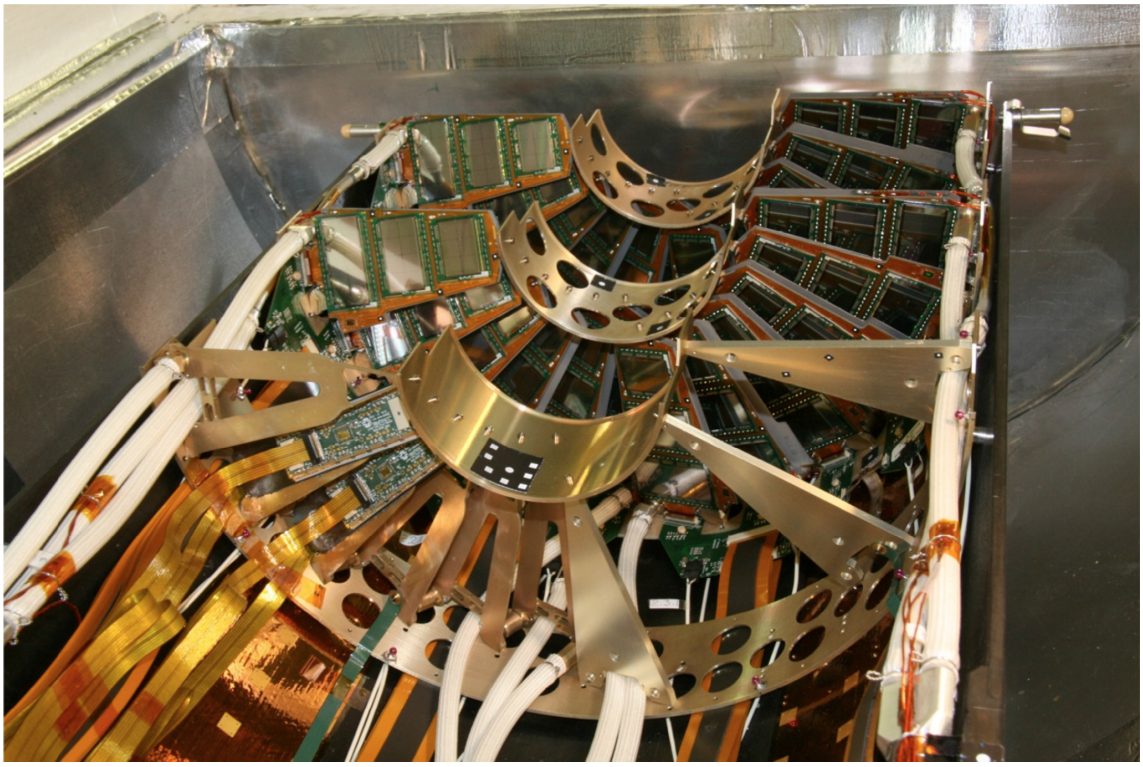

Figure 1: FPIX half-cylinder with the plaquettes (present wedge-shaped FPIX modules) for the current pixel system on the first two disks and the pilot modules on the third disk.

modules, Aluminum flex cable, Pixel Optohybrids, Port Card, DC-DC converter bus board, DC-DC converters with FEAST2 chips, and the modified FED. In addition the present pixel Front End Controller (FEC) and tracker FEC VME boards, which are back-end boards used to program the chips on the pixel module and the auxiliary electronic components, respectively, are reused for the pilot system. The spare Aluminum half-ring support structures and the brazed aluminum channels are used. No other mechanical support or cooling lines are required. Figure 2 shows a DC-DC converter, the drawing of a phase1 module and Figure 3 shows pilot system auxiliary electronics in the service-cylinder.

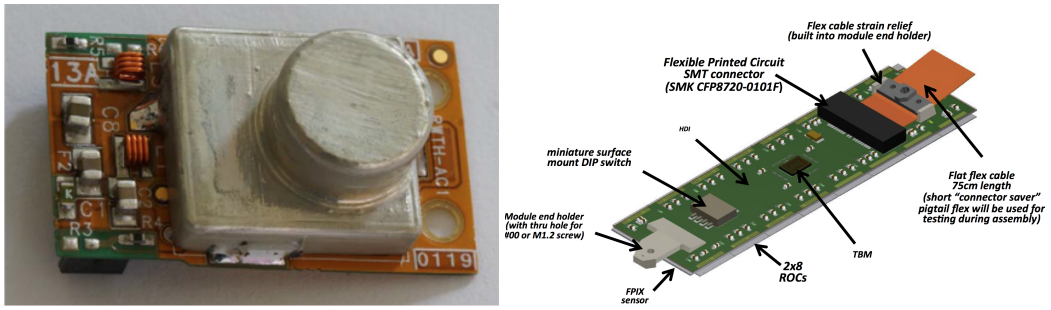

Figure 2: A DC-DC converter with the FEAST2 chip (left), and the CAD drawing of a FPIX phase1 module (right).

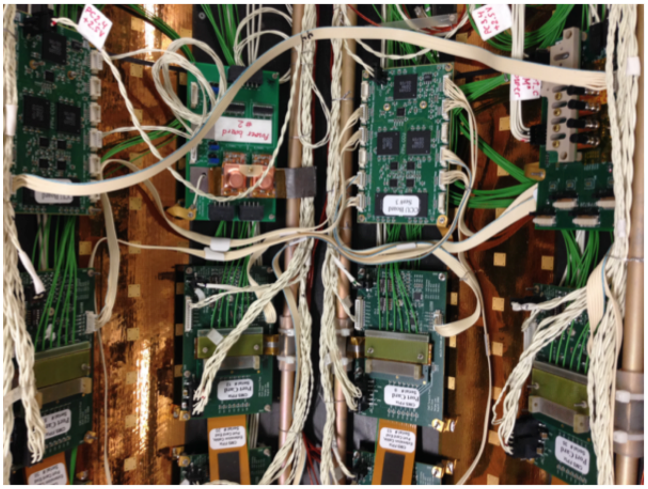

Figure 3: The photo shows the pilot auxiliary electronics (upper row) and current pixel detector port cards (lower row) in the service-cylinder. The upper row shows, from left to right, pilot CCU board, DC-DC board, current pixel CCU board and pilot port card.

For trunk power cables, power filtering boards, and power cables within the half cylinder, the spares left over from the construction of the FPIX detector are used. A modified CAEN power supply unit, which can provide 10V, is used for powering the modules with DC-DC converters.

All the required components were tested electrically and functionally. The ROC and TBM wafers were tested with a probe-card with known good dies marked. Likewise, the sensor wafers were tested with a probe-card, and only good sensors and ROCs were used for bump bonding. The prototype aluminum flex cable, Port Card, and POHs were fully tested before installation. The HDIs were tested with a probe-card, and the accepted ones then had the TBMs glued to them. Then the assembled HDIs were electrically and functionally tested.

The new μTCA pixel FED hardware and firmware that can receive and decode the new digital data format is under development. To ensure the capability to read out the pilot blades earlier than when the μTCA system is fully operational, prototype versions of daughterboards for the existing FED were used at the time of integration at CERN.

2.2 Assembly and Testing of the Pilot Pixel Modules

Bump-bonded pilot modules were delivered to two sites for assembly and testing, Purdue University and University of Nebraska at Lincoln. Both have acquired a new gantry system and used the modules to fully check out their assembly procedure. The assembly includes gluing the HDI to the pilot modules. The assembled pilot modules were then tested for functionality and shipped from the assembly sites to Fermilab for performance tests with a digital test board. The tested pixel modules were then shipped from Fermilab to CERN for installation in the FPIX half cylinder and further testing.

3. Installation, Commissioning and Monitoring

The pilot system half disks are integrated into the existing FPIX half cylinders and commissioned using a test stand running a standalone test software at CERN. Commissioning of the hardware and software begins with functional tests of the communication and readout using the test software. Parameters for the ROCs are initially taken from module test results. Prototype detector calibration procedures implemented in the online software are validated after the installation in CMS.

The pilot system was installed with the present FPIX half cylinders into CMS in December 2014. The installation into CMS at point 5 (P5) followed the identical procedure for the initial installation of the FPIX detector, performed in 2008 and repeated after repairs in 2009. No changes to the installation procedure were required to accommodate the pilot system, apart from connection of a few additional cables and fibers for readout and control.

3.1 Integration into the DAQ

The pilot system requires addition of new hardware to the pixel DAQ system at P5. The pilot system is initially controlled and readout from dedicated VME boards placed in a dedicated pilot system VME crate. Clocks, triggers, and control commands are initially distributed from the trigger and timing control (TTC)ci module in the pilot VME crate. In May 2015 the pilot system started to use its own partition in the trigger, control and distribution system (TCDS) system. The pilot VME crate has a pixel front-end controller (FEC) motherboard with two mezzanine front-end controllers (mFECs), each connected to one of the pilot system half-disks, which are serviced by separate optical fiber ribbons. Devices on the port card and the DC-DC converter card are programmed by a separate tracker FEC with two mFECs, each connected to the pilot CCU boards in each half cylinder. One modified FED card with two daughter boards is used to receive the optical links from the two pilot system half-disks. One S-link connection, a data-link which can be used to connect front-end to read-out at any stage in a dataflow environment, to the central CMS DAQ allows readout of the pilot system FED in the usual data stream. When available, prototype μTCA FED/FEC electronics will also be used with the pilot system. The pilot system uses its own PC to be decoupled from current pixel detector operations.

3.2 Modification Needed to Existing DAQ and Detector Control System

To accommodate the pilot system in the pixel data acquisition system at P5, some modest changes are required to the online software that are accommodated within the present software framework. Existing low-level interfaces are cloned and modified to program parameters of the new devices present in the phase 1 readout chain. This includes programming of new ROCs and TBMs, accessed through the pixel FEC, and new devices on the port card and DC-DC converter card, accessed through I^2C programming via the tracker FEC. The nature of these changes are minor (e.g. hardware addresses and functions) and are made with minimal development within the existing software framework.

The existing software framework also supports numerous local calibration runs that are used to optimize front-end electronics parameters. Many of these procedures are used directly or with

small modifications. Additional scans and optimization procedures appropriate to the new readout chain have been developed within the software framework in a straight-forward manner.

Likewise, the changes required to the Detector Control System (DCS) are relatively minor changes related to details of hardware changes or additional channels for control and monitoring. They are achieved within the existing framework.

3.3 Integration into Offline Reconstruction

The pilot system will be integrated into the CMS tracking software. The data will be present in the CMS software (CMSSW) framework when the prototype FED is included in the data taking.

4. Lessons Learned During Pilot System Operations

During the pilot blade system tests at CERN it was observed that the FED was having problems in decoding the data with high-rate triggers. The problem is traced back to two separate sources, an asymmetric eye diagram due to the TBM design and jitter on the phase1 port card. While an asymmetric eye diagram can be accepted for the pilot system, a new version of the TBM was designed, which is meanwhile available and has been shown to provide a symmetric eye diagram. This TBM version will be used for the final phase1 pixel modules that will be installed in CMS at the end of 2016. Regarding the jitter on the port card, an external quartz phase lock loop (QPLL) chip needed to be put in between the tracker phase lock loop (TPLL) and delay25 chip, which sets the delay parameters for control clock and signals, on the pilot port card. For the phase1 port cards, the design has been changed and the QPLL chip is incorporated in the PCB. These improvements proved that the pilot system plays an important role for the pixel phase1 upgrade and it is teaching us valuable lessons even before it is operated in CMS.

5. Conclusion

The pilot system has been built with pixel phase 1 prototype electronics. It has been tested at CERN on the surface and was installed in CMS with the current pixel detector in December 2014. It has been commissioned in CMS after installation and modifications to DAQ, DCS and DQM are ongoing. During the tests on the surface we have learned valuable lessons that lead to new designs for the TBM and the port card for the phase1 upgrade. The pilot system will take collision data in CMS with the current pixel detector during 2015-2016 which will help to gain operational experience with digital modules and the new readout chain.

References

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