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Vertexing at the ILC

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The International Linear Collider (ILC)has been very prominently mentioned in the international strategy documents for high energy physics and here is a strong interest in Japan to become the host country for the ILC. Two detectors have been proposed for the ILC, the SiD and ILD concepts. They have both been validated by an international advisory committee and Detailed Baseline Designs have been presented in 2012. While both detectors are built for particle flow, their approach to tracking is quite distinct. While ILD uses a combination of a TPC with silicon detectors, SiD has an all-silicon detector approach to tracking, with a fully integrated tracker. First an overview of both concepts will be given and then the recent technology developments for both vertex and tracker sensors, as well as the state of the reconstruction software suites, will be reviewed.

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1. Introduction

The International Linear Collider (ILC) [1] is a proposed e^+e^- collider at the energy frontier. The ILC is a 31 km long linear accelerator using superconducting cavities (see Fig. 1) with a baseline center-of-mass energy of 500 GeV. The ILC will provide polarized beams for both electrons (80%) and positrons (30%), which is a unique capability of linear colliders. The ILC project includes a clear upgrade path to center-of-mass energies of 1 TeV, or even slightly beyond. The ILC has a mature baseline design which has been summarized in the Technical Design Report (TDR), which was presented in 2012 [2, 3].

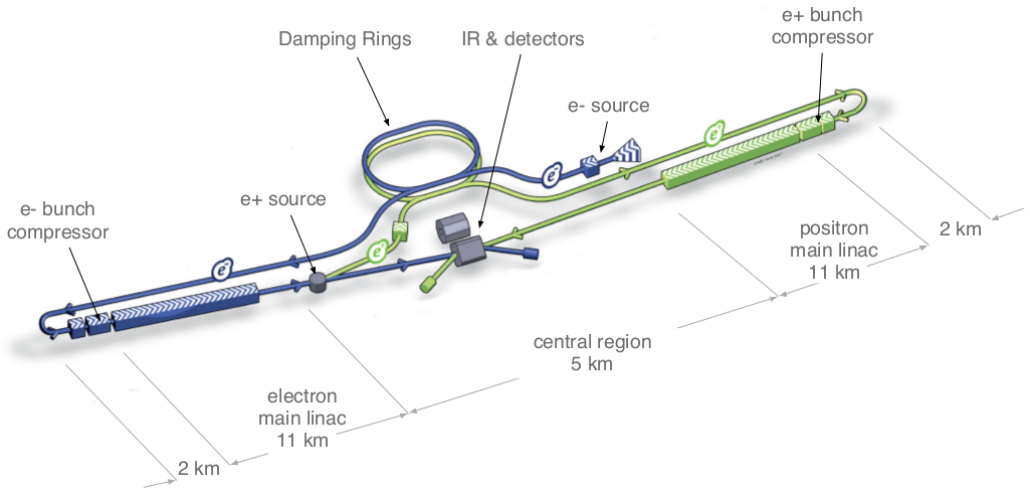

Figure 1: Schematic layout of the proposed International Linear Collider [1]

The ILC physics program will complement the one at the Large Hadron Collider (LHC) at CERN and it will provide key precision measurements of the Higgs boson and Top quark properties. The ILC will perform searches for new physics beyond the Standard Model [4] as well, particularly in areas, where the LHC is not sensitive. Currently two detectors are foreseen for the ILC, sharing one interaction region in a push-pull operation scheme. Both detector concepts, SiD and ILD, have been extensively studied [5] and in both of them the vertex detectors are key elements for the planned precision measurements.

This paper is organized as follows: first a short summary of the ILC physics case is presented and then an overview of the two ILC detectors is given. The second part of the paper will focus on the vertexing at the ILC, outlining the general requirements and then summarize the latest developments both on the Vertex Detector technology itself and on the associated software developments. In the last part a summary of the current ILC status in Japan is given.

2. ILC Physics case

After the discovery of the Higgs boson at the LHC by the ATLAS and CMS Collaborations [6, 7] in 2012 both experiments have performed many analyses to establish the mass and the properties of the newly found particle. Its mass has now been measured to be 125.09 ± 0.24 GeV/c^2

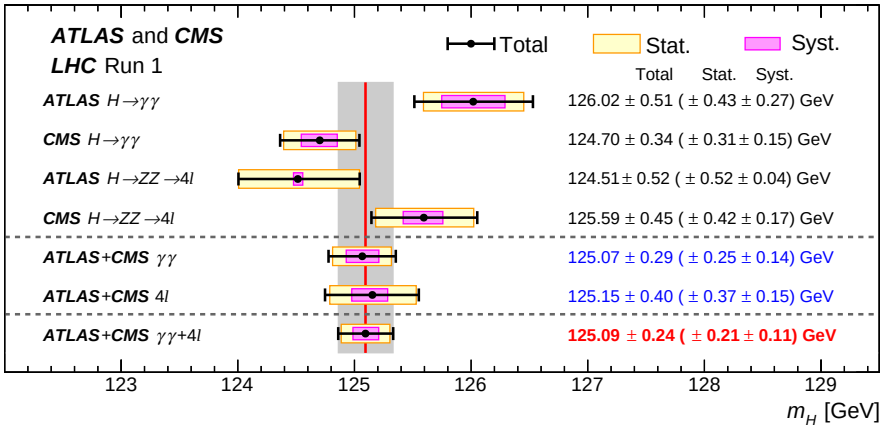

Figure 2: Higgs Bosons results from the LHC: The Higgs Boson mass measurements from both ATLAS and CMS and the combined analysis. The current average mass is m_H=125.09 $\pm$ 0.24 GeV/c^2 [8].

(see Fig. 2) and all the measurements indicate that this particle is very much compatible with the predicted properties of the Standard Model Higgs Boson.

It is expected that especially the signal strength (and therefore the Higgs Boson branching ratios) would be very sensitive to physics beyond the Standard Model (SM) and any deviation there would indicate that this particle is not the Higgs Boson predicted in the SM. However, currently there is very little evidence for any deviation (see Fig. 3) and therefore one must conclude, given the current results from LHC Run-I, that this Higgs Boson looks very much like the Standard Model Higgs Boson.

The ILC will complement the LHC with precision measurements for both Higgs and Top. In order to establish the required accuracy on the measurements of the Higgs Boson branching ratios, it is quite instructive to look at the predicted deviations for a set of models [10]. The expected deviations are all in the order of a few percent (see Fig. 4) and therefore to exclude the models, the ILC does require percent-level accuracy for the branching ratio measurements.

For the measurements of the Higgs Boson properties, the ILC will perform all the measurements of the LHC, but in a much cleaner environment. It will also perform measurements of the $H \to c\bar{c}$ and $H \to gg$ decay modes, which are very challenging for the LHC detectors. One unique measurement at the ILC is measuring the total width of the Higgs Boson by using the recoil-mass approach. In this method the process $e^+e^- \to ZH \to ffH$ is reconstructed by using only the two fermions from the Z decay without any requirements on the Higgs decay. This enables the measurement of the total width directly and thereby to severely constrain e.g. invisible decay modes.

While the ILC physics program has a strong emphasis on Higgs precision physics, the ILC will also perform key measurements for top-quark physics and will measure the top-quark mass to an accuracy of better than 100 MeV/c^2. This is accompanied by a strong electroweak physics program and searches for physics beyond the Standard Model. All these measurements benefit from the unique ILC environment and of course from the detectors that will offer an unprecedented performance.

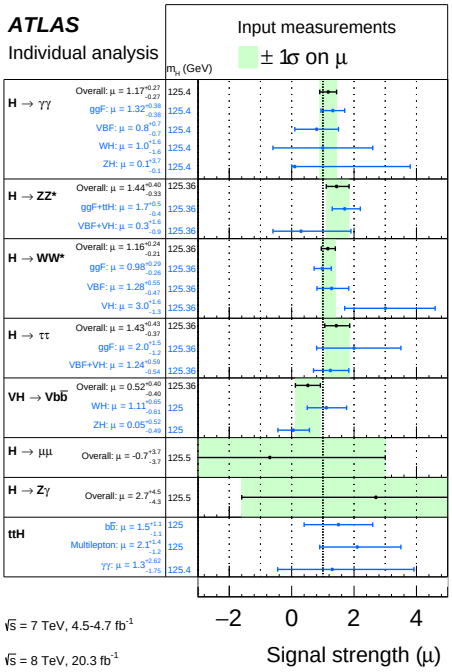

Figure 3: Higgs Boson results from the LHC: Summary of the signal-strength measurements in ATLAS (left). The Higgs Boson mass column indicates the m_H value at which the result is quoted. The overall signal strength of each analysis (black) is the combined result of the measurements for different production processes (blue) assuming Standard Model values for their cross-section ratios. The error bars represent the $\pm$ 1 σ total uncertainties. The combined signal strength of the $H \to \gamma\gamma$ analysis also includes the ttH contribution which is listed separately under ttH production[9].

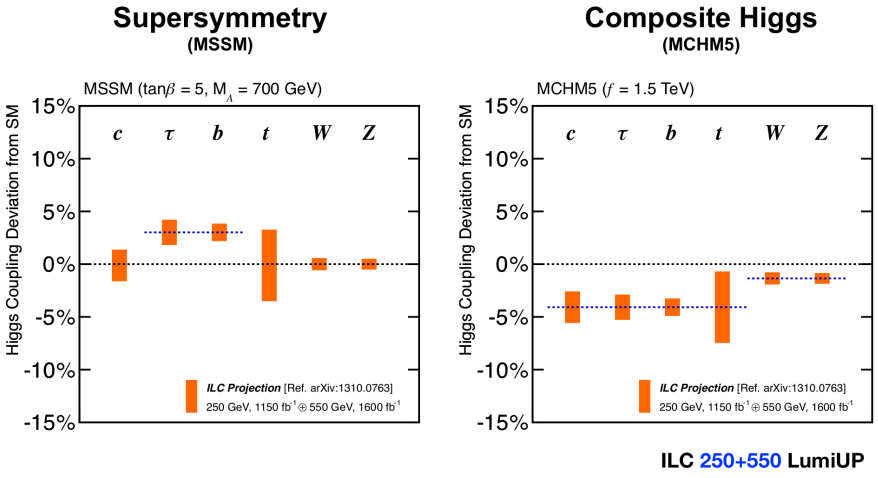

Figure 4: The deviation of the Higgs Boson branching ratios compared to the Standard Model for a Supersymmetric Model (left) and a model with composite Higgs Bosons (right) [10]. In both cases the expected deviations are only a few percent. The bars indicate the projected precision of the ILC using a specific running scenario.

3. ILC Environment and Detectors

The environment at the ILC is vastly different than the one at the LHC. This is partly to the physics of e^+e^- collisions, but also due to the unique beam structure of a linear collider. The ILC delivers collisions in bunch trains with 1312 bunches with 554 ns spacing in the 500 GeV baseline layout. For the proposed 1 TeV operations and the Luminosity upgrades, the number of bunches roughly doubles, while the bunch spacing gets reduced to 366 ns. After each bunch train, there is a quiet time of 199 ms. This is very much in contrast to the LHC with 2880 bunches and 25 ns spacing and the long quiet time actually allows the powering down of the front-end electronics in order to reduce the power consumption. Given the beam structure, power saving of O(100) are possible. In terms of occupancy, one moves from more than a hundred interactions per crossing - the expectation at the High-Luminosity-LHC - to about one physics event per train. The actual occupancy in the detectors is dominated by beam backgrounds and noise.

These unique conditions have quite some impact on the overall detector design. The event data buffered is on the front-end electronics during the train and is only read out at the beginning of the quiet time. The front-ends are then powered off to lower power consumption, which for many detectors eliminates the need for liquid cooling and the associated systems. Instead of having a dedicated trigger system, the whole detector is being read out and the interesting events are selected offline.

As ILC physics involves a large fraction of multi-jet final states, an excellent jet energy resolution is very important. The physics goal is to disentangle a hadronic W decay from a hadronic Z decay, which mandates a jet energy resolution of $\approx 30\%/\sqrt{E}$. The use of Particle Flow Algorithms is currently considered to be key idea to achieve this goal.

Several detector concepts have been proposed for the ILC [11, 12, 13] and after an international review, two detectors - SiD and ILD - have been validated and presented a "Detailed Baseline Design" (DBD) in the ILC TDR [5] (see Fig. 5).

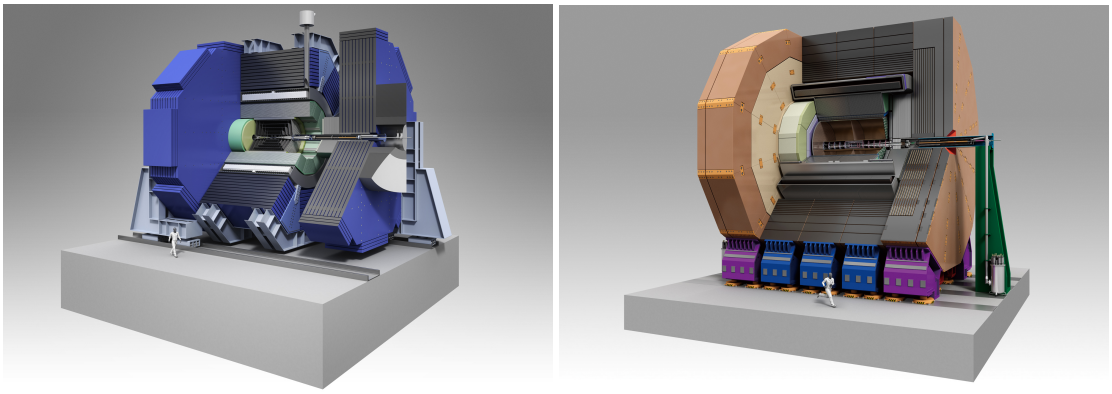

Figure 5: The two ILC detector concepts, SiD (left) and ILD (right)

Both designs are built upon the PFA paradigm which is combining all available reconstruction information: Momentum (Tracker), Energy (Calorimetry) and Particle type (PID). In a typical jet at the ILC, 60% of the energy comes from charged particles, 30% from photons and only 10% neutrals. In order to optimally exploit PFA, there has to be excellent tracking and a highly granular

calorimetry in order to resolve individual showers and accurately match them with the tracking information. This also implies that the entire calorimeter is placed inside the solenoid. In the implementation there are significant differences between the two detector concepts, especially in the tracking and vertexing detectors.

SiD is using a compact detector design with a outer tracker radius of 1.25 m and a solenoid with a 5 T field. The tracking and vertexing at SiD is based on an all-silicon approach. The tracking system consists of a five layer pixel vertex detector and a five layer silicon strip tracker in the barrel. In the endcaps there are seven pixel detector disks and four strip detector disks. This provides a low-mass system with a few (a maximum of 12) highly precise hits over a large polar angle (see Fig. 6). All hits have single-bunch time-stamping making the tracking more robust against beam backgrounds.

ILD is significantly larger, which an outer tracker radius of 1.8 m and a large solenoid with a 3.5 T field. The approach of ILD is build around a large Time Project Chamber (TPC), complemented with a three double layer vertex detector and a set of intermediate silicon layers. In this solution one obtains a high hit redundancy with up to 228 hits (see Fig. 6). Both detectors have the

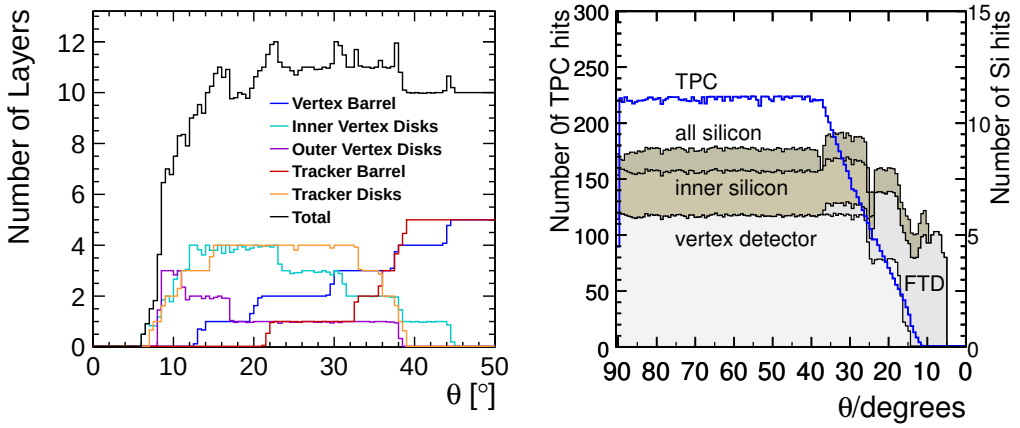

Figure 6: The available hits in both the vertex detector and the main tracker depending on the polar angle for SiD (left) and ILD (right). Both detectors have an excellent coverage down to very small angles.

goal of keeping the material budget below 20% of an radiation length in the entire tracking system, which has been demonstrated in the simulation of the DBD detectors [5]. In order to achieve this goal, the use of power-pulsing is essential and the goal is to keep the power consumption low enough that the tracking detector can be air-cooled.

For the Vertex detectors SiD and ILD have picked different choices in their baseline designs. SiD uses a design based on single-sided layers with five layers in the barrel, four endcap disks and three additional forward pixel disks (See Fig. 7). The single hit resolution is required to be less than 3 μm which implies pixel sizes of $\mathcal{O}(20\mu\text{m})$ or less depending on the readout architecture. The goal for the material budget is 0.1% of a radiation length (X_0) and in order to effectively use air-cooling the power consumption needs to be less than 130 μW/mm^2. Single bunch timing resolution is, as for all SiD subsystems, a general requirement. ILD has a slightly different approach by proposing

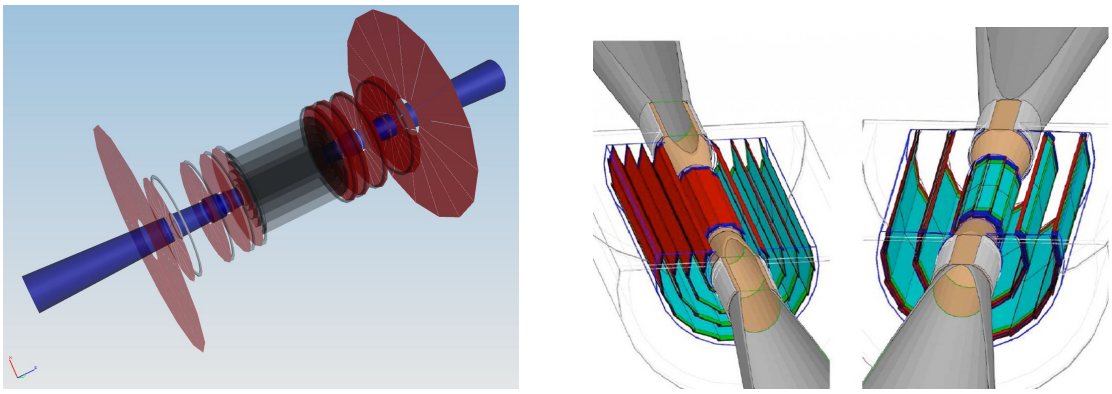

Figure 7: The vertex detector layouts of both SiD (left) and the two layout variants for ILD (right) showing the different approaches of both concepts

a long-barrel layout with either five single layers or three double-sided layers. Overall the pixel requirements are similar but ILD has not specified any time-stamping requirements yet.

4. Vertexing technologies for the ILC

In this section, a summary of some of the recent pixel developments will be given; more details and a broader overview on the very active field of Vertex detector R&D are given in [14, 5]. The various technologies proposed basically solve the occupancy issues by moving to very finely grained pixels, e.g. 5 μm and then integrate over the entire bunch train, go with larger pixels $\mathcal{O}(25\mu\text{m})$ with single bunch time-stamping or go for a solution somewhere in between (time-slicing).

4.1 Fine-Pixel CCD (FPCCD)

The FPCCD [15] group has been driving the development of a CCD-based device for the ILC. In order to compensate for the relatively slow readout of the CCD architecture the FPCCD uses very small pixels (5 μm). The current prototype has achieved a pixel size of 6 μm $\times$ 6 μm and is read out during quiet time. The silicon thickness is just 50 μm and it needs to be operated at -40 degrees Celsius. Recently the radiation hardness has been studied, which the CCD is inherently sensitive to due to the multiple charge transfers. The current results are quite promising and the final goal is to withstand $1{\cdot}10^{12}$ neq/cm^2. FPCCDs are one of the candidate technologies for ILD vertex detector.

4.2 DEPFETs

The DEPFET[16] devices use small pixels ($\approx$ 20 μm) to achieve an excellent single point resolution of $\approx$ 3 μm). The thin sensors (75 μm) have a large signal-to-noise and minimize support & services at the same time by using the silicon itself as a support structure. The pixels are read out using a rolling-shutter approach, where one row is constantly being read out. The goal is to take as many frames as possible to minimize occupancy, so currently about 1/50 μs for the

entire frame [17]. A conceptual look at a DEPFET ladder, including all the required periphery, is shown in Fig. 8. The DEPFET sensors are radiation tolerant up to 1MRad and 10^{12} neq /cm^2 for ten years operation (e^- in the MeV range). DEPFET sensors are going to be used in the Belle-II PXD[18], so there will be a lot of experience with this kind of sensors.

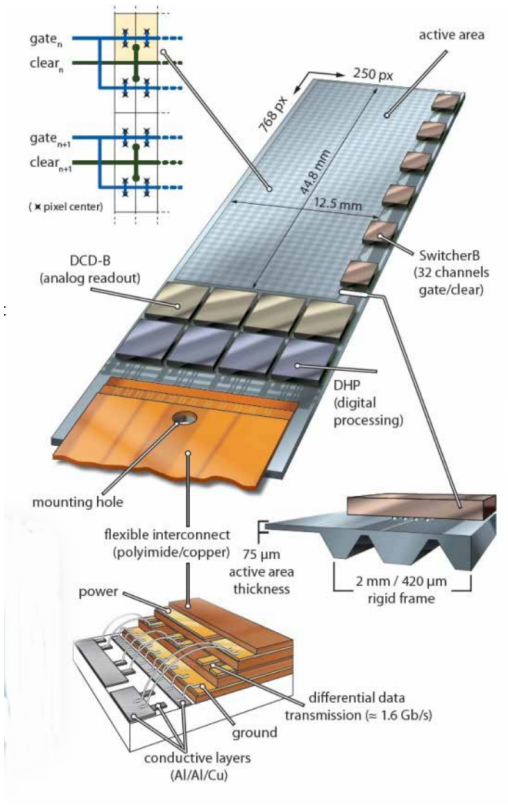

Figure 8: The DEPFET vertex detector ladder showing the sensors, the support ASICS for reading out the DEPFETS and the interconnects at the end of the detector ladder [17].

4.3 Monolithic Active Pixel sensors

Monolithic Active Pixel Sensors (MAPS) have been proposed in the early 90s as an alternative to CCD sensors (see e.g.[19]). They use standard CMOS processes and combine both the active sensor and the readout in one silicon layer. The basic MAPS cell for particle detection [20] is built using a three transistor (3T) structure, however over time various modifications to this design have been made.

A basic limitation of the MAPS devices in general is the charge collection mechanism, which is driven by diffusion instead of drift like in a classic silicon detector. This has been mitigated by using thicker and more resistive epitaxial material [21] or dedicated High Voltage CMOS processes [22]. At the same time the integration of full CMOS has been limited because of the parasitic charge collection of PMOS transistors. This has been addressed by embedding deep p-well implants, which allow the use of full CMOS capability within the pixel [21]. Alternative approaches use the

Silicon-on-Insulator (SoI) technology in order to implement full CMOS and have a thick active area to collect charge in the carrier wafer layer [23]. Another way to increase particularly the noise performance is to move from a 3T structure to a 4T structure, like e.g. with the FORTIS chips or CHERWELL chips [24, 25]. Finally there is a move to smaller deep sub-micron structures in order to make smaller pixels, using 90 nm processes or smaller, which has been for example explored by the Chronopixel chips [26]. A common theme for all MAPS devices is, that they allow having very small pixels with $\mathcal{O}(25\mu\text{m})$ or smaller, which is close to the ILC goal. MAPS use either time-stamping or time-slicing technology depending on the architecture.

The PLUME collaboration [30] is using MIMOSA CMOS Pixel [27] sensors to build low-mass modules, so-called ladders. The MIMOSA family of chips has been successfully used in the EUDET/AIDA telescopes [28] and in the STAR heavy-ion experiment [29] at RHIC in Brookhaven. The PLUME collaboration is currently working on designing prototype ladders for ILC vertex detector. The latest prototype of a PLUME ladder, which has been produced, integrates six MIMOSA26 sensors on each side. The sensors are glued on a kapton flex tape, where two options using copper or aluminum traces are being studied. The two modules are then glued on a common mechanical support consisting of 2 mm thick Silicon Carbide Foam with a fill factor of only 4%. The goal in terms of radiation length is to achieve 0.35% X_0 for a complete double-sided ladder. MAPS is a technology considered both by SiD and ILD for their vertex detectors.

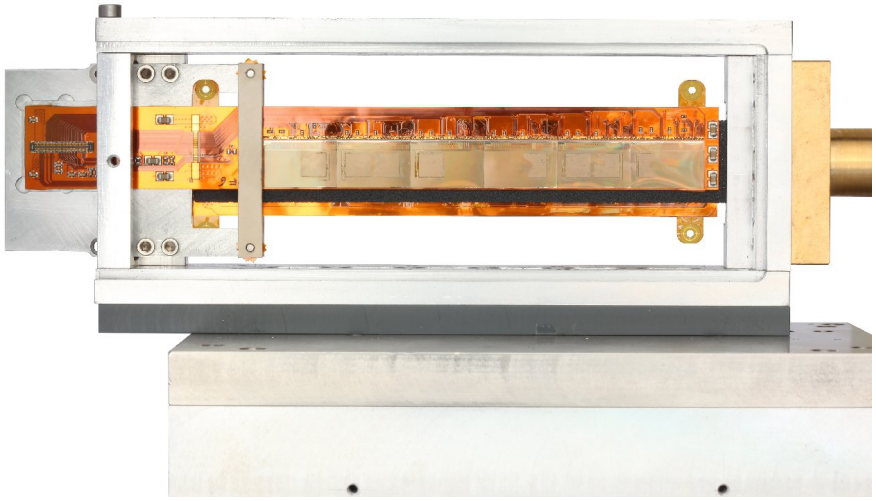

Figure 9: The first prototype of a double-sided PLUME ladder for future ILC vertex detectors consisting of six MIMOSA26 sensors on each side with a sensitive area of 12 cm^2 in total.

4.4 3D Integrated Pixel Sensor Developments

In the context of silicon pixel detectors, 3D-Integration refers to devices were several wafers have been interconnected. This is achieved by the use of Through-Silicon-Vias (TSV) and the use of various bonding techniques (Oxide-, polymer-, metal-, or adhesive bonding) to bond the different

wafers together. Depending on the 3D technology, either wafer on wafer, chips on wafer or chip on chip methods are used. This technology allows a fully active sensor area with independent control of the substrate materials for each of the individual wafer layer, the so-called tiers. This enables the optimization of the fabrication for each tier depending on its foreseen function. Increased circuit density due to multiple tiers of electronics allows advanced in-pixel data processing in very small pixels, which is one of the key ingredients for an ILC Vertex detector. A basic demonstrator chip, the VIP2b [31] has recently been developed. It features an array of 192×192 pixels with a pitch of 24×24 μm^2 pixels with an 8 bit digital time stamp. The data can be readout between ILC bunch trains and is already sparsified. The chip uses wafer-wafer bonding and post processing of the two layers done in 130 nm technology. A first result - a radiogram using a cadmium source- is shown in Fig. 10. While this technology is currently still in its infancy it is a very promising approach for the upcoming ILC vertex detectors.

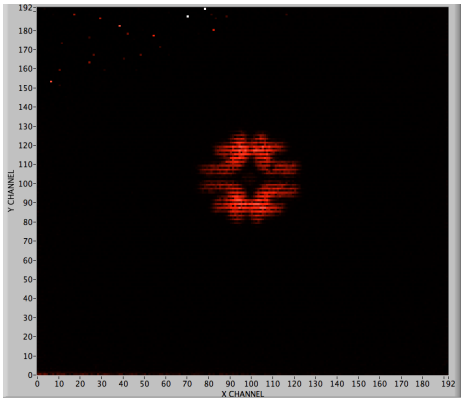

Figure 10: Cd^{109} radiogram of a tungsten mask record with the VIP2b chip [31]

4.5 Technology summary

The vertex detectors for the ILC are technologically challenging, but the HL-LHC detectors will bring a lot more experience in terms of data rates, cooling, mechanics and powering schemes. The sheer number of channels is impressive (1.7 Gigapixels), however the total active area is rather small (0.7 m^2). Both ILD and SiD plan for a late pixel technology decision, which is possible thanks to the projected assembly time and the current installation plans, which foresee the installation of the Vertex detector only at the end of the detector assembly. Given the total construction time of the ILC, which is around ten years, it seems very feasible to make a final technology choice even halfway through construction.

5. Reconstruction Software

For the DBD both concepts had a full GEANT4-based [32] detector simulation with full reconstruction. Both SiD and ILD use a common event data model, LCIO [33] which allows easy sharing of results. There is a complete simulation of the beam backgrounds including the pair production and the background from $\gamma\gamma \rightarrow$hadrons processes [5].

The vertexing resolution is better than ≤ 4 μm in both in the xy-plane and in z as shown in Fig. 11. For the flavor-tagging, both concepts use the LCFI [35] and LCFIPlus [36] packages. A detailed review about the ILC vertex software has been presented in [34]. The flavor-tagging performance for di-jets in ILD is shown in Fig. 11, demonstrating both the b- and c-tagging capabilities of the ILC detectors. Recent developments include both the inclusion of the recent changes of the

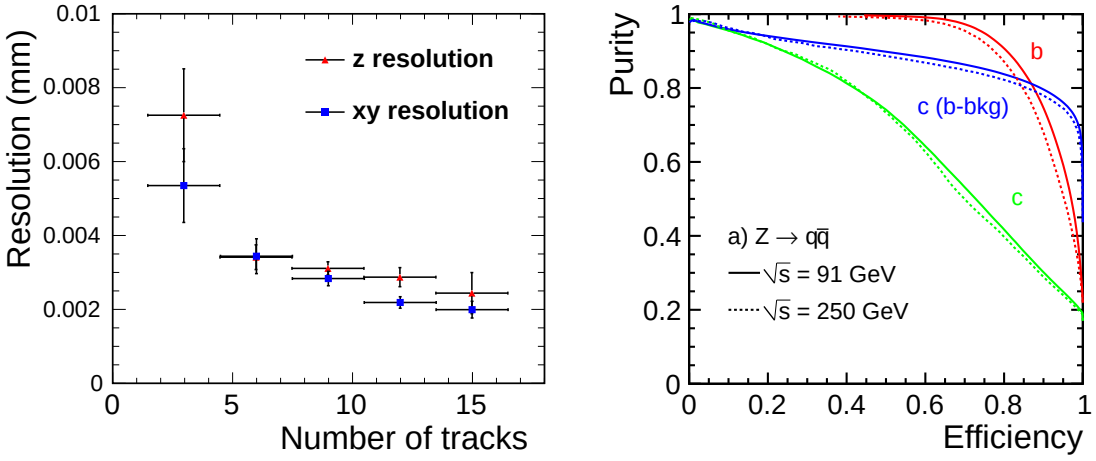

Figure 11: The vertexing resolution for SiD in both xy and z depending on the number of tracks associated to the vertex (left) and the ILD flavor-tagging performance for di-jets showing both the b-tagging and c-tagging performance as well as the performance of separating c-jets from a b-jet background (right).

machine-detector-interface and also improvements in the software itself. Among these is the switch to a new geometry system (DD4HEP [37]) and improved tracking software as well. The tracking & vertexing software has been extended with low-p_T tracking, adaptive Vertex fitting using weighted tracks and a π^0 finder to improve the resolution on the vertex mass. All these extensions clearly demonstrate the potential of the ILC vertex detectors and also show that there is even more to come in the upcoming years.

6. ILC Project Status

The Japanese HEP community has announced in 2012, that they would be interested to host the ILC in Japan. Two potential sites in Kitakami, Honshu and Sefuri, Kyushu (the so-called Northern and Southern site) were then presented. After the presentation of the TDR [1], an international Expert Panel Review, based on the scientific merits of each site, recommended the Northern Site (see Fig. 12) as the site to be further studied. It is very important to note,that this was a purely scientific decision and the Japanese Government has not yet made a site decision.

The ILC was then discussed by the Science Council of Japan, which recommended to MEXT (Ministry of Education, Culture, Sports, Science and Technology) to set up an ILC task force [38] and academic expert committees to further study the ILC; namely its physics potential and the TDR baseline machine. The committees are then expected to report back to MEXT in Spring 2016.

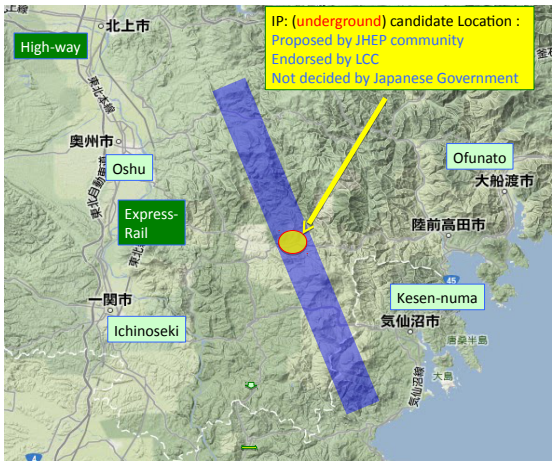

Figure 12: The proposed location of the ILC in the Kitakami mountains region of the Tohoku region in the northern part of Honshu, Japan

7. Summary & Acknowledgements

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References

[1] T. Behnke *et al.*, "The International Linear Collider Technical Design Report - Volume 1: Executive Summary," arXiv:1306.6327 [physics.acc-ph].

[2] C. Adolphsen *et al.*, "The International Linear Collider Technical Design Report - Volume 3.I: Accelerator & in the Technical Design Phase," arXiv:1306.6353 [physics.acc-ph].

[3] C. Adolphsen *et al.*, "The International Linear Collider Technical Design Report - Volume 3.II: Accelerator Baseline Design," arXiv:1306.6328 [physics.acc-ph].

[4] H. Baer *et al.*, "The International Linear Collider Technical Design Report - Volume 2: Physics," arXiv:1306.6352 [hep-ph].

[5] T. Behnke *et al.*, "The International Linear Collider Technical Design Report - Volume 4: Detectors," arXiv:1306.6329 [physics.ins-det].

[6] G. Aad *et al.* [ATLAS Collaboration], Phys. Lett. B **716** (2012) 1 doi:10.1016/j.physletb.2012.08.020 [arXiv:1207.7214 [hep-ex]].

[7] S. Chatrchyan *et al.* [CMS Collaboration], Phys. Lett. B **716** (2012) 30 doi:10.1016/j.physletb.2012.08.021 [arXiv:1207.7235 [hep-ex]].

[8] G. Aad *et al.* [ATLAS and CMS Collaborations], Phys. Rev. Lett. **114** (2015) 191803 doi:10.1103/PhysRevLett.114.191803 [arXiv:1503.07589 [hep-ex]].

[9] G. Aad *et al.* [ATLAS Collaboration], arXiv:1507.04548 [hep-ex].

[10] D. M. Asner *et al.*, "ILC Higgs White Paper," arXiv:1310.0763 [hep-ph].

[11] H. Aihara *et al.*, "SiD Letter of Intent," arXiv:0911.0006 [physics.ins-det].

[12] T. Abe *et al.* [Linear Collider ILD Concept Group - Collaboration], "The International Large Detector: Letter of Intent," arXiv:1006.3396 [hep-ex].

[13] S. K. Park, F. Grancagnolo, J. Hauptman, A. Mikhailichenko and N. Akchurin, "The 4th Concept Detector for the International Linear Collider," arXiv:0708.0142 [hep-ex].

[14] M. Artuso *et al.*, "Working Group Report: Sensors," doi:10.2172/1128407 arXiv:1310.5158 [physics.ins-det].

[15] C. Calancha Paredes *et al.*, "Progress in the development of the vertex detector with fine pixel CCD at the ILC," PoS Vertex **2013** (2013) 022.

[16] J. Kemmer and G. Lutz, Nucl. Instrum. Meth. A **253** (1987) 365. doi:10.1016/0168-9002(87)90518-3

[17] C. Marinas [DEPFET Collaboration], JINST **10** (2015) 11, C11002. doi:10.1088/1748-0221/10/11/C11002

[18] P. Kodys [DEPFET Collaboration], JINST **10** (2015) 02, C02037. doi:10.1088/1748-0221/10/02/C02037

[19] E.R. Fossum, IEEE Trans. Electron. Devices, 44 (10) (1997), p. 1689

[20] R. Turchetta *et al.*, Nucl. Instrum. Meth. A **458** (2001) 677. doi:10.1016/S0168-9002(00)00893-7

[21] J. A. Ballin *et al.*, JINST **6** (2011) P05009 doi:10.1088/1748-0221/6/05/P05009 [arXiv:1103.4265 [physics.ins-det]].

[22] I. Peric, Nucl. Instrum. Meth. A **582** (2007) 876. doi:10.1016/j.nima.2007.07.115

[23] Y. Arai [SOIPIX Collaboration], "Progress on Silicon-on-Insulator Monolithic Pixel Process," PoS Vertex **2013** (2013) 021.

[24] J. J. Velthuis [SPIDER Collaboration], "First beam test results of the FORTIS sensor," doi:10.1109/NSSMIC.2010.5873919

[25] J. Mylroie-Smith *et al.*, Nucl. Instrum. Meth. A **731** (2013) 137. doi:10.1016/j.nima.2013.05.023

[26] C. Baltay, W. Emmet, D. Rabinowitz, J. Brau, N. Sinev and D. Strom, "Chronopixel Vertex Detectors for Future Linear Colliders," arXiv:1109.2811 [physics.ins-det].

[27] M. Winter *et al.*, "Development of CMOS Pixel Sensors fully adapted to the ILD Vertex Detector Requirements," arXiv:1203.3750 [physics.ins-det].

[28] C. Hu-Guo *et al.*, Nucl. Instrum. Meth. A **623** (2010) 480. doi:10.1016/j.nima.2010.03.043

[29] I. Valin *et al.*, JINST **7** (2012) C01102. doi:10.1088/1748-0221/7/01/C01102

[30] J. Baudot *et al.*, "Development of Single- and Double-sided Ladders for the ILD Vertex Detectors," arXiv:1203.3689 [physics.ins-det].

[31] R. Lipton *et al.*, PoS Vertex **2014** (2015) 045.

[32] S. Agostinelli *et al.* [GEANT4 Collaboration], Nucl. Instrum. Meth. A **506** (2003) 250. doi:10.1016/S0168-9002(03)01368-8

[33] F. Gaede, T. Behnke, N. Graf and T. Johnson, "LCIO: A Persistency framework for linear collider simulation studies," eConf C **0303241** (2003) TUKT001 [physics/0306114].

[34] G. G. Voutsinas [ILD and SiD groups Collaborations], "Vertexing Software and Methods for the ILC," PoS Vertex **2014** (2015) 040.

[35] D. Bailey *et al.* [LCFI Collaboration], Nucl. Instrum. Meth. A **610** (2009) 573 doi:10.1016/j.nima.2009.08.059 [arXiv:0908.3019 [physics.ins-det]].

[36] T. Suehara and T. Tanabe, Nucl. Instrum. Meth. A **808** (2016) 109 doi:10.1016/j.nima.2015.11.054 [arXiv:1506.08371 [physics.ins-det]].

[37] M. Frank, F. Gaede, C. Grefe and P. Mato, "DD4hep: A Detector Description Toolkit for High Energy Physics Experiments," J. Phys. Conf. Ser. **513** (2014) 022010. doi:10.1088/1742-6596/513/2/022010

[38] Science Council of Japan, Report on the International Linear Collider Project, `http://www.scj.go.jp/ja/info/kohyo/pdf/ReportonILC_ExectiveSummary.pdf`