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Chronopixel project status

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A monolithic CMOS pixel detector with time-stamping capability (Chronopixel) is being developed in collaboration with SRI International. The design goals are based on the requirements of an International Linear Collider (ILC) vertex detector. The main feature of the design is that each hit is accompanied by a time tag with sufficient precision to assign it to a particular bunch crossing of the ILC - thus the name Chronopixel. This reduces the occupancy to negligible levels, even in the innermost vertex detector layer, yielding a robust vertex detector which operates at background levels significantly in excess of those currently foreseen for the ILC. Chronopixel differs from the similar detectors developed by other groups by its capability to record time stamps for two hits in each pixel while using standard CMOS processing for manufacturing. The first set of prototype devices was fabricated in 2008, the second prototype in 2012, and the third prototype in 2014. The main goal of the third prototype was to test possible solutions for a high capacitance problem discovered in prototype 2. The problem was traced to the TSMC 90 nm technology design rules, which led to an unacceptably large value of the sensor diode capacitance. Six different layouts for the sensor diode were tested in prototype 3, and tests have shown that the high capacitance problem was solved.

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1. Introduction

Vertex detectors are used for precise measurements in many high energy collider experiments, such as the measurements of the branching ratios of the decay modes of the Higgs boson. To achieve superb flavor-tagging capability, the impact parameter resolution should be 5μm $\oplus$ 10μm/(p $\sin^{3/2}\theta$) which will require spacepoint precision of better than $4\,\mu$m. The transparency requirement on each layer of the vertex detector is $\sim$0.1% X_0. The spacepoint precision of 3.9 μm and transparency of 0.4% X_0 that were achieved by SLD encourages this [1].

Charge Coupled Devices (CCD) are widely used in many technical applications, from digital photography to particle physics vertex detectors like the one used for SLD. They are simple and reliable. However, they are not particularly suitable for experiments with large numbers of background hits because of slow readout. For International Linear Collider (ILC) experiments, hit rates and occupancies result from an estimated 0.03 hits/mm^2/ bunch crossing for the innermost layer, for a bunch train pixel occupancy approaching 10 percent. Reliable track reconstruction in vertex detectors is possible with pixel occupancy of less than 0.1% . To address this problem, we have conceived a project in a collaboration of the University of Oregon, Yale University and Sarnoff Corporation (now known as SRI International) through an R&D contract. The goal of the project is to explore the development of an innovative monolithic CMOS vertex tracker with the ability to record time stamps of up to two hits in each pixel with good enough precision to associate each hit with a particular bunch crossing. We call this device "Chronopixel". The ability to associate each hit with a particular bunch in the bunch train will reduce occupancy to $<< 10^{-4}$ per pixel, giving considerable headroom should occupancies be higher than expected. Discussions with SRI International (then Sarnoff Corporation) on this project started in 2004.

2. Prototype 1 features and test results

The first prototype was designed by Sarnoff Corporation and manufactured by the TSMC foundry in May of 2008. The goal of the first prototype design was a proof of principle. It was manufactured using 0.18 μm technology, the pixel size was $50\times50\,\mu$m^2, and the chip had an array of 80×80 pixels on it. Each pixel contained two 14-bit memory cells to record the time stamp, a calibration circuit to compensate for comparator offsets, a sensor diode, a source follower and a specially designed diode reset circuit which was expected to provide a "soft reset". (The "soft reset" is a Sarnoff propriety method to reduce reset noise.) The simplified block diagram of the first prototype pixel is presented in figure 1. In addition, the chip contained circuitry to implement a sparse readout scheme, allowing it to read only pixels with hits.

Comparator offset calibration was an essential part of the design, as the spread of the comparator offsets due to fluctuation in the transistor parameters (like channel and gate width and length) was larger than the required precision of the comparator threshold setting. The calibration circuit was based on a 10-bit register, which was sequenced during the calibration process until the comparator fired. Then the register sequencing stopped and the output voltage of the circuit was applied to compensate for offset spreads during hit detection and recording.

The first report on the status of the Chronopixel project was given at the LCWS2008 conference in November, 2008 [2].

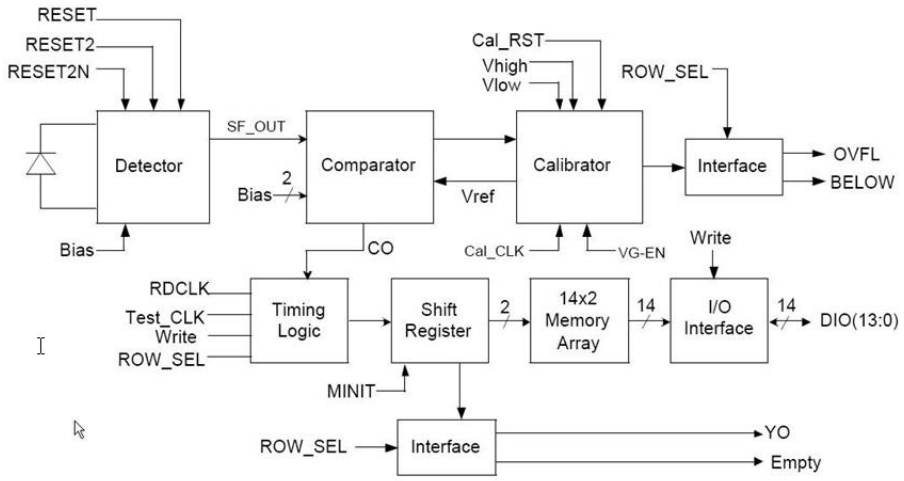

Figure 1: Simplified block diagram of the pixel in the Chronopixel prototype 1.

The first prototype was thoroughly tested in a test stand at SLAC. Test results led to the following conclusions:

2.1. We have proven that we can record time stamps in every pixel with time resolution better than 300 ns. (We have tested it down to 150 ns.)

2.2. We have tested sparse readout, allowing us to read only pixels with hits, thus reducing readout time to the level allowing readout of all pixels in the sensor in the intervals between bunch trains.

2.3. We have tested pulsed power for the analog part of the pixels and have proven that turning power on about 100 μs before the bunch train and turning it off between bunch trains does not create any problems for the threshold-setting accuracy in the comparators.

2.4. The noise figure with "soft reset" was found do be within specifications. It was 24 e^- r.m.s., when the specification was 25 e^- r.m.s.

2.5. We found that the comparator offset spread is a few times larger than we expected, and our offset compensation circuit does not have enough granularity to compensate for offsets with the required precision.

Some results of the prototype 1 tests were reported at the DPF-2011 Conference in August, 2011 [3].

3. Prototype 2 features

In the second prototype we addressed the offset compensation precision problem by implementing an analog instead of digital offset calibration circuit. The idea was to store the voltage which was needed for the offset compensation on special capacitors which were large enough to hold the voltage stably (within the required precision of about 1 mV) during the bunch train (1 ms). Because of the analog form of the voltage storage, there was no granularity in voltage levels.

Another modification in prototype 2 came from the decision to try all NMOS electronics (instead of CMOS) inside the pixels. In the CMOS design there are nearly equal numbers of NMOS

and PMOS transistors. Since PMOS transistors are formed on NWELLS, which need to be under positive potential relative to the P-type substrate, they are competing with the sensor diode (which is also a NWELL) for signal electrons generated inside the epitaxial layer by charged particles. Therefore, the signal charge collection efficiency would always be much less than 100 percent (depending on the ratio of the sensor diode area and the area of the PMOS transistors). If we could avoid using PMOS transistors, the charge collection efficiency would improve and could approach 100 percent. To avoid higher power consumption of the memory cells built on all NMOS transistors, a special memory cell design was suggested. It used a switching capacitor array as a substitute for the high resistivity load. A SPICE simulation showed that such a design could have negligible power consumption, close to that of CMOS memory. However, building comparators on all NMOS transistors appeared to be a very difficult task, and would require allocation of a considerable portion of the area inside a pixel for the comparator. Instead, it was decided to sacrifice some charge collection efficiency and allow use of PMOS transistors in comparators. Depending on the sensor diode size it would reduce charge collection efficiency to values of 60 to 80 percent.

It was decided to built prototype 2 using 90 nm technology, which would allow reduction of the pixel size to $25\times25\,\mu\text{m}^2$. To simplify the chip design it was decided not to implement sparse readout in this prototype. Sparse readout was tested in prototype 1, but could not be simply copied from the prototype 1 layout because of the different pixel pitch. To save time and money, we decided to use a simple row/column-addressed readout for this prototype.

4. Results of prototype 2 tests

We received packaged prototype 2 chips in June of 2012. First we checked if an all-NMOS memory worked. Without it all tests would be impossible. It appeared that it worked as expected. After that we could check comparator offsets compensation with analog offset storage. Results are shown in figure 2. Without compensation (left), the offset spread was much larger than it was in prototype 1. The r.m.s. of this distribution in prototype 1 was 6.1 mV, and in prototype 2, as seen on the left plot on figure 2, it was 31.3 mV - five times larger. It is not a surprise, as the 90 nm technology used for prototype 2 was expected to have larger relative fluctuations of transistor parameters compared to the 180 nm technology used in prototype 1. The figure shows that the offset compensation was working well in prototype 2.

The next issue to test was the sensor diode capacitance. In prototype 1 we used a rather large area sensor diode (about 100 μm^2) because signal amplitude and charge collection efficiency were not supposed to be tested in prototype 1. (We expected it would be poor because many PMOS transistors were used there.) However, for prototype 2, the goal of getting a high charge collection efficiency was the motivation for using all NMOS electronics. And for optimization of signal/noise ratio we implemented two pixel options here - with a 9 μm^2 sensor diode and a 20 μm^2 diode. It was expected that the smaller diode would have the smaller capacitance, thus generating larger signal amplitude for the same amount of charge, but would collect a smaller fraction of the charge from the sensitive volume because of the presence of a small number of PMOS transistors competing for collection of the signal electrons. Simulations indicated that optimal diode size should be close to 20 μm^2 and we wanted to check our simulations.

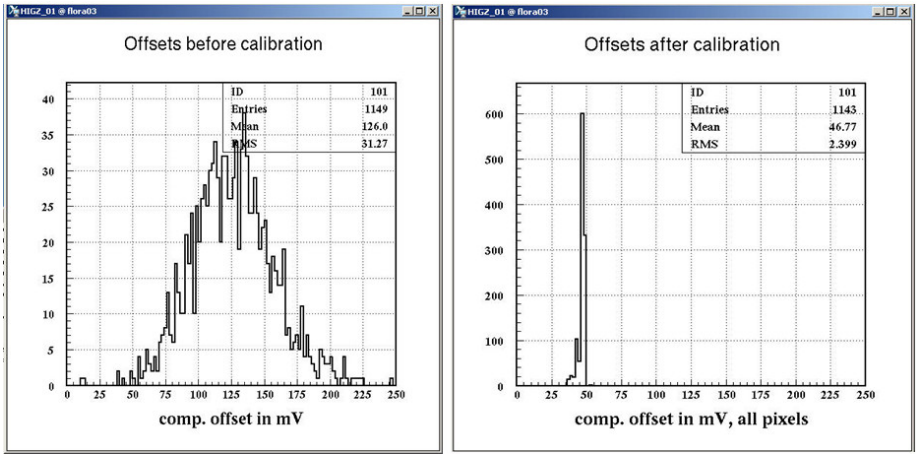

Figure 2: Comparator offsets compensation performance in prototype 2. On the left plot the distribution of comparator offsets without compensation is shown and on the right plot, after compensation. Mean values in both distributions are arbitrary; what matters here is the width of the distributions. The plots show that analog offset compensation circuits are working well.

However, tests with a Fe55 source revealed completely unexpected results. Figure 3 presents the test results with a Fe55 source. From the maximum signal values we could estimate a sensor capacitance as ∼5 fF for prototype 1, 9.6 fF for the small sensor diode option, and 10.3 fF for the large diode option of prototype 2. Stray capacitances of the diode reset circuit and source follower input can be estimated as ∼1 fF for all cases. But the diode area in prototype 1 was about five times larger than the large diode option in prototype 2, and ten times that of the small diode option. So we could expect ∼1.4 fF for the small diode and ∼1.8 fF for the large diode. What factor had we overlooked?

TSMC has design rules for the 90 nm feature size which prohibit making a window in the p^{++} implant for the deep NWELL. The deep NWELL forms the body of the sensor diode, and if it is placed without any gap into the highly doped p^{++} top layer of the chip, the thickness of the depleted layer on its side walls is very small (of the order of 0.1 μm) and it creates a large capacitance for the sensor diode. To achieve an acceptable efficiency of charge particle registration in 20 μm (which we plan for the final sensors) we needed a sensor capacitance of the order of 2-3 fF. So we needed to find a way to bypass that design rule. Just decreasing the sensor diode size would not help here, as we had about 10 μm^2 of PMOS transistors competing for charge collection. Going to a smaller charge collection diode would decrease charge collection efficiency, thus not helping to increase the signal.

5. Prototype 3

In prototype 3 we decided to test a few strategies to fight the high sensor capacitance problem. One obvious way was just to ignore the design rule (obtain a waiver from TSMC) and take responsibility for any consequences. Another way was to implement a so-called "natural transistor", which was allowed by TSMC design rules. The "natural transistor" uses a p substrate as its body, placing two n-type diffusion areas on top of it, which would work as the source and the drain of transistor.

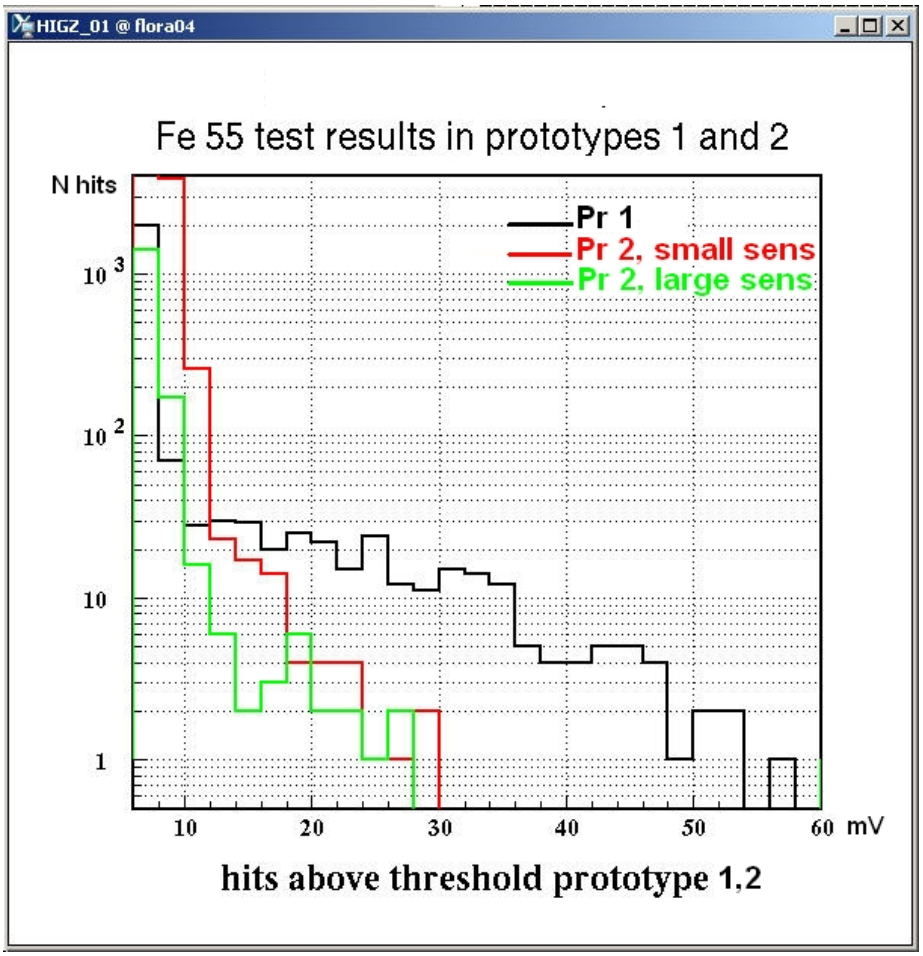

Figure 3: Fe55 source signal above threshold distribution for prototype 1 (black curve) and prototype 2 small (red) and large (green) pixel diodes.

This structure is allowed by TSMC design rules; however, the gap between these n-diffusion areas and p^{++} implant covering the rest of the chip is restricted, not to exceed 0.5 μm. Since n-diffusion areas are not deep NWELLs, their side walls should not create large capacitance to a p^{++} implant with such a gap. Finally we decided to have six different sensor options for prototype 3:

1. First option would repeat the prototype 2 design (large diode variant) for comparison.

2. Second option violated design rules. Sensor diode was formed as a deep NWELL of the same size as in option 1, but inside the window of 5×5 μm^2 in the p^{++} implant.

3. Third option also violated design rules, but used only a shallow NWELL (about 1.5×1.5 μm^2) inside the window of 5×5 μm^2 in the p^{++} implant.

4. Fourth option followed design rules and implemented a one-finger "natural transistor" as a sensor. Transistor gate, source and drain were all connected and formed a signal node.

5. Fifth option was the same as fourth, but a two-finger transistor layout was used.

6. Sixth option was the same as fourth; however, transistor gate was not connected to source and drain, but to a separate bias net. The bias on it could be controlled externally.

Test results with an Fe55 source are shown in figure 4. The smallest sensor capacitance oc-

curred in option 3, and it met our goal of achieving 2-3 fF capacitance. However, the sensor diode size was very small here - about 2 μm^2 - and it may have caused low charge collection efficiency in the presence of competing PMOS transistors.

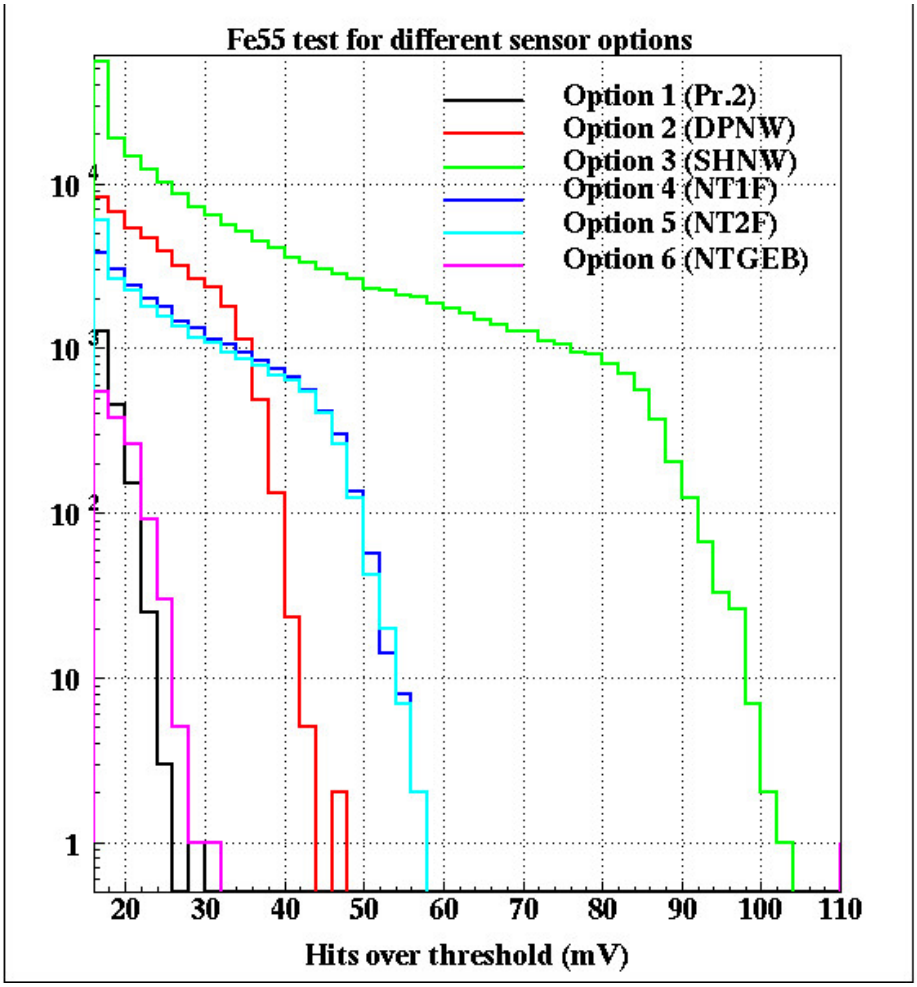

Figure 4: Fe55 source signal above threshold distribution for prototype 3 sensor options.

Table 1 summarizes signal/noise values for the Fe55 signal. The minimum ionizing particle signal in the 20 μm epitaxial layer is approximately the same as the signal from Fe55. So the figures in the table could be viewed as the expected signal/noise ratio for the ultimate sensor. However, they are overestimated as we did not take into account unknown-for-now charge collection efficiencies for different sensor diode options.

6. Conclusion and plans

Prototype 3 tests have proven that a Chronopixel sensor can be built. We have solved all the problems we found so far. However, to accomplish optimum sensor design, more tests are needed. First of all we need to measure charge collection efficiency for different sensor diode options and find the option with the best signal-to-noise ratio. To measure sensor efficiency we will need to

Option	Noise r.m.s. (mV)	Fe55 signal (mV)	S/N ratio
1	1.12	30	26.8
2	1.08	45	41.7
3	1.7	105	61.8
4	1.21	58	47.9
5	1.23	58	47.2
6	0.98	32	32.6

Table 1: Signal/Noise ratio for Fe55. Noise is obtained from noise signal distributions.

experiment with charged particles having enough energy to penetrate through the sensor thickness (together with its ceramic package) and fire a trigger telescope. The source of such particles may be either a radioactive beta source or a test beam. We plan to perform such an experiment. The next step would be to build a prototype sensor of a size usable for a vertex detector (at least a few cm^2), with a final readout scheme. It would be desirable to build such a prototype with a thick epitaxial layer of higher resistivity. There are a few issues to be tested with such a prototype. The major one is the length of the traces; as we move from $\sim$1 mm to a few cm, resistance, capacitance, and crosstalks all raise issues. Experience in building large sensors certainly exists, so there should be no show stoppers, but we need to prove that everything works for our particular sensor. We aim to be ready to build a Chronopixel-based vertex detector in time for the ILC. The Chronopixel sensor may also be of interest for other experiments, such as a Large Hadron Collider upgrade or for the Compact Linear Collider (CLIC) project. For CLIC it would require some modification, such as the addition of a time/time converter to be able to do time stamping in the sub-nanosecond range.

References

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