PROCEEDINGS OF SCIENCE

# New needs and directions in microelectronics and ultrafast electronics

**Angelo Rivetti***
*INFN Sezione di Torino, 10125 Torino, Italy*
*E-mail:* rivetti@to.infn.it

High granularity radiation sensors readout by custom integrated circuits play a fundamental role in modern particle and nuclear physics experiments. The performance improvements made possible by these systems have been recognized also in other domains, such as astrophysics, medical imaging and radiation dosimetry, to name just a few. Custom integrated circuits will be of primary interest for the upgrades of the LHC detectors, where new challenging requirements have to be met, as well as for other experimental facilities planned or under construction worldwide. In the past years, the microelectronic industry has made impressive progress and the trend is expected to continue in the future, giving the chip designers new opportunities to address ambitious goals. In this paper, emerging needs of integrated electronics for particle detectors are discussed and the evolution of ASIC fabrication technologies is briefly reviewed. The impact of these advancements on the design of next generation systems is analyzed.

*INFN Workshop on Future Detectors for HL-LHC*
*16-18 December, 2015*
*Aula Magna della Cavallerizza Reale, Torino, Italy*

*Speaker.





PoS(IFD2015)036

## 1. New requirements in electronics for radiation detectors

Initiated about thirty years ago with the design of the Microplex [1] for the Mark II vertex detector at SLAC, microelectronics for radiation detectors has now become a mature field that involves several engineers and physicists worldwide. The activity was fostered by the development of the electronics for the LHC detectors, all of which incorporate a substantial number of custom integrated circuits. The design of the first generation ASICs for the LHC came along with a major breakthrough, the adoption of standard deep submicron CMOS technologies as the baseline choice for implementing radiation detector electronics. It was in fact proved by a dedicated R&D led by CERN [2] that these technologies combine good analog and digital performance with adequate radiation hardness, well exceeding in this respect the original LHC requirements for ten years of operation (100 kGray of Total Ionizing Dose (TID) and $10^{14}$ 1 MeV equivalent neutrons/cm$^2$).

Mandatory when thousands of channels must be simultaneously readout, the use of integrated front-end circuits offers important benefits also in applications where more conventional alternatives based on discrete component can be considered, as it allows to short the connection length between the detector and its front-end electronics and to reduce power consumption, leading to more compact and higher resolution systems. The advantage of ASICs in the readout of radiation detectors was soon recognized in other domains beyond particle physics and custom integrated circuits are today found in many different fields, from medical imaging [3] to astronomy [4]. Integrated electronics is expected to play an even more important role in the radiation detectors of the future.

At the energy frontier, the next major step will be the luminosity upgrade of the LHC, now scheduled to be completed in 2025. The increase of the peak luminosity from $10^{34}$ to $5{\cdot}10^{34}$ will take to the extreme the already challenging specifications that had to be addressed in the first generation of LHC ASICs. In the inner layers, the hit rate will jump from the present value of 200 MHz cm$^{-2}$ to 3 GHz cm$^{-2}$, leading to an average rate of 75 kHz on a pixel of 50 $\mu$m $\times$ 50 $\mu$m area. The trigger rate is expected to become 1 MHz, requiring a data bandwidth in excess of 1.25 Gbit s$^{-1}$cm$^{-2}$. Trigger matching should take place close to the front-end and larger memory buffers are needed to accommodate a longer latency. In the outer layers, the finer segmentation must be paired with additional functionality, allowing the tracker to generate directly trigger primitives (CMS) or to deliver to the L1 trigger processors a prompt readout of selected regions of interests (ATLAS). The electronics for the calorimeters and muon detectors also need a substantial upgrade to cope with the new pile-up regime, as up to 200 collisions are expected in a 25 ns bunch crossing. A good time resolution (100 ps or better) that could be provided by some detectors (e.g. the electromagnetic calorimeters) is being investigated as an option to mitigate the pile-up issue. The LHCb experiment is moving to a trigger-less readout, while ALICE plans to install already at the next long shut-down a new ultra-low mass tracker. The LHC will likely be followed by a linear collider (ILC or CLIC) or, perhaps, by a muon collider. High granularity and extremely low-mass tracker and high resolution calorimeters will be key systems for these accelerators. In some designs, the anticipated background calls for a time resolution in the order of the nanosecond to allow for efficient rejection.

Nuclear physics experiments also target high luminosity to access rare processes. To cope with the large particle flux, detectors with finer segmentation are needed, making ASICs more

and more necessary also in this domain. Versatile systems are often desired, in which data-push readout architectures are preferred to the more traditional trigger-base approach. A good example is provided by the FAIR complex, that will be a major facility for nuclear physics in Europe and will host several medium scale experiments. A number of chips are under development for the FAIR detectors [5, 6, 7]. In this context, low-power tracking systems combining spatial resolution of 100 $\mu$m or smaller with timing accuracy better than 1 ns and large data bandwidth are one of the challenges that have to be addressed.

Long baseline neutrino experiments and new generation dark matter detectors are entering the multi-ton regime, where it becomes impractical to use discrete electronics. Large dynamic range, low noise and low power are essential for the readout of Liquid Argon TPCs [8, 9]. Integrated solutions have also been explored for directional dark matter detectors [10]. The use of ASICs may also help in reducing the contribution of the electronics to the background, which is paramount for apparatus that look for very rare events and thus require extremely high sensitivity. In several cases, such as LAr TPCs, the front-end must be located inside the cold volume, thus operating at temperatures at which commercial technologies are usually not well modeled.

ASICs, mostly in the form of waveform digitizers, are employed in the electronics of ground-based Cherenkov telescopes. The output signal of a fast photosensor is captured at 1 GSamples/s or more and selective readout is performed on potentially interesting events [11]. Here the challenge is to increase the analog bandwidth, the sampling speed and the rate per channel, while possibly decreasing the power consumption. In photon science, high spatial resolution (better than 100 $\mu$m), large dynamic range ($1 \div 10000$) and fast readout rate must be combined [12, 13].

The specifications of a detector system change significantly between different applications. Albeit not exhaustive, the above examples allow nevertheless to identify challenges that designers of ASIC for radiation sensors are facing:

- The access to rare probes in physics requires detector with increased segmentation and lower material budget, hence the number of channels increases while the power consumption must be reduced. New integration strategies or monolithic realization of the sensor and its front-end electronics are essential to implement lighter systems.

- Many applications favor data-push readout schemes to improve flexibility, which implies large data bandwidth as all events above noise must be transmitted. Efficient signal processing architectures must also be deployed.

- Time resolution is more and more emphasized as mean to resolve pile-up is high intensity environments. This is turn calls for fast front-end that can take full advantage of the intrinsic sensor speed.

The improvement in ASIC performance critically depends on the progress of the microelectronics industry, that provides the technologies to implement the chips. In the next two sections, the status and trends in the microelectronics industry are reviewed and the implications on the design of readout systems for radiation sensors are considered. The attention is focused on CMOS technologies, which cover the large majority of applications.

## 2. Status and trends in IC technologies

In his seminal paper of 1965 [14], Gordon Moore anticipated that the number of components on an integrated circuit would double every year, leading to systems with progressively better performance. This prediction was up to now realized thanks to CMOS technologies, which have been the workhorse behind the computer revolution of the last thirty years. Their success stems from the inherent capability of implementing digital gates with minimal static power consumption. Furthermore, it has been relatively easy to scale-down CMOS transistors, integrating devices with better performance in smaller area. The rules of scaling were comprehensively elucidated by Dennard and co-workers in 1974 [15]. The basic idea was to scale at each generation the device physical dimensions by a given factor $\kappa$, so that the gate density increases by $\kappa^2$. All the operating voltages should also reduced by $\kappa$, to keep the power density constant, thus integrating more functionality for the same power consumption. From one CMOS generation to the next, $\kappa$ is typically 0.7, thus doubling the circuit density at each step. New technology nodes have been introduced at a pace of roughly a new generation every eighteen months, shifting from processes with a minimum gate length of 5 $\mu$m in 1974 to 14 nm in 2015. To grasp the effectiveness of scaling, one can consider that the area of a bit cell for a static RAM memory has been squeezed from 10 $\mu$m$^2$ in 1995 (250 nm node) to 0.0588 $\mu$m$^2$ in 2014 (14 nm technology) [16].

The straightforward constant field scaling proved to be inadequate in the deep sub-micron regime, therefore the original Dennard's scaling had to be adapted. One of the reason is that when the gate-source voltage reaches the threshold, the transistor does not switch-off instantly, but rather displays a bipolar-like behavior. Below threshold, the characteristics of the MOS can be written as:

$$I_{DS} = 2n\mu C_{ox}\phi_T^2 \frac{W}{L} e^{\frac{V_{GS}-V_{TH}}{n\phi_T}} \tag{2.1}$$

For a NMOS transistor is 65 nm, the term $\mu C_{ox}$ can be as high as 650 $\mu$A/V$^2$ and the current for $V_{GS} = V_{TH}$ for a device with unit aspect ratio is about 1 $\mu$A. From 2.1, it can be easily seen that $V_{GS}$ must drop below the threshold by 240 mV in order to reduce the subthreshold current to 1 nA. This prevents the use of too small threshold voltages and thus limits the minimum supply voltage at which CMOS logic can operate. The power supply voltage, for instance, is basically the same in the 130 nm and 65 nm nodes (1.2 V) and it is only reduced to 0.7 V in 14 nm. The power density thus increases from generation to generation. In complex digital chips fabricated in ultra-deep submicron nodes, not all parts can simultaneously work at fully speed in order to prevent an unacceptable self-heating. Therefore, only a fraction of the system is always used at its full potential, an issue known as the "dark silicon problem". The need of a better control of the gate terminal on the channel conductivity has lead to a continuous reduction of the gate-oxide thickness, increasing in turn the specific gate capacitance $C_{ox}$. Below 1.5 nm thickness, the gate leakage current due to tunneling of charge carriers through the gate oxide becomes too large. This led to the introduction of new materials with higher permittivity for the gate dielectric. In most recent technologies, the gate terminal "wraps" around the channel, as shown in Fig. 1 a), originating a new device type called a "FinFET". Copper interconnects, dielectrics with low permittivity to reduce the capacitance between the metal lines, strained silicon channels to improve carrier mobility are other important innovations that have been introduced so far to keep on with the scaling targets. Plans

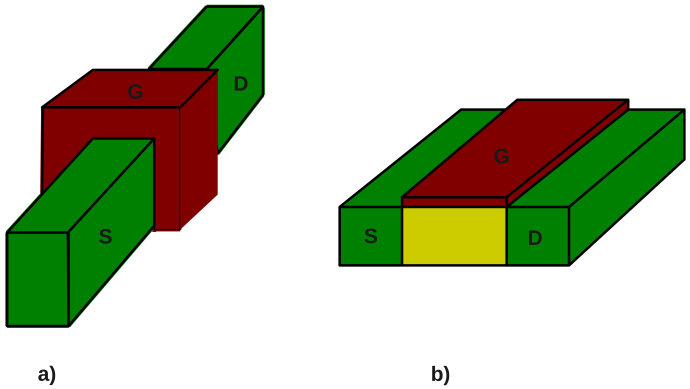


**Figure 1:** Comparison of a FinFET (on the left) and a standard planar MOS transistor (on the right).

in the industry are to further scale down CMOS technologies at least to the 5 nm node. This will likely be achieved by using FinFETs where a material with higher mobility, such as Germanium or III-V composite semiconductors replace Silicon in the device channel. Vertical and horizontal gate-all-around transistors in which the gate completely encircles the channel are other options under investigation. Research is being actively pursued to replace MOS transistors with other devices more amenable to scaling. One possibility are transistors based on carbon nanotubes. Recent results announced by IBM [17] could contribute to solve one key issue limiting the practical use of nanotubes, i.e. the resistance of the contacts necessary to access the transistor channel. This may accelerate the introduction of the carbon nanotube technology and could allow scaling to continue down to at least 1.8 nm. Other promising devices are Tunnel Field Effects Transistors (TFETs), in which the conduction between source and drain is controlled by a quantum barrier modulated by the gate voltage [18]. An interesting feature of TFETs is that their subthreshold slope can be greater than the one of MOS, allowing to turn on and off the device with a smaller voltage swing. Operation at lower supply voltages can thus be achieved, reducing significantly the power consumption of digital circuits. TFETs can also be suited for analog design [19].

At each generation the speed of MOS transistors increases. CMOS technologies have thus eroded the market of bipolar ones and they are extensively used today also in RF applications. An interesting alternative is offered by SiGe BiCMOS, in which ultra-fast bipolar devices can be combined with standard CMOS gates to design fast and high performance mixed signal circuits. However, bipolar transistors reach their peak frequency at higher current density than their MOS counterparts. They are hence mostly interesting to design very fast circuits for data transmission, where power is not the primary issue [21].

Speed in large digital systems is limited by the parasitic of the interconnects. This, combined with the awareness that planar 2D scaling may hit relatively soon its physical limits, has stimulated research on 3D integration. Here, several tiers of electronics, even realized with different technologies, are piled-up and interconnected with vias that run across the individual layer (true silicon

vias, TSV). Many technical challenges still need to be addressed before the 3D approach can be systematically used in high volume industrial production [20], but 3D integration is likely to be one of the tools that will allow the continuation of Moore law beyond what it possible with planar 2D scaling.

The availability of very deep submicron technologies combined with architectural innovations made possible to attain very good progress also in building blocks that are critical in many radiation detector systems, namely ADCs and TDCs. In a 130 nm process, a 50 Msamples/s, 10 bit resolution ADC can be implemented in 0.09 $mm^2$ with 1 mW of power consumption. Time-to-Digital Converters with 20 ps binning, 1 mW power and 1 Msample/s or faster have been reported. Even better performance have been achieved in technologies with smaller feature size. A more detailed discussion of this topic can be found in [22] and references therein.

## 3. Perspectives for radiation detector ASICs

The considerations of the previous section suggest that ASICs for radiation detectors may evolve in the near to medium future along three main paths. The first one concerns signal processing architectures. With ADCs offering 50 - 100 Msamples/s and 1 mW of power, the use of analog memories is justified only when extremely high sampling rates are necessary. In most cases, the ADC can be integrated immediately after the amplifier on a channel by channel basis, and digital filtering and event selection take place in the digital domain. Another option is to exploit low-power and high granularity Time-to-Digital Converters. This is a natural choice for those applications seeking very good time resolution, even though accurate timing information can also be retrieved through waveform sampling. A TDC can be used as well to extract the charge released by the impinging particle in the detector. One choice is to exploit the Time-over-Threshold technique, by measuring the time spent over a fixed threshold by a discriminator driven by the front-end amplifier. TDCs can also serve to implement fast Wilkinson-type digitizers. As an example, a binning of 20 ps allow to cover a 10 bit dynamic range in 20 ns, offering a resolution equivalent to a 50 GHz clock[1]. Digital algorithms can be employed in addition to correct the imperfection of the analog blocks. It is thus expected that front-end ASICs of the future will rely more and more on early digitization, digital calibrations and digital signal processing techniques.

Another line of research will deal with technology. Electronics instrumenting now the LHC detectors is based on 250 nm and many new developments are done in 130 nm. The potential of state-of-the art CMOS technologies for detector readout is yet to be explored. The main reason is that ASICs for radiation detectors are fabricated in small volumes. The main cost for chip fabrication is due to Non Recurrent Engineering Costs (NRE) associated with mask production. To give a reference, the price of a mask set may range from 300.000 USD in 130 nm to 3 millions USD in 28 nm, discouraging the adoption of technologies with smaller feature size. The access to silicon foundries is usually granted by an intermediate service, such as MOSIS in the U.S. and Europractice and CMP in Europe. Prototyping is carried-out through Multi-Project-Wafers,

[1] Observe that the rate performance depends on the TDC architecture. Flash-type TDCs, such as those based on DLLs, are able to take instantaneous snapshots of the timing events. The digitization time thus coincides with the duration of the interval to be measured. Other architectures, like Vernier, have instead conversion times longer than the interval to be digitized.

that allow to share the NRE costs among several users. At present, MPW services offer access to a large variety of technologies, down to the 28 nm node. If most of the signal processing is moved in the digital domain, it must be expected that significant advantages in terms of power consumption and embedded functionality will come from using such advanced processes. CERN has now established a vigorous R&D program for the design of next generation pixel front-ends in 65 nm [23]. The study of even more scaled nodes should also be encouraged.

The third important path involves system integration. 3D integration was already explored by the community with promising results [24] and it is expected to play an increasing role as the technology matures in the industry. Another important step will come from the full exploitation of monolithic detectors based on CMOS Image Sensors technologies. A few process offer today the integration of the charge collecting diode in close proximity of CMOS electronics, allowing for monolithic arrays with fast, sparsified readout. The upgraded inner tracker of the ALICE experiment is based on such a technology [25]. A further improvement is the addition of a reverse bias voltage sufficient to deplete substantially the substrate, thus allowing a prompt charge collection. This in turn enhances the radiation hardness and improves the time resolution, making such depleted CMOS sensors competitive with standard hybrid pixel and strip detectors. Several R&D projects are presently active in this domain [26] and significant progress can be expected in the near future.

The impressive boost in computational power, combined with the increased complexity of CMOS technologies, drove the developments in CAD software. Large mixed-signal chips can be today assembled with automatic tools, reducing the time spent in error-prone handcrafted layout. New methodologies have been introduced that allow to verify large designs, thus increasing the chance of first working silicon. If the number of design revisions is reduced, more advanced processes can be afforded for similar project budgets. The complexity of tools has however increased as well, needing a higher specialization of the designers on the different design tasks. In the academia and in the research labs the potential of last generation CAD systems is often underused. It is therefore of primary importance that adequate investments are made to support training in the most advanced design methodologies. As more specialization is needed, it also necessary to guarantee in each project an adequate critical manpower, encouraging the cooperation between different design centers.

## References

[1] J. T. Walker, S. Parker, B. Hyams, and S. L. Shapiro. *Development of high density readout for silicon strip detectors.* Nucl. Instr. Meth. A226, pp. 200-203, 1984.

[2] W. Snoeys et al., *Integrated circuits for particle physics experiments.* IEEE JSSC, vol. 35, pp. 2018 - 2030, 2000.

[3] M. D. Rolo et al., *TOFPET ASIC for PET applications*, JINST 8, C02050, 2013.

[4] P. O'Connor et al., *Technology of the LSST focal plane*, Nucl. Instr. Meth. A582, pp. 902-909, 2007.

[5] M. Deveaux and J. M. Heuser, *The silicon detector systems of the Compressed Baryonic Matter experiment*, PoS (Vertex 2013) 009, 2013.

[6] T. Ambruster et al., *SPADIC - A self-triggered pulse amplification and digitization ASIC*, IEEE NSS-MIC Conference records, 2010.

[7] G. Mazza et al., *The ToPiX v4 prototype for the triggerless readout of the PANDA silicon pixel detector*, JINST, C01042, 2015.

[8] G. Degeronimo et al. *Front-End ASIC for a Liquid Argon TPC.* IEEE Trans. Nucl. Sci., vol. 58, pp. 1376-1385, 2011.

[9] H. Chen et al., *Readout electronics of the MicroBooNE LAr TPC, with CMOS front-end at 89 K.* JINST, C12004, 2012.

[10] J. P. Richter et al., *Development of a front end ASIC for Dark Matter directional detection with MIMAC.* Nucl. Instr. Meth. A620, pp. 470-476, 2010.

[11] L. Tibaldo et al., *TARGET: toward a solution for the readout electronics of the Cherenkov Telescope Array*, PoS(ICRC2015) 932.

[12] A. Dragone et al., *ePix: a class of architectures for second generation LCLS cameras*, Journal of Physics: Conference Series 493 (2014) 012012.

[13] L. Ratti et al., *PixFEL: developing a fine pitch, fast 2D X-ray imager for the next generation X-FELs*, Nucl. Instr. Meth. A796, pp. 2-7, 2015.

[14] G. E. Moore. Cramming more components onto integrated circuits.*Electronics*, 38:114, 1965.

[15] R. H. Dennard et al., *Design of ion-implanted MOSFET's with very small physical dimensions*, IEEE J.S.S.C, vol.SC-9, 1974.

[16] S. Natarajan et al., *A 14 nm Logic Technology Featuring 2$^{nd}$-Generation FinFET Transistors, Air-Gapped Interconnects, Self-Aligned Double Patterning and 0.0588 $\mu m^2$ SRAM cell size.* Proceedings of IEEE International Electron Device Meeting (IEDM), 2014.

[17] IBM news releases, *IBM Research Breakthrough Paves Way for Post-Silicon Future with Carbon Nanotube Electronics.* https://www-03.ibm.com/press/us/en/pressrelease/47767.wss.

[18] A. Marshall, *Thoughts on Possible Future Charge-Based Technologies for Nano-Electronics*, IEEE Trans. Circ. Syst. I, vol. 61, n. 11, pp. 3057-3065, 2014.

[19] B. Sedighi et al., *Analog Circuits Design Using Tunnel-FETs*, IEEE Trans. Circ. Syst., vol. 62, pp. 39-48, 2015.

[20] A. Pizzagalli et al., *3D technology applications market trends and key challenges.* Proceedings of 25$^{th}$ Annual Semiconductor Manufacturing Conference, Saratoga Springs, New York, 2014.

[21] *International Technology Roadmap for Semiconductors*, 2013 Edition.

[22] A. Rivetti *Fast front-end electronics for semiconductor tracking detectors: Trends and perspectives*, Nucl. Instr. Meth. A765, pp. 202-208, 2014.

[23] RD53 collaboration: http://rd53.web.cern.ch/RD53/

[24] V. Re, *Status and perspectives of pixel sensors based on 3D vertical integration*, Nucl. Instr. Meth., A765, pp. 47-52, 2014.

[25] M. Magner, *ALPIDE, the Monolithic Active Pixel Sensors for the ALICE ITS upgrade* Nucl. Instr. Meth., article in press.

[26] N. Wermes, *Depleted CMOS pixels for LHC proton-proton experiments*, Nucl. Instr. Meth., article in press.