PROCEEDINGS OF SCIENCE

DEPFET Pixel Detector for Belle II

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The Belle II detector is a general-purpose spectrometer which is being built at the asymmetric electron-positron collider SuperKEKB in Japan. The experiment aims at more precise measurement of the Standard Model contribution and overconstraining of the unitarity triangle in the B and D meson decays. The 2-layer active pixel detector based on the novel DEPFET technology is the innermost detector in the experiment and a part of the vertex detector which consists of pixel detector and double-sided silicon strip detector. The pixel detector provides excellent spacial resolution of around 10 µm and low material budget resulting in 0.21% X_0/layer. The detector is used to measure the precise position of the primary decay vertex. The energy loss in the detector may also be used for the identification of the incident particles. The working principle of the detector as well as the current development status are presented in the paper.

54th International Winter Meeting on Nuclear Physics
25-29 January 2016
Bormio, Italy

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PoS(BORMIO2016)029

1. Introduction

The Belle II is the detector constructed around the interaction point of the energy-asymmetric electron-positron collider SuperKEKB at KEK in Tsukuba, Japan. The experiment is an upgrade of the Belle experiment which was running from 1999 to 2010 and performed studies in the heavy-flavour sector on the data set of 1 ab^{-1}. The Belle II experiment aims to increase the data set by factor 40 by 2025 in order to refine the search for the New Physics and study the mechanism of the CP-violation.

The SuperKEKB accelerator will collide electrons at 7 GeV and positrons at 4 GeV around the 10.58 GeV center-of-mass energy. The asymmetric beam energies give Lorentz-boost to the B mesons which translates the time decay difference into a distance. The projected peak luminosity of $8 \cdot 10^{35}$ cm^{-2} s^{-1} will be achieved by utilization of the crab-cavities [1] which allow for high currents of 10 A and short bunch length of 3 mm, and the nano-beam scheme [2] which reduces the beam interaction cross-section.

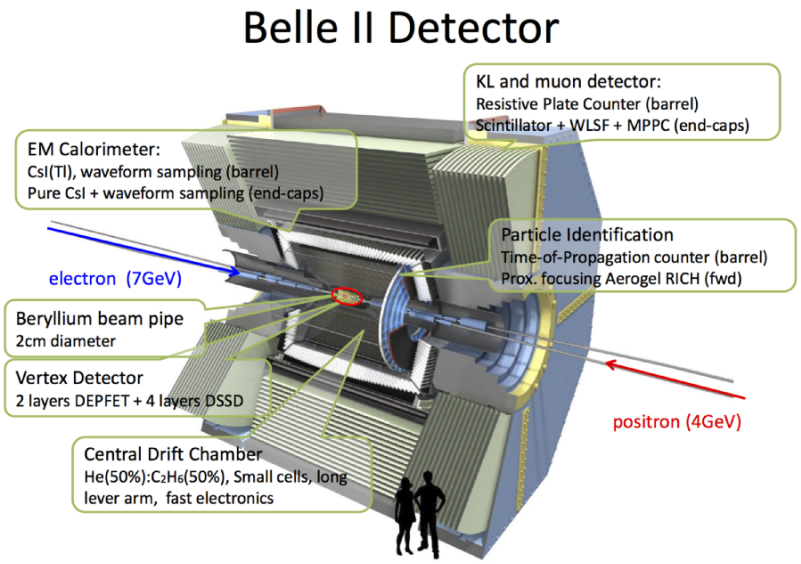

Figure 1: Cross-section of the Belle II spectrometer

The Belle II detector is a general-purpose solid-angle spectrometer installed inside of the superconducting solenoid coil that provides a 1.5 T magnetic field along the z-direction (parallel to the electron beam).

The innermost detector of the Belle II experiment is the vertex detector which consists of two layers DEPFET pixel detector and four layers double-sided silicon strip detector. The vertex detector is used to measure the precise position of the primary decay vertices.

The vertex detector is surrounded by the central drift chamber. The central drift chamber is a wire chamber which contains 14000 sense wires and is filled with 8000 l of the He (50%)/C_2H_6 (50%) gas mixture. The central drift chamber measures the trajectories, momenta and the energy loss of the particles and therefore is used in particle identification, tracking and triggering.

Two ring-imaging Cherenkov detectors which provide particle identification are installed around the central drift chamber. Barrel-shaped array of the Time-Of-Propagation counters reconstructs cones of Cherenkov light in quartz radiators. Aerogel-RICH reconstruct cones of Cherenkov light in the forward end-cap.

The RICH detectors are surrounded by the electromagnetic calorimeter built out of pure CsI crystals. The electromagnetic calorimeter measures the energy of the particles which is used by the trigger systems.

The iron flux-return structure is instrumented with the resistive-plate chambers to detect the long-lived kaons and muons.

2. Pixel Detector

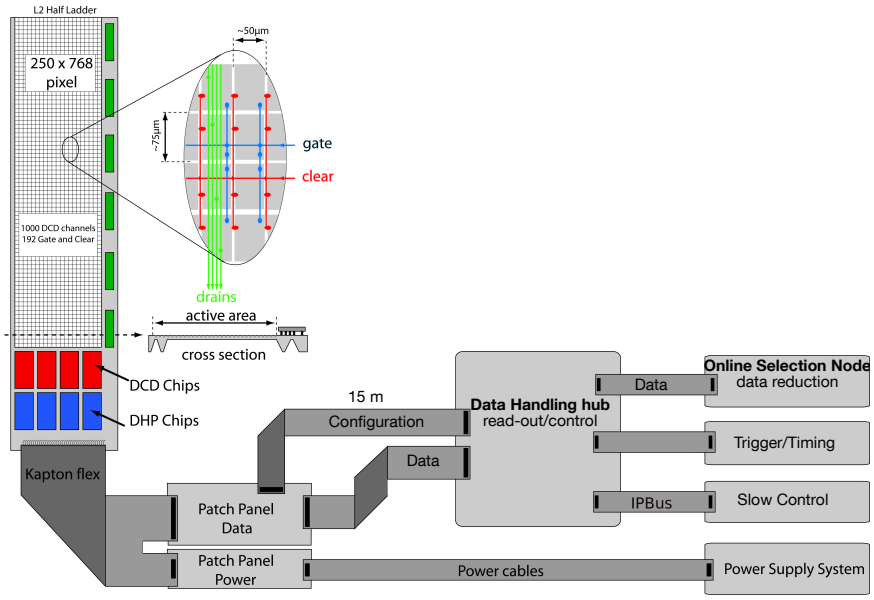

Figure 2: Schematic overview of the Belle II pixel detector

The schematic overview of the Belle II pixel detector unit is shown in fig. 2. The sensor module which carries the DEPFET matrix and front-end electronics is wire-bonded to the kapton flex. The kapton flex carries digital signals and power lines to the data/power patch panel installed in the "dock boxes" underneath of the central drift chamber end-caps. The patch panel provides connectors for the 15 m cables to the read-out system and to the power supply units, and 4-channel optical transmitters for the high-speed data links. The read-out system and power suppy units are installed on top of the spectrometer.

The challenges for constructing the pixel detector for the Belle II experiment are caused by its location and functions. The proximity to the interaction point of the accelerator causes high radiation damage and high background level mostly dominated by 2-photon process. As the innermost detector in the experiment, the pixel detector is required to have low material budget to prevent multiple scattering. Its function as a vertex detector requires excellent resolution and high signal-to-noise ratio. In the following chapter the technology of the pixel detector is described.

2.1 DEPFET Technology

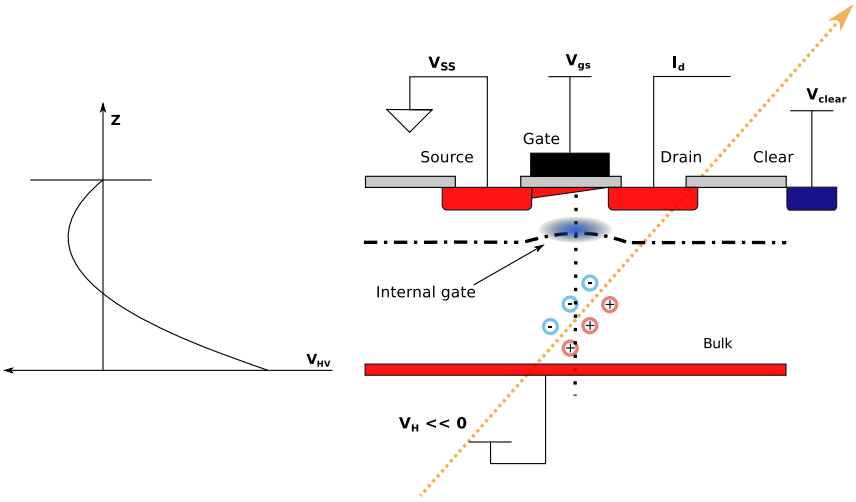

Figure 3: Principle of the particle detection by the DEPFET detector

The depleted P-channel field effect transistor (DEPFET) was invented by J. Kemmer and G. Lutz in 1987 [3]. The device is built upon a p-channel MOSFET integrated on top of the depleted Si bulk (fig. 3). The depletion is achieved by using the punch-through effect. The electrons are collected in the region beneath the gate of the MOSFET where a local minimum of the electric potential is created by n+ doping. This region is called the internal gate. The charge accumulated in the internal gate modulates the current through the MOSFET proportionally to the transconductance constant $g_q \approx 400\,\mathrm{pA/e^-}$. The low capacitance provides high signal-to-noise ratio of 40 for 75 µm thickness [4]. The read-out does not destroy the signal in the internal gate. After the measurement is finished, the charge is removed from the internal gate by raising the potential of the deep n+ contact, the clear contact, which becomes the most attractive potential for electrons.

The DEPFET technology shows high radiation tolerance. The electrons trapped in the silicon oxide layer contribute the most to the radiation damage. These electrons cause the shift in the threshold voltage which could be compensated by adjusting the operation voltages of the detector and in the front-end (e.g. dynamic offset subtraction in the ADC). The damage to the crystal structure of the bulk is found to be negligible [5].

2.1.1 Intrinsic Electronic Shutter

The injection frequency of SuperKEKB is 50 Hz. The newly injected bunches have high energy spread and therefore require significant time period (approx 20% of the injection cycle) to "cool down". In this time they induce high background through the intra-beam scattering (e.g Touschek effect) and damping on the beam pipe structure. Due to the rolling shutter read-out the charge collection cannot be stopped. The signal from the noisy hits would oversaturate the pixel detector and cause the data loss in the front-end.

To counteract the injection noise the intrinsic electronic shutter feature of the DEPFET is used. The detector can alter the electric field in the bulk to immediately remove the generated charge and simultaneously protect the electrons accumulated in the internal gate. Hence, the charge in the

internal gate is not distorted. This mode of operation is called gated mode. The gated mode is activated by raising the clear potential and turning off the gate potential of the MOSFET. The time required for the activation of the gated mode is around 1 µs.

2.2 Detector Module

The Belle II pixel detector is built out of 40 half ladder DEPFET modules. Two half ladders are glued in the middle to build a ladder. The ladders are arranged around the interaction point in two layers. The layer 1 is built with 8 ladders at the radius 14 mm. The layer 2 is built with 12 ladders at the radius 22 mm. The layout of the half ladder is shown in fig. 4.

The sensor matrix is bonded on the SOI [1] wafer and thinned to the thickness of 75 µm to reduce the material budget. The SOI wafer underneath of the matrix is etched and the remaining material builds a self-supporting structure with the thickness of 450 µm to gain mechanical stiffness. Additionally, rims are etched in the thick silicon to further reduce material budget. This brings the total material budget of the module to 0.21 X_0 [6].

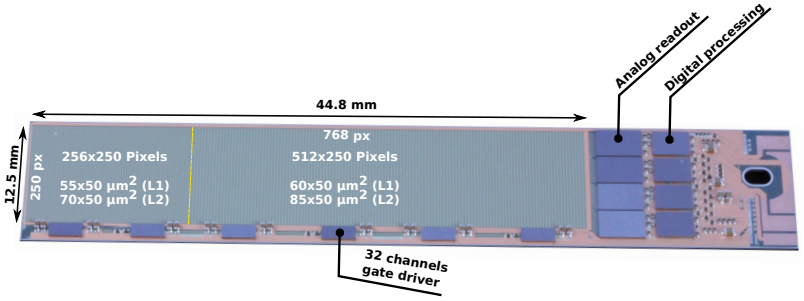

Figure 4: Belle II pixel detector module

The sensor matrix consists of 768x250 DEPFET pixels. The pixels are divided by size in two regions to preserve the consistent angular resolution. The inner region contains 256x250 pixels with the dimensions 55x50 µm^2 in the layer 1 and 70x50 µm^2 in the layer 2. The outer region contains 512x250 pixels with the dimensions 60x50 µm^2 in the layer 1 and 85x50 µm^2 in the layer 2. The prototypes with different thicknesses were produced. In the test beam the spacial resolution is measured at 10 µm for the thickness 50 µm [7].

2.3 Matrix Operation

The matrix is operated in the rolling shutter mode. The so-called four-fold read-out is used to reduce the integration time of the detector. Four rows of pixels share the same gate and clear lines and therefore are activated at once. This comes at the expense of the number of drain lines, because every pixel in these four rows is connected to a separate drain line. A drain line connects the drain of the MOSFET to the analog read-out (ADC) input and is shared between pixels in the different groups of the four pixel rows. Therefore, only one pixel attached to a drain line is active at any given time.

The typical DEPFET read-out cycle is shown in fig. 5. The cycle starts with the activation of the MOSFET gate. The current on the drain line starts to rise until it saturates on the plateau where

[1] Silicon-On-Insulator

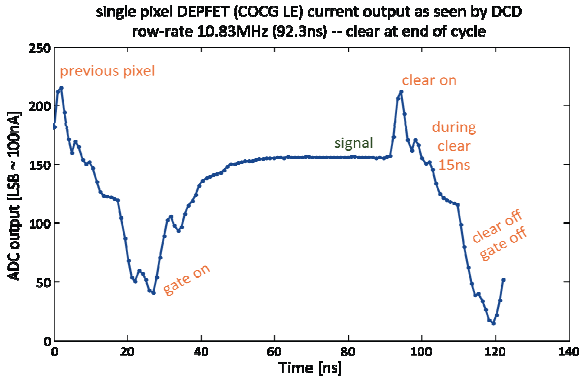

Figure 5: Drain current during DEPFET read-out cycle [8]

the signal is digitized by the ADC. The pixel is then cleared by switching on the clear voltage which causes the sharp rise and fall of the drain current to the minimum value. The next group of rows is activated and the cycle repeats. Since the steering sequence is subdivided in 32 steps, the duration of the cycle is 105 ns at the nominal clock frequency of 305 MHz. With 192 rows this adds to the matrix integration time of 20 µs.

The matrix operation is performed by three types of active electronic components which are bump-bonded on the silicon support structure. The steering ASICs[2] drive the gate and clear lines. The multi-channel ADCs perform digitization of the drain currents. The digital processors synchronize the matrix operation and transfer the signal to the read-out chain. The radiation hardness of the active components is ensured by using technologies proved to be radiation hard and design technics aimed at protecting the configuration and data memories (e.g. triple redundancy and error-correcting codes). Radiation campaigns has been performed to show the radiation hardness of the front-end ASICs.

2.3.1 Matrix Steering

The steering ASICs, called SwitcherB [9], can control up to 32 row groups. Six SwitcherB ASICs are connected in the daisy chain which builds a 192-bit shift register. The active bit in the chain defines the active group of rows. The control sequence is generated by the digital processor.

The SwitcherB is equipped with level-shifters which translates low-voltage control signals into high-voltage. The level-shifters can generate fast high-voltage (around 20 V) pulses to drive gate and clear lines.

2.3.2 Signal Digitization

The Drain Current Digitizer for Belle (DCDB) [10] is a 256-channel 8-bit ADC. The DCDB features the analog common-mode correction, the configurable current amplification and per-pixel dynamic pedestal compensation.

The ADC operates at 305 MHz with the sampling rate of 10 MS/s. Four DCDBs are installed on the module which brings the total data rate to 80 Gb/s per half ladder.

[2] Application Specific Integrated Circuit

2.3.3 Digital Data Processing

Four Data Handling Processors (DHP) [11] are interfaced to the DCDB on the module. The DHP generates the matrix steering sequence and synchronizes it to the signal digitization. The raw data from the DCDB are buffered in the memory of the DHP and processed only if the level-1 trigger is received. The DHP performs calculation of the common mode, subtraction of the pre-calculated pedestals and the data reduction by applying zero suppression with the configurable threshold. The data are then packaged into frames and sent to the read-out electronics over 1.6 Gb/s high-speed serial link. Due to the limited buffer memory and the bandwidth of the output link in the DHP, the average detector occupancy, which the DHP could tolerate without data loss, is limited by 3 %.

3. Data Read-out and Data Reduction

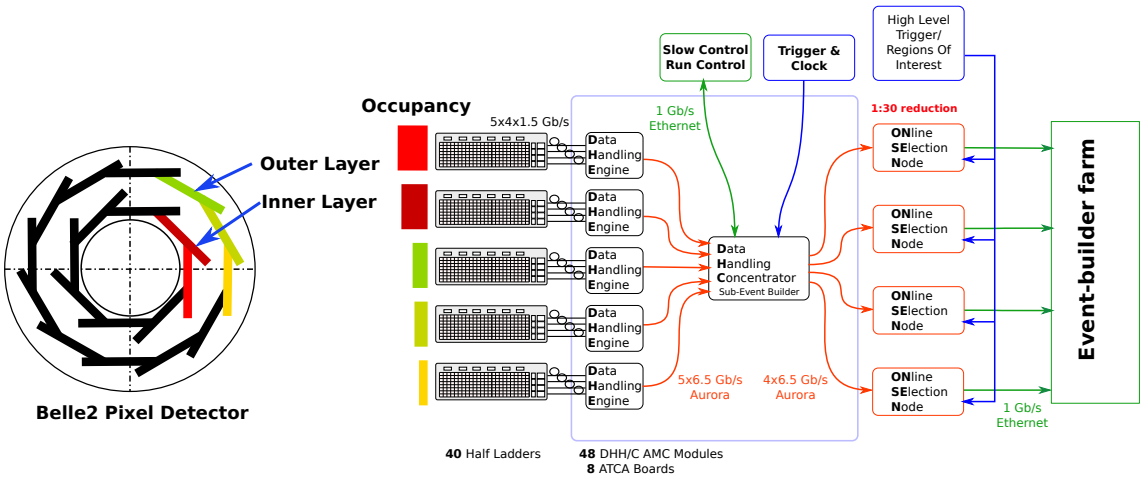

Figure 6: Data read-out chain of the Belle II pixel detector. The figure also shows the possible data rate averaging effect achieved by the sub-event builder algorithm. The effect appears if events from half ladders with different mean occupancy are combined.

The maximum data rate of the detector at 3 % occupancy level and 30 kHz trigger rate is estimated at 20 GB/s. The data rate is 10 times higher than the combined data rate of all other detectors in the experiment. This requires the special treatment of the data outside of the common Belle II data path. The data read-out system which performs the online data reduction has been developed.

The architecture of the data read-out system is shown in fig. 6. Each half ladder sends data over four high-speed serial links to the FPGA-based read-out boards, Data Handling Engine (DHE) [12]. The data from 5 half ladders are multiplexed on-line by the FPGA-based sub-event builder, Data Handling Concentrator (DHC). The sub-events are distributed to the Online Selection Nodes (ONSEN) [13]. The FPGA-based ONSEN system performs on-line data reduction based on the tracks reconstructed in the outer detectors.

3.1 Read-Out Electronics

The DHE provides configuration and control interfaces to the half ladder, as well as the receiver for data. The received data are buffered in the external memory and then processed by the FPGA. The data processing includes pixel re-mapping, cluster reconstruction and cluster analysis.

The cluster analysis analyzes the shape and energy distribution of a cluster to identify the low-energy ("slow") pions from D^* or $B\bar{B}$ decays. The slow pions do not reach outer detectors and therefore would be rejected by the data reduction system. The simulations show the efficiency of 95 % for identification of the slow pions with the p_t = 15-25 MeV with the background rejection of 90 % [14].

The data are then sent to the hardware sub-event builder DHC. The DHC combines events with the same event number from 5 half ladders to a single sub-event. The data rate averaging effect may be achieved during sub-event building if the events from different detector layers are combined (fig. 6). The sub-events are then distributed among online selection nodes.

3.2 Online Data Reduction

The online data reduction relies on the information available from the outer detectors. This information is received by the ONSEN system in form of Regions-Of-Interest (ROI). An ROI is calculated by extrapolation of the reconstructed particle tracks towards the intersection with the pixel detector planes. An ROI consists of coordinates which define a rectangular region in the coordinate system of the pixel detector.

The ONSEN system supports two exclusive algorithms for data reduction. The pixel-based algorithm retains all pixels inside an ROI. The cluster-based algorithm retains all clusters which intersect an ROI. The clusters marked as generated by slow pions bypass the data reduction algorithms without filtering.

The ROIs are generated by two independent systems. The high level trigger (HLT) performs reconstruction and extrapolation of the tracks in software on the full event data except for the pixel detector event. The HLT makes a decision whether the event should be kept and calculates the ROIs which are sent to the ONSEN system over Ethernet. The typical time budget for an event is around 1 ms. The expected reduction factor in the ONSEN system using HLT is 10. The HLT has been first tested at the beam test at DESY in January 2014,[15].

Another factor 3 in the data reduction is expected from the track reconstruction on the silicon strip detector data only. The tracks are reconstructed by the FPGA-based system Data Concentrator using Hough transform algorithm [16].

4. Performance at the Beam Tests

The prototypes of the pixel detector have been used for studying the properties of the detector at the beam tests at CERN and at DESY. The first two modules of the final Belle II design (fig.4), have been studied at the beam test at DESY in April 2016. The goal of the beam test is the integration of the data acquisition systems of the pixel and silicon strip detectors into the Belle II data acquition.

The setup at the beam test consists of one sector of the Belle II vertex detector: two layers of the pixel detector and four layers of the double-sided silicon strip detector. The sector of the vertex

detector is installed between 3rd and 4th planes of the AIDA telescope [17] which is used for efficiency studies. The vertex detector and the telescope are installed inside of the superconducting magnet PCMAG in the test beam area 24/1. The magnet can generate magnetic field of 1 T which is used to study the tracking performance. The data from the silicon strip detector planes were used as a source for the HLT.

During the beam test the pixel detector showed the signal-to-noise ration 33. The online data reduction worked stable at 2 kHz trigger rate on the beam. Off the beam the online data reduction worked stable at 8 kHz trigger rate. The more detailed analysis of the data is currently ongoing.

5. Conclusions

The pixel detector for Belle II experiment based on the DEPFET technology has been developed. The detector has been studied at various beam tests and optimized to fulfill the requirements of the experiment. The full sector of the vertex detector has been studied at the beam test at DESY in April 2016 where the concept of online data reduction has been confirmed. The final production of the detector modules is ongoing and will be finished by 2017. The vertex detector will be installed in Belle II in 2018.

6. Acknowledgements

The research leading to these results has received funding from the European Commission under the FP7 Research Infrastructures project AIDA, grant agreement no. 262025. This work is supported by the German Ministry of Education and Research, Excellence Cluster Universe and the Maier-Leibnitz-Laboratory.

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