

Physics performance with the new ATLAS Level-1 Topological trigger in Run 2

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The ATLAS trigger system aims at reducing the 40 MHz proton-proton collision event rate to a manageable event storage rate of 1 kHz, preserving events valuable for physics analysis. The Level-1 trigger is the first rate-reducing step in the ATLAS trigger system, with an output rate of 100 kHz and decision latency of less than 2.5 micro seconds. The Level-1 system is composed of the calorimeter trigger, muon trigger and central trigger processor. During the last upgrade, a new electronics element was introduced to Level-1: The Topological Processor System. The topological processor will make it possible to use detailed realtime information from the Level-1 calorimeter and muon triggers, processed in individual state of the art FPGA processors to determine angles between jets and/or leptons and calculate kinematic variables based on lists of selected/sorted objects. More than one hundred VHDL algorithms are producing trigger outputs to be incorporated into the central trigger processor decision. This information will be essential to improve background rejection and increase the significance of a large spectrum of ATLAS physics measurements. An overview of the firmware implementation, algorithms performance and their impact on physics results will be illustrated.

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1 1. Introduction

ATLAS [1] is one of the multi-purpose experiments at the Large Hadron Collider (LHC) at 2 the European Centre of Nuclear Research (CERN) in Switzerland. The LHC collides bunches 3 of opposing protons at a frequency of 40 MHz. The ATLAS Trigger system filters out collision 4 events of little physics interest, lowering the average output rate to a level of about 1 kHz. This is 5 achieved using a multi level trigger system. The fully hardware based Level-1 trigger uses muon 6 and calorimeter signals to determine "Regions of Interest" (RoI) and, based on counting clusters of 7 jets, tau, electron/ γ and missing E_T at various energy thresholds, reduces the event rate to about 100 8 kHz. The next stage High Level Trigger (HLT) is implemented in software. The HLT uses Level-1 9 RoIs to reconstruct detailed physics properties for a further rate reduction to approximately 1 kHz. 10 The ATLAS Level-1 Trigger is a fixed latency, 40 MHz, pipelined, synchronous system, built 11 to operate at the LHC design instantaneous luminosity of 10^{34} cm⁻²s⁻¹. The Level-1 trigger system 12 consists of three sub-systems: The Level-1 Calorimeter Trigger (L1Calo) [3], the Level-1 Muon 13 Trigger (L1Muon) [4], and the Central Trigger Processor (CTP) [5]. The hardware of the Level-1 14 Trigger is primarily based on field-programmable gate arrays (FPGAs). Including cabling, the max-15 imum latency budget of the Level-1 electronics chain is 2.5 μ s. A simplified outline of the Level-1 16 trigger is shown in Fig. 1. The L1Calo input data consists of 7200 analog "trigger towers". The trig-2014-2015 LHC collisions (40MHz, 6.5+6.5TeV, lumi>1034)



Figure 1: Integration of L1Topo into the ATLAS Level-1 trigger systems. Signals from the L1Calo upgraded merging modules as well as from the muon interface are fed into L1Topo where topological algorithms are applied. The results are sent to the Central Trigger Processor which sends the Level-1 accept of the event.

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ger towers are built with a granularity of 0.1×0.1 in the $\eta - \phi$ plane (ϕ being the azimuthal angle 18 around the beam axis and the pseudorapidity η is given by the polar angle θ as $\eta = -\ln \tan(\theta/2)$. 19 which is covered by the ATLAS electromagnetic and hadronic calorimeters. Digitization of the 20 input signals and digital filtering is done on a upgraded mixed-signal Pre-Processor. The trigger 21 tower signals are then forwarded to two feature processors, namely the Cluster Processor (CP) and 22 the Jet/Energy-sum Processor (JEP). The CP identifies electron, photon and tau candidates with a 23 transverse energy E_T above a set of configurable thresholds [6]. Simultaneously the JEP identifies 24 jet candidates and produces global sums of total, missing, and jet-sum E_T . The L1Muon input data 25 comes from Resistive Plate Chamber (RPC) strips in the barrel region and Thin Gap Chambers 26

(TGCs) in the endcap regions. Multiplicities for different thresholds at high and low transverse
momentum are measured by coincident hits in the RPC and TGC planes. Both the L1Calo and

²⁹ L1Muon triggers are only based on multiplicity of different thresholds.

In order to cope with the increased luminosity and the higher collision energy expected from 30 2015 onwards, the Level-1 Topological Processor (L1Topo) was installed during the first long shut-31 down phase. The central idea is to have topological information of different particles all available 32 on one module to apply topological algorithms at the first trigger stage. These triggers facilitate 33 the reduction of trigger rates while keeping E_T thresholds low. To provide input for L1Topo, mul-34 tiple new modules were installed. The new merger modules [7] sort and forward the L1Calo data 35 from JEP and CP. In the muon system the new muon interface [8] sends information about muon 36 candidates to the topological processor. L1Topo can therefore apply topological algorithms on 37 electron/ γ , tau, jets, energy sums and muon particle candidates. 38

The final trigger decision is made in the Central Trigger Processor (CTP), which receives input about particle multiplicities from the CMX modules as well as from the MUCTPI and the decision bits of all algorithms from L1Topo.

42 2. L1Topo Hardware

The L1Topo system must be able to process about 1 Tb/s of input data in only ~150ns. To meet the low latency requirements, PCBs with three state of the art FPGAs per module have been built. Two Xilinx Virtex7 XC7V690T FPGAs (processor FPGAs) are used to provide the resources of 433200 lookup tables and 3600 digital signal processing slices (DSPs) per FPGA for the topological algorithms. The third one (Kintex 7) is a control FPGA and contains all communication logic for interfacing to exterior systems. The Kintex 7 handles the readout and facilitates configuration of the processor FPGAs via IPBus.

The large amount of data processed by the system is received on 160 optical fibers per module. These signals are then converted to electrical signals via Avago miniPODs and then fed into a processor FPGA's multi gigabit transceivers (MGT). The realtime output, which consists only of algorithm decision bits (32 per FPGA), is directly transferred to the CTP where the final trigger decision is made.

⁵⁵ Currently two of these modules are installed in order to provide ressources for running more ⁵⁶ than 100 topological algorithms in parallel.

57 3. Relatime Data Path Firmware Structure

58 3.1 Receipt and Deserialization

Each processor FPGA receives serial data on 80 links at a rate of 6.4 Gbit/s. The data are first deserialized and 8b/10b decoded using internal MGTs to get 32 bit words in the 160MHz clock domain. In a next step these words are further deserialized to obtain the 128 bit words that contain the information of exactly one event. To provide stable data transfer in a scenario where all upstream systems may have different response times configurable delays in multiples of the 160MHz subticks are applied in the deserialisation process by using shift registers. ⁶⁵ The 128 bit words can contain differing amounts of Trigger OBjects (TOBs). On each fiber 4 ⁶⁶ jet TOBs, 5 cluster (Em/ γ /Tau) TOBs, 16 muon TOBs or energy sum information can be received ⁶⁷ resulting in a total of 64 Jet TOBs, 120 Em/ γ TOBs, 120 tau TOBs, 32 muon TOBs and one ⁶⁸ missing energy TOB. These TOB words are then decoded to obtain the angular values (η , Φ) and ⁶⁹ the transverse energy E_T . These lists of TOBs are then fed into the topological algorithms.

70 3.2 Algorithm Structure

The topological algorithms often combine all the elements of one TOB type with another. Due to the large amount of input data and combinatorics inside the algorithms, the amount of resources required would allow only a very low number of algorithms. To mitigate this the TOB lists of the different types are shortened in a first stage and then fed into the actual topological decision algorithms (see Fig. 2).



Figure 2: General algorithm structure

The timing constraint for the algorithms is currently given as three LHC bunch ticks (3×25 ns). The first two of them are used for the mentioned data reduction. This can be done in two different ways. In a sort algorithm the TOBs are sorted by their E_T value resulting in a sorted list of 6 TOBs. If there are more TOBs, an overflow bit is set. The alternative is a selection algorithm that applies an E_T cut and provides an output list of 10 TOBs. The length of these output lists is mainly limited by the logic delay of these algorithms.

During the third bunch tick the topological decision algorithms are applied on the shortened TOB lists. Their output consists of a decision and an overflow bit. In the realtime data path the overflow sets the decision to true so the high level trigger will rerun the algorithm. The decision bits are then sent directly to the CTP.

4. Physics Triggers with L1Topo

L1Topo triggers have various use cases in the fields of Standard Model, Higgs and B-Physics
 measurements, searches of Supersymmetry and Exotic particles, as well as for detector calibration
 (e.g. with J/Ψ, W Tag-and-Probe or for Liquid Argon Calorimeter tests).

Physics triggers (see Fig.3), including cuts on the invariant mass between jets (vector boson fusion), scalar sum of jet E_T (Susy, Exotics), $\Delta R = \sqrt{(\Delta \eta)^2 + (\Delta \phi)^2}$ between muons (B-Physics),

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Figure 3: Examples of topological quantities: angular distributions, hardness of the interaction or sums of energy or momenta and invariant mass

⁹² $\Delta\Phi$ between two leading jets and missing E_T above a given threshold (Higgs), require the imple-⁹³ mentation of many different algorithms.

For this about 15 different categories of decision algorithms were implemented. Simple angular cuts, but also cuts on the transverse or invariant mass, can be applied. In addition there are disambiguation algorithms, TOBs can be matched or multiplicities can be calculated. The missing energy can be corrected using information from jets and energy ratios can be determined. To maximise algorithm composition flexibility the FPGAs can be easily reconfigured and new algorithms

⁹⁹ can be added in future trigger menu configurations.

100 5. Conclusion

L1Topo for the first time makes it possible to perform topological selections as part of the first trigger stage within ATLAS using inputs from the calorimeters and the muon sub-detectors. This allows the trigger system to maintain efficiency without having to raise E_T and p_T thresholds in the existing multiplicity triggers. The system is being commissioned in ATLAS data taking runs throughout 2015 and 2016, with new triggers validated and enabled as the luminosity increases.

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