# PoS

## The Level-1 Calorimeter Global Feature Extractor (gFEX) Boosted Object Trigger for the Phase-I Upgrade of the ATLAS Experiment

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The Global Feature Extractor (gFEX) module is a planned component of the Level 1 online trigger system for the ATLAS experiment planned for installation during the Phase-I upgrade in 2018. This unique single electronics board with multiple high speed processors will receive coarsegranularity information from all the ATLAS calorimeters enabling the identification in real time of large-radius jets for capturing Lorentz-boosted objects such as top quarks, Higgs, and W/Zbosons. The gFEX architecture also facilitates the calculation of global event variables such as missing transverse energy, centrality for heavy ion collisions, and event-by-event pile-up energy density. Details of the electronics architecture that provides these capabilities are presented, along with results of tests of the prototype systems now available. The status of the firmware algorithm design and implementation as well as monitoring capabilities are also presented.

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#### 1. Introduction

The Global Feature Extractor (gFEX) is one of several electronics modules designed for the Phase-I upgrade in 2018 [1–3] of the online event selection and processing system, or *trigger system*, in the ATLAS Experiment [4]. The gFEX module is designed to extract information from the entire calorimeter for processing within a single printed circuit board. This scheme enables the use of global event information for identification and selection of events in real-time, therefore significantly extending the online trigger capabilities of the ATLAS Experiment, and thus also its physics potential.

Of particular importance for the design of the gFEX is the identification of Lorentz-boosted hadronic objects that are characteristic of several new physics scenarios. At high transverse momentum, the hadronic decay products of energetic bosons and top quarks tend to be highly collimated. Using large-radius jets to capture these decay products in a single trigger object and exploiting the internal two/three-prong structure of these jets yields enhanced signal-to-background discrimination. The gFEX reconstructs these large-radius jets to efficiently identify boosted objects while maintaining a suitable rate in the expected environment of the Large Hadron Collider after the Phase-I upgrade in 2018. Additionally, the gFEX allows for subtraction of energy deposits from multiple simultaneous proton-proton collisions, or *pile-up*, and supports several different methods for the calculation of missing transverse momentum ( $E_T^{miss}$ ) that will enable flexibility for  $E_T^{miss}$  algorithms at in the first level of the trigger system.

#### 2. Electronics architecture

The special feature of the gFEX is that it receives data from the entire calorimeter enabling the identification of large-radius jets and the calculation of whole-event observables [5]. To perform these functions with a single module, the gFEX must handle the output bandwidth of the entire calorimeter. Due to constraints on the specifications for the Phase-I upgrade electronics, the gFEX module is able to accommodate 4 field-programmable gate array (FPGA) integrated circuits, where each FPGA has  $\mathcal{O}(100)$  high-speed communication links. While this is similar in scale to other Phase-I L1Calo electronics, those boards use many of the high-speed links for intra-FPGA communications as opposed to off-board transmission. The gFEX organizes data sharing between FPGAs differently from these other boards instead putting a premium on maximizing the number of optical fibers carrying the calorimeter output.

The current design of the gFEX utilizes three large processor FPGAs (pFPGA) for data processing and a combined FPGA and CPU Multi-Processor System-on-Chip (MPSoC) for control and monitoring. Each pFPGA has  $2\pi$  azimuthal coverage for a given range in  $\eta$  and executes all feature identification algorithms. As shown in Fig. 1, the pFPGAs communicate with each other via low-latency General Purpose I/O (GPIO) links while input and output to the board are via Multi-Gigabit Transceivers (MGT). The pFPGAs communicate with the Xilinx Zynq MPSoC via both MGT and GPIO links. The baseline speed for the communication links between the calorimeter electronics and gFEX is 11.2 Gb/s, and thus the MGTs are commissioned to operate at this bandwidth (see Section 4 for more information). Each pFPGA processes calorimeter tower data in  $\Delta \eta \times \Delta \phi = 0.2 \times 0.2$  units from a range in  $\eta$ : pFPGAs #1 and #2 correspond to negative and positive  $\eta = 0 - 2.5$ , respectively, and pFPGA #3 corresponds to  $|\eta| = 2.5 - 4.9$ . These pFPGAs transmit data to other electronics modules within the trigger system (e.g. the Level 1 Topological Processor [6], or L1Topo, and the Front-End Link EXchange [7], FELIX) as well as to the on-board MPSoC for real-time monitoring and analysis. Upon receiving calorimeter data, the pFPGAs are responsible for executing jet reconstruction algorithms, computing pile-up energy densities for the event, and transmitting the results to L1Topo.



(a) gFEX Block diagram

(b) gFEX prototype FPGA communication

**Figure 1:** (a) A block diagram of the gFEX module. Shown are the real-time (to Level 1 Topological Processor (L1Topo)) and readout data paths (to Front-End Link EXchange (FELIX)). (b) Illustration of FPGA connections for the gFEX module with the Zynq Multi-Processor System-on-Chip (MPSoC).

#### 3. Algorithm design and implementation

To capture the decay products of a boosted top quark, such as shown in Figure 2(a), largeradius jet reconstruction with  $R \approx 1.0$  (shown as the black circle) is necessary, as opposed to jets in the current system which use  $R \approx 0.4$  (shown as the red circle). The gFEX pFPGAs execute a seeded simple-cone jet algorithm for the large-area non-iterative jet finding. The tower transverse energy,  $E_{\rm T}$ , in an approximately "circular" region surrounding local maxima (computed in  $3 \times 3$ tower blocks) is summed as illustrated in Fig. 2. Portions of the jet area can extend into an  $\eta$  region on a neighboring pFPGA, necessitating the transfer of information between pFPGAs. These partial sums are sent to the original pFPGA and are included in the final  $E_{\rm T}$  of the jets as in Fig. 2(b).

In addition to jet reconstruction, the transverse energy density  $\rho$  is calculated in each pFPGA region on an event-by-event basis using the average  $E_T$  of all towers below a given  $E_T$  threshold. This density is subtracted from each jet using the area of each jet and  $\rho$  from the associated region.

#### 4. Prototype system tests and early results

Two prototype versions of the gFEX are currently under test. The primary differences with respect to the design presented in Section 2 are that the first prototype version has one Xilinx Virtex-Ultrascale FPGA, while the second version has three Xilinx Virtex-Ultrascale FPGAs (see Fig. 3), and both versions use an older Zynq SoC than the design specification with an MPSoC. Both prototype versions have undergone extensive high-speed communications link tests with several





**Figure 2:** (a) Fully-simulated large-radius jet from a top quark produced at high transverse momentum [8]. Subjets of a particular category have the same fill color and their extent represents the subjet active catchment area. Jet constituents are shown as black dots. The red circle represents current trigger capabilities, whereas the black circle represents the triggers provided by the gFEX. (b) Illustration of a few potential large-radius jets in the same event. Note that jets are allowed to overlap.

bandwidth configurations. The single pFPGA prototype was tested at 9.6 Gb/s, 11.2 Gb/s and 12.8 Gb/s [3], whereas the triple pFPGA prototype was tested at 9.6 Gb/s, 11.2 Gb/s and 12.8 Gb/s with all external interfaces, and at 25.6 Gb/s for inter-FPGA links. The tests were successful, with a Bit Error Ratio (BER)  $< 10^{-15}$ . Firmware and software integration is currently ongoing, including the deployment of a Linux operating system on the Zynq SoC for on-board monitoring, slow control, and testing.

#### 5. Conclusions

The production, testing, and integration of electronics and firmware is progressing well for the gFEX electronics module for the Phase-I upgrade in 2018 of the online event selection and processing system in the ATLAS Experiment. Prototypes of the new gFEX module have demonstrated performance at multiple bandwidth configurations for the high-speed communication links and are currently undergoing hardware, firmware and software integration tests and commissioning with other electronics modules in the ATLAS detector.

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Figure 3: gFEX prototype version 2.

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