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Upgrade of the CMS Tracker for the High Luminosity LHC

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The LHC machine is planning an upgrade program which will smoothly bring the luminosity to about 5×10^{34}cm^{-2}s^{-1} in 2028, possibly reaching an integrated luminosity of 3000 fb^{-1} by the end of 2037. This High Luminosity LHC scenario, HL-LHC, will require a preparation program of the LHC detectors known as Phase-2 Upgrade. The current CMS Tracker, including both inner pixel and outer strip systems, is already running beyond design specifications and will not be able to survive HL-LHC radiation conditions. CMS will need a completely new device in order to fully exploit the demanding operating conditions and the delivered luminosity. The upgrade plan includes extending the Pixel Detector in the forward region from the current coverage of $|\eta| < 2.4$ to $|\eta| < 4$, where up to seven forward- and four extension disks will compose the new detector. Additionally, the new outer system should also have trigger capabilities. To achieve such goals, R&D activities are ongoing to explore options and develop solutions that would allow including tracking information at Level-1. The design choices for the CMS Tracker upgrades are discussed along with some highlights of the R&D activities.

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1. Introduction & Requirements

The Large Hadron Collider (LHC) at CERN is scheduled to undergo a major luminosity upgrade around the year 2025 with the goal to deliver additional 3000 fb^{-1} to the experiments in the decade after 2026. This so-called High Luminosity LHC [1] will present extraordinary challenges to the tracking systems of the experiments in terms of radiation tolerance and performance. The expected instantaneous luminosity of 5×10^{34} $cm^{-2}s^{-1}$ translates into fluences of up to 2×10^{16} 1MeV n_{eq} cm^{-2} for the innermost regions of the Pixel Detector of CMS (Figure 1) and to a pile-up of 200 proton-proton collisions per LHC bunch crossing.

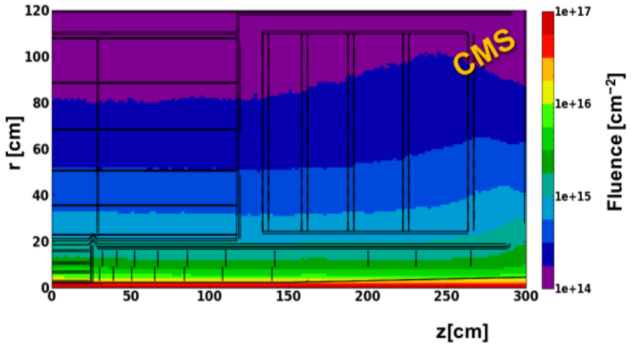

Figure 1: Simulation of the expected fluence in 1 MeV n_{eq} cm^{-2} for one quadrant of the CMS Tracker as function of the radial (r) distance from the interaction point and along the beam-axis (z) in the High-Luminosity LHC scenario.

Since the present CMS Tracker was designed for a target integrated luminosity of 300 fb^{-1} and a maximum pile-up of about 50, the complete Tracker will have to be replaced for the HL-LHC era. This is referred to as Phase-2 Upgrade. The new system will have to withstand ten times the radiation dose of the present one and will require increased granularity to ensure low occupancy in the order of 1% and robust tracking in the expected high pile-up conditions. At the same time, this pile-up will require the Tracker to provide information about high transverse momentum (p_T) tracks to the Level-1 Trigger at every bunch-crossing in order to improve the trigger system's discriminating power and output rate. However, this requires the front-end buffers of all on-detector electronics to be significantly deeper than in the present system since the Level-1 trigger latency will increase from 3.2 µs to 12.4 µs. At the same time the collaboration is aiming to reduce the material budget of the Tracker for better tracking performance and improved momentum resolution, as well as extending the acceptance from a pseudorapidity of $\eta = 2.4$ to $\eta \approx 4$, which enables the use of the particle-flow concept in the deep forward region.

2. Geometry

In order to meet the requirements of low material budget, extended acceptance, p_T discriminating power and full coverage, CMS is studying several different layouts for the Tracker. One such layout is shown in Figure 2. It features a large pixel detector with four barrel layers and seven forward disks plus an additional four extension disks, which ensure coverage up to $\eta = 4$. Furthermore, the four extension disks extend to a radius of 30 cm from the beam axis, which is necessary

to allow the installation and removal of the pixel detector with the beam-pipe in place. The part at radii larger than 20 cm (30 cm for $|z| > 150$ cm) is referred to as outer tracker. It features six barrel layers and five end-cap disks that use two different types of modules. The three inner barrel layers and parts of the end-caps use so-called PS modules that provide an accurate measurement of the z-coordinate, whereas the outer layers are built from "2S modules" with cruder z-granularity. These two types of modules and their p_{T} discriminating features will be described in more detail in Section 4. A large part of the barrel-PS modules are tilted to face the interaction point which mitigates inefficiencies in the p_{T} discriminating power that a flat barrel layout [2] implies and reduces the number of modules required for hermetic coverage.

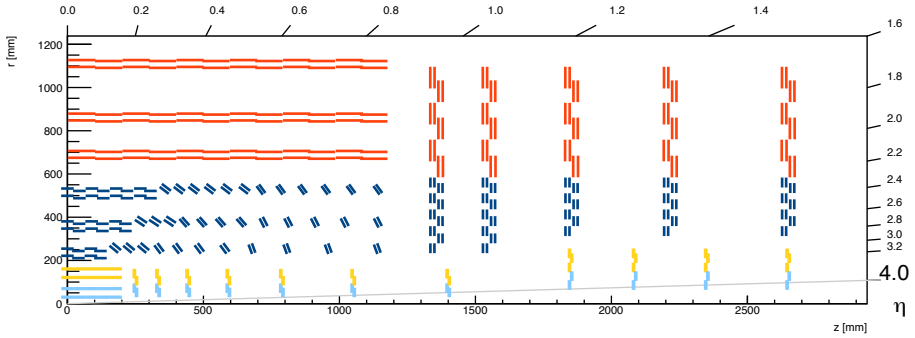

Figure 2: Possible layout of the upgraded CMS Tracker generated with [3]. The pixel system consists of four barrel layers, seven forward- and four large extension disks. The Outer Tracker consists of six barrel layers and five end-cap disks. The three inner layers of the barrel and the inner part of the disks feature so-called PS modules that provide an accurate measurement of the z-coordinate.

First estimations of the material budget based on the layout in Figure 2 and realistic models of the detector modules show that the new detector will be a factor of two lighter than the present CMS Tracker and have a more uniform material distribution along η.

3. Pixel Detector

The requirements imposed by the High-Luminosity LHC on the pixel detector are extremely challenging, both in terms of radiation tolerance and capabilities. The expected pile-up requires high granularity read-out chips and small pixel sizes, while the longer Level-1 latency requires deep buffers able to store the data generated by the expected hit rates of up to 3 GHz cm^{-2}. Furthermore, thin sensors, required for radiation tolerance, generate low signals which requires low detection thresholds and excellent noise characteristics of the read-out chip. In order to meet these challenges, CMS and ATLAS have formed the RD53 collaboration to develop a suitable read-out chip (ROC) in 65 nm CMOS technology for their future pixel detectors. The chip will feature a unit cell size of 2500 µm^2 and will be mostly digital with the analog circuits embedded in the pixel matrix [4]. The pixel sensors will have to withstand an integrated equivalent fluence of 10^{16} 1MeV n_{eq} cm^{-2}, which is half of the value expected for the innermost layer (Section 1) – which is possible since the design of CMS allows for the replacement of the pixel detector during an extended year-end techincal stop without removing the beam pipe (Section 2). The technologies under study are thin n-on-p planar devices and 3D detectors for the innermost layer, which have

both shown excellent radiation hardness during previous R&D campaigns carried out by CMS and ATLAS [5]. Only two types of modules are planned for the pixel system: small 1×2 chip modules for the inner barrel layers and the inner rings of the forward disks and 2×2 chip modules for the outer regions. The modules are designed to consume as little power as possible, and to further reduce the material budget for the services, a serial powering scheme is under development. The read-out will be done via low-mass electrical links that transmit the signals to a low-power optical transceiver mounted on the service structure.

4. Outer Tracker

The future Outer Tracker of CMS is designed to provide high p_{T}-track data to the Level-1 trigger as this information can be used to identify interesting events. Since transmitting the full tracker data at the bunch crossing frequency of 40 MHz would require very high bandwidth which comes with a mass- and power penalty, a new type of modules is developed that is capable of filtering out signals from tracks above a certain p_{T} threshold at the level of the front-end electronics. Such modules are referred to as p_{T} modules [6]. Applying a momentum cut of 2 GeV/c corresponds to a data-volume reduction by a factor of about 10. The modules are implemented by means of two closely spaced sensors that are connected to the same set of ASICs which are able to correlate the hits measured on the two sensors. Combinations of two hits that are compatible with a high transverse momentum track are referred to as "stubs" and the principle is illustrated in Figure 3. The data flow is such that only the stub information is transmitted to the back-end and subsequently the Level-1 trigger at 40 MHz. Only if an event is selected by the global trigger, the full hit data is read out and transmitted to the DAQ system as is the case in the present CMS Tracker.

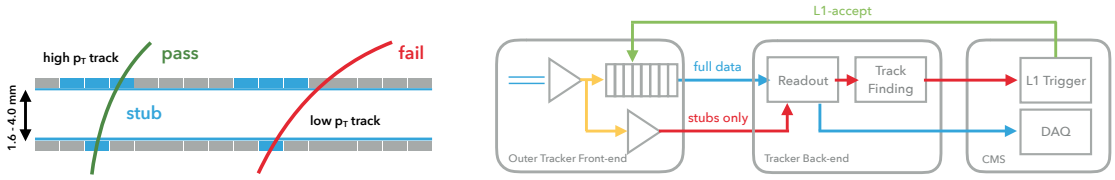

Figure 3: The p_{T} module concept and data-flow diagram for the two different read-out paths required for providing Tracker information to the Level-1 trigger. The path indicated in red transmits stub data at the LHC bunch-crossing frequency of 40 MHz whereas the path indicated in blue will not exceed the specified Level-1 trigger rate of 750 kHz.

The p_{T} module concept requires that the strips in both layers of a module are parallel to the z-axis. For that reason it is not possible to use strips tilted by a stereo-angle to measure the z-coordinate. The three outer barrel layers and the outer sections of the forward disks (compare Figure 2) will be built of so-called 2S (2 strip sensor) modules with an active area of about 10×10 cm^2. Two columns of 5 cm-long strips with a pitch of 90 µm are read out by individual front-end hybrids. In the inner layers PS (pixel-strip sensor) modules will be used that feature one strip sensor with strips of 2.3 cm length and one macro-pixel sensor with 1.44 mm long pixels. These ensure a precise measurement of the z-coordinate in the inner layers. Figure 4 illustrates the two types of modules.

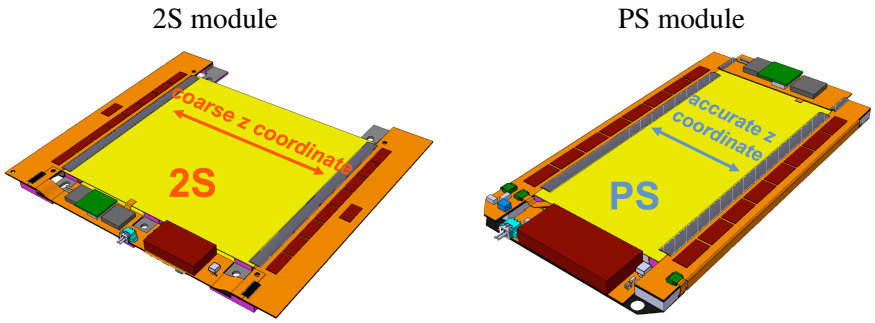

Figure 4: The two types of p_T discriminating modules designed for the CMS Outer Tracker.

Both module types will use sensors with about 200 µm active thickness made from n-on-p silicon since these proved to cope best with the expected fluences during a previous R&D campaign [5]. Custom ASICs are being developed for the specific application on the 2S and PS modules.

2S modules will be read out by the CMS Binary Chip [7], a circuit implemented in a 130 nm CMOS process that includes the stub finding logic necessary for the p_T discrimination feature.

PS modules require two dedicated ASICs for the two kinds of sensors. The strips will be read out by the Short-Strip ASIC (SSA) that does not have many features beyond the analog front-end and hit-detection logic. The stub-finding logic will be included in the Macro-Pixel ASIC (MPA) [8] that will read out the pixelated sensor. Both chips are implemented in a 65 nm CMOS process for radiation tolerance.

Common to both types of modules is a concentrator chip (CIC) that re-formats the data collected from eight CBCs or MPAs[1] and block-synchronously transmits the stub data via a low-power optical link. The read-out data for each received Level-1 trigger is included in the CIC data frame.

5. Level-1 Tracking

As described in Section 4, providing tracks for the Level-1 trigger at the LHC bunch-crossing frequency is challenging and unfeasible unless the data volume can be reduced at the detector front-end. By exploiting the fact that only 3% of tracks in CMS have a p_T above 2 GeV/c, the data that needs to be transmitted to the Level-1 trigger can be reduced by a factor of ten by using the p_T module concept. However, given the finite speed of optical links and the time overhead for the global Level-1 trigger, only about four microseconds remain from the total design latency of 12.4 µs for the actual track reconstruction. In order to tackle this challenge, CMS is currently investigating three different concepts (Figure 5):

Pattern recognition using associative memory: This concept exploits content-addressable memory (CAM) for pattern recognition. Custom-made ASICs store pre-loaded patterns that correspond to possible tracks. Once a series of stubs matches one of the patterns, the stubs are selected and forwarded to a track fitting stage implemented in an FPGA [9].

[1] The SSA data is sent to the MPA

Time Multiplexed Trigger: This concept uses a concept where data from a single LHC bunch-crossing is processed by a single processing node. This requires a formatting and ordering stage before the track-finding stage with a switching network in between. The track finding is done via a Hough Transform implemented in an FPGA where parameters of all straight lines compatible with each individual stub are filled into a 2D histogram. The point where these lines intersect is the most likely track candidate [10].

Tracklet extrapolation: The third approach uses a conventional tracking algorithm implemented in FPGAs where *Tracklets* are formed from stubs in a number of seed layers that are then extrapolated to other layers and further stubs are added, if they fall into a search window compatible with the tracklet parameters [11].

The associative memory and tracklet approach both search for patterns in a 3-dimensional parameter space whereas the time-multiplexed architecture first searches for tracks in the $r-\phi$ plane and then checks the candidate's z-coordinates for consistency. Track candidates (sets of stubs) obtained by the three approaches have then to be fitted in FPGAs and duplicates removed.

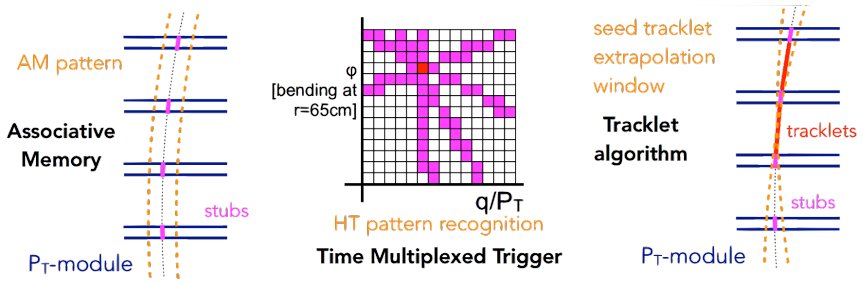

Figure 5: Overview over the different approaches under study for track reconstruction for the Level-1 Trigger in CMS.

6. Summary

The LHC is scheduled to undergo a major upgrade around the year 2025 with the goal to deliver additional 3000 fb^{-1} to the experiments in the following decade. This has severe implications for the tracking systems of the experiments as it means much harsher radiation environments and higher pile-up. Since the present CMS Tracker will not be able to operate under these conditions, it will have to be completely replaced with a new system. The Tracker Collaboration is working on the design and specification of a new Tracker that will be able to cope with the requirements.

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