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# Results of FE65-P2 Pixel Readout Test Chip for High Luminosity LHC Upgrades

**R. Carney, K. Dunne, M. Garcia-Sciveres*, D. Gnani, T. Heim, V. Wallangen**
*Lawrence Berkeley National Lab., Berkeley, USA*
*e-mail:* mgarcia-sciveres@lbl.gov

**A. Mekkaoui**
*Fermilab, Batavia, USA*

**T. Hemperek, H. Krüger**
*Bonn University Institute for Physics, Bonn, Germany*

A pixel readout test chip called FE65-P2 has been fabricated on 65 nm CMOS technology. FE65-P2 contains a matrix of 64 x 64 pixels on 50 micron by 50 micron pitch, designed to read out a bump bonded sensor. The goals of FE65-P2 are to demonstrate excellent analog performance isolated from digital activity well enough to achieve 500 electron stable threshold, be radiation hard to at least 500 Mrad, and prove the novel concept of isolated analog front ends embedded in a flat digital design, dubbed "analog islands in a digital sea". Experience from FE65-P2 and hybrid assemblies will be applied to the design for a large format readout chip, called RD53A, to be produced in a wafer run in early 2017 by the RD53 collaboration. We review the case for 65 nm technology and report on threshold stability test results for the FE65-P2.

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*Speaker.





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## 1. Introduction

A pixel readout test chip called FE65-P2 has been fabricated on 65 nm CMOS technology and tested without bump bonded sensors. FE65-P2 contains a matrix of 64 x 64 pixels on 50 $\mu$m by 50 $\mu$m pitch, designed to read a bump bonded sensor. It contains 8 column flavors of 8 columns each, for testing design variants such as leakage current compensation or increased PMOS width for higher radiation tolerance. FE65-P2 is about 4 mm x 3 mm and was produced in a multi-project run. It prototypes design elements of the RD53 [1] Collaboration's development of a large format demonstrator pixel readout chip for ATLAS and CMS upgrades for the High Luminosity Large Hadron Collider (HL-LHC). This demonstrator is called RD53A and follows detailed specifications documented in [2]. In this note, we review the motivation for the choice of 65 nm technology and report test results of FE65-P2 threshold stability vs. temperature and radiation.

Uniform response of all pixels is critical for pixel detector operation. Spatial uniformity is mainly achieved though individually trimming the charge threshold of each pixel, a process known as tuning. A pixel produces a signal only when the collected sensor charge exceeds a programmed threshold. Stable response vs. time is not addressed by tuning. Gradual threshold drift is mitigated by periodic tuning, but it is only feasible to tune the detector in long enough gaps between data runs. A pixel chip design must therefore be robust against changes in temperature and radiation dose in order for the response to remain stable during at least one run. This becomes more challenging as collider intensity increases: the radiation dose expected during a single run at the HL-LHC will approach 1 Mrad for the innermost pixel layer. Operation at lower threshold, as required for thin and heavily irradiated sensors with small pixels, also makes stability more challenging.

## 2. 65 nm Technology for High Rate and Radiation Readout Chips

The pixel detectors in the ATLAS and CMS experiments operate in triggered readout mode and will continue to do so at the HL-LHC [4][5]. This means that all hits must be time stamped and stored during a trigger latency period of order 10 µs. This storage is done digitally, after amplifier signals have been discriminated and digitized. Thus, for a given trigger latency, the rate of hits per unit area (which is proportional to luminosity) directly translates into a memory per unit area requirement. There is thus a fundamental connection between luminosity and logic density. Other things being equal (radius, trigger latency, ADC information), a chip with a given logic density can operate up to a certain luminosity and no higher. For higher luminosity one must increase the logic density (note there was no mention of pixel size, as the physical hit rate is per unit area, not per pixel). This was the reason for choosing the 65 nm CMOS process, which provided the highest logic density we had access to at the time.

Radiation damage also goes hand-in-hand with luminosity, but 65 nm CMOS was not required to improve radiation tolerance. On the contrary, very small transistors, as is possible with 65 nm but not in larger feature size nodes, present new challenges for radiation tolerance. In order to reduce radiation damage effects, the smallest transistors that can be made in 65 nm CMOS will in fact not be used in the RD53A chip. Even with such restrictions, the logic density will be between two and three times higher than in the 130 nm CMOS chip [3] of the present ATLAS inner pixel layer. We did not place such restrictions on FE65-P2, which therefore contains minimum size logic.

## 3. FE65-P2 Devices and Measurements

Measurements were performed on three FE65-P2 chips without a sensor, mounted on printed circuit boards. Two of them had been irradiated at the Los Alamos LANSCE facility in Spring 2016 to doses of 150 and 350 Mrad(Si) in an 800 MeV proton beam. We refer to these chips as "O Dose," "150 Mrad," and "350 Mrad." The tuned threshold variation with temperature and further radiation was then investigated at LBNL. LBNL irradiations used the 88" Cyclotron's 50 MeV proton beam. The per-pixel threshold was found by injecting charge of varying magnitude through a built-in calibration circuit. Charge injection was repeated 50 times at each value and the response (number of hits) of each pixel was registered. The result is a sigmoid curve for each pixel showing firing rate vs. injected charge. These data were fit to an error function (s-curve), with the mean being the threshold and the width the noise (sigma). All measurements involved first tuning the chip to a reference threshold and then measuring the variation with either temperature or radiation, without retuning. FE65-P2 chips can be operated with very low threshold (down to 300 $e^-$ before irradiation), but we chose a higher reference threshold of 800 $e^-$ or 1000 $e^-$ in order to reliably measure shifts in either direction. The higher value was used for the 350 Mrad chip in the irradiation setup, because of some difficulty tuning to 800 $e^-$ in the short time available.

### 3.1 Temperature Dependence

The three FE65-P2 chips underwent threshold stability measurements vs. operating temperature. The FE65-P2 and test board were placed in a temperature and humidity controlled environmental chamber. Each chip was first tuned to a threshold of 800 $e^-$ at 20 °C. The temperature was changed in 10 °C steps between -40 °C and 40 °C. At each increment the temperature was held stable while a threshold scan was performed.

### 3.2 88" Cyclotron Irradiation

Chips were irradiated one at a time to a dose of approximately 1 Mrad. The beam was stopped periodically and threshold scans were taken. The FE65-P2 test board was installed in a temperature controlled box set to -10 °C. Cooling was implemented with a vortex tube, which automatically provides dry air at the operating temperature, avoiding the risk of condensation within the cold box. As the available beam time was limited, the 50 MeV proton intensity was set to deliver 1 Mrad in about three hours: 10 times higher than the maximum expected during operation at the HL-LHC. The 0 Dose chip was further irradiated at half this rate to check the effect of dose rate on threshold shift. The test setup allowed the remote operation of current and voltage sources as well as the readout software used to perform threshold scans.

## 4. Results

For both experiments, two qualities were characterized for each column flavor: threshold mean and threshold dispersion. Given occasional failures in tuning each pixel properly, we compared only those pixels considered "well tuned" at 20 °C for the temperature measurements and at 0 dose for the irradiation data. For the 0 and 150 Mrad chips, these were determined to be those pixels with tuned threshold within 50 electrons of the nominal tuned threshold. The column flavors are

referred to by their number and corresponding features. Flavors 1 and 5 have no leakage current compensation (No LCC). All other flavors have LCC and are labeled LCC if they have no other features. Flavors 4 and 7 have no PMOS transistors of width less than 300 nm, to increase radiation hardness (RH). Finally, column flavor 3 has a power down feature (PD).

### 4.1 Temperature

Fig. 1 shows the shift in threshold mean vs. temperature for the 350 Mrad chip. In this chip, column flavors 4 and 7 (RH + LCC) perform best.

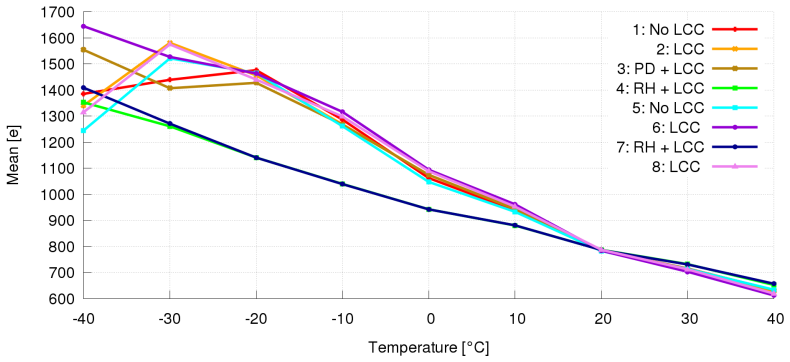


Figure 1: Threshold mean as a function of temperature of a chip tuned at 20 °C to 800 $e^-$ previously irradiated to 350 Mrad.

The per-pixel threshold distributions of column flavor 8 in all three chips just after tuning at 20 °C can be seen in Fig. 2. Fig. 3 shows the distribution of each chip at -20 °C without retuning. Both the threshold mean and dispersion increase with decreasing temperature, and the magnitude of the effect scales with total radiation dose.

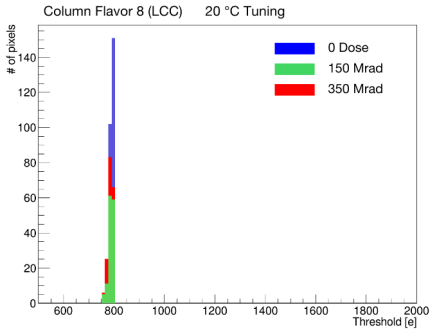


Figure 2: Threshold distributions of a 0, 150, and 350 Mrad chips tuned at 20 °C to 800 $e^-$.

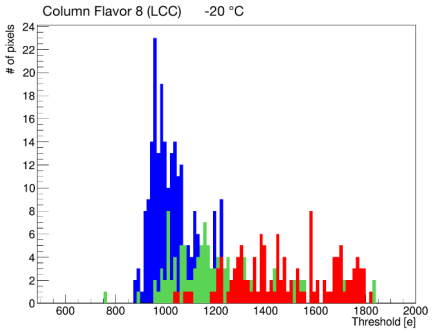


Figure 3: Threshold distributions of a 0, 150, and 350 Mrad chips at -20 °C

A linear fit was performed on the threshold mean data from all chips and all columns as shown in the example of Fig. 1. A linear fit was performed on the dispersion data after subtracting in quadrature the dispersion at the tuning point. Table 1 contains the results for the fit slope, characterizing the change in mean or dispersion with temperature. Flavors 4 and 7 have the smallest shift in mean across all chips. In the 0 Dose chip, flavors 4 and 5 have the lowest increase in dispersion, but as total dose increases, flavors 4 and 7 outperform all others. As the total dose increases, the rates increase across all chips as well, consistent with Figs. 2 and 3.

| Column Flavor | Threshold Shift [e$^-$/°C] | | | Dispersion Increase [e$^-$/°C] | | |
|---|---|---|---|---|---|---|
| | 0 Mrad | 150 Mrad | 350 Mrad | 0 Mrad | 150 Mrad | 350 Mrad |
| 1 (No LCC) | $3.4 \pm 0.4$ | $5.3 \pm 0.3$ | $13.0 \pm 0.8$ | $1.6 \pm 0.3$ | $1.8 \pm 0.1$ | $3.7 \pm 0.3$ |
| 2 (LCC) | $3.3 \pm 0.6$ | $5.1 \pm 0.3$ | $12.6 \pm 0.6$ | $1.9 \pm 0.4$ | $2.1 \pm 0.4$ | $4.0 \pm 0.3$ |
| 3 (PD+LCC) | $3.5 \pm 0.5$ | $5.2 \pm 0.3$ | $12.4 \pm 0.4$ | $1.8 \pm 0.3$ | $2.6 \pm 0.2$ | $6.1 \pm 0.9$ |
| 4 (RH+LCC) | $2.6 \pm 0.2$ | $4.3 \pm 0.1$ | $6.7 \pm 0.8$ | $1.4 \pm 0.1$ | $1.5 \pm 0.1$ | $3.1 \pm 0.6$ |
| 5 (No LCC) | $3.2 \pm 0.4$ | $5.3 \pm 0.3$ | $12.8 \pm 0.4$ | $1.2 \pm 0.1$ | $1.5 \pm 0.2$ | $3.6 \pm 0.3$ |
| 6 (LCC) | $3.2 \pm 0.4$ | $4.9 \pm 0.3$ | $13.7 \pm 0.5$ | $1.5 \pm 0.2$ | $2.6 \pm 0.1$ | $4.0 \pm 1.0$ |
| 7 (RH+LCC) | $2.9 \pm 0.3$ | $4.5 \pm 0.1$ | $7.2 \pm 0.3$ | $1.7 \pm 0.1$ | $2.0 \pm 0.1$ | $2.2 \pm 0.2$ |
| 8 (LCC) | $3.7 \pm 0.5$ | $5.1 \pm 0.3$ | $12.4 \pm 1.0$ | $1.7 \pm 0.1$ | $2.0 \pm 0.1$ | $5.0 \pm 1.0$ |

Table 1: The shift in mean and dispersion as temperature is decreased. The rate for mean shift is taken from a linear fit. The dispersion rate is taken from a linear fit after subtracting the original dispersion in quadrature.

### 4.2 Irradiation

Fig. 4 depicts the shift in threshold mean as a function of absorbed dose in the 0 Dose chip. The chip was retuned after 1000 krad and then further irradiated at half the original dose rate. The effect of the lower dose rate can be seen in the smaller slope from 1000 to 1300 krad. The sharp decrease at 1300 krad is due to a temperature increase to 20 °C as the device was removed from the setup. The column flavors with the lowest shift in mean are 4 (RH + LCC) and 5 (No LCC).

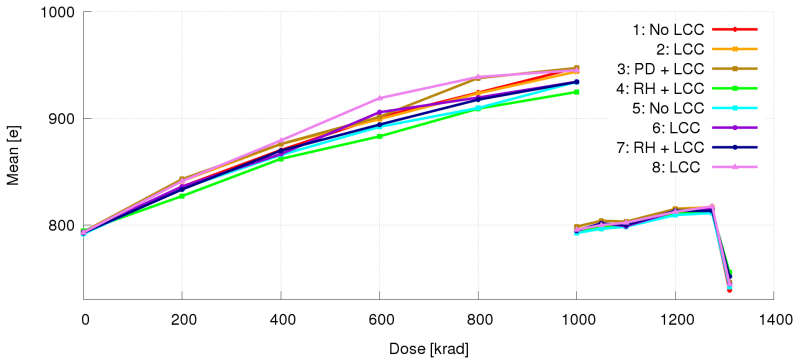


Figure 4: Threshold mean per radiation dose for an unirradiated chip. At 1 Mrad the chip was retuned and dose rate decreased. At 1.3 Mrad the temperature increased to 20 °C.

For the 150 and 350 Mrad chips the temperature was not stable during exposure, due to lack of time to wait for the setup to fully equilibrate between chip replacements. The temperature change during exposure was in all cases less than 5 °C, and was continuously monitored. Using the known temperature shifts from Table 1, the data were corrected and the shifts due only to irradiation extracted. Because each chip was tuned at low operating temperatures and the correction data was taken from room temperature tunings, an analysis was completed that ensured the shift rates agree in both cases. All radiation data shown are corrected for such temperature shifts.

A similar process was applied to find rate of change per Mrad dose (Table 2). In the 150 Mrad chip there is a small but still visible evolution of mean and dispersion. The threshold shift for this chip decreased in the best case to nearly 6 e$^-$/Mrad for flavors 2, 4 and 7. For the 350 Mrad chip,

shift in mean is consistent with zero within uncertainty, but interestingly the dispersion increases more than the 150 Mrad chip.

| Column Flavor | Threshold Shift [$e^-$/Mrad] | | | Dispersion Increase [$e^-$/Mrad] | | |
|---|---|---|---|---|---|---|
| | 0 Mrad | 150 Mrad | 350 Mrad | 0 Mrad | 150 Mrad | 350 Mrad |
| 1 (No LCC) | $160 \pm 10$ | $18 \pm 3$ | $2 \pm 4$ | $73 \pm 09$ | $9 \pm 3$ | $21 \pm 7$ |
| 2 (LCC) | $170 \pm 10$ | $6 \pm 2$ | $-16 \pm 8$ | $110 \pm 10$ | $11 \pm 3$ | $17 \pm 7$ |
| 3 (PD+LCC) | $170 \pm 10$ | $10 \pm 3$ | $-11 \pm 7$ | $100 \pm 10$ | $9 \pm 5$ | $26 \pm 8$ |
| 4 (RH+LCC) | $150 \pm 10$ | $7 \pm 1$ | $-5 \pm 5$ | $100 \pm 09$ | $11 \pm 3$ | $19 \pm 7$ |
| 5 (No LCC) | $150 \pm 10$ | $18 \pm 4$ | $0 \pm 4$ | $80 \pm 10$ | $13 \pm 3$ | $18 \pm 6$ |
| 6 (LCC) | $160 \pm 10$ | $11 \pm 2$ | $-23 \pm 6$ | $100 \pm 20$ | $11 \pm 3$ | $21 \pm 7$ |
| 7 (RH+LCC) | $160 \pm 10$ | $5 \pm 1$ | $-2 \pm 6$ | $100 \pm 10$ | $9 \pm 4$ | $16 \pm 6$ |
| 8 (LCC) | $180 \pm 10$ | $8 \pm 2$ | $-21 \pm 6$ | $130 \pm 20$ | $10 \pm 4$ | $19 \pm 10$ |

Table 2: Rate of shift in $e^-$/Mrad for threshold mean and dispersion, after correction for temperature shift.

## 5. Conclusion

Three FE65-P2 front ends have been tested for stability vs. temperature and radiation dose. Temperature change causes larger shifts in both mean and dispersion as chips acquire higher dose, while shifts vs. dose were only significant on for previously unirradiated chip. Therefore, stability vs. radiation dose will be the main concern for initial operation, while after an exposure of order 100 Mrad temperature stability will become the main concern. The "radiation hard" design variants (column types 4 and 7) mitigate both these effects, outperforming the other variants. They appear to be the best choice for the RD53A demonstrator to be produced in 2017.

## 6. Acknowledgements

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## References

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