The innermost layer of the CMS Detector at the LHC is the silicon pixel tracker. The current version of the detector has performed well and been critical to the physics program of CMS. The HL-LHC Upgrade of CMS will replace the entire silicon tracking system. As part of this upgrade, a proposed new section of the pixel tracker will be added in the so-called “very-forward” ($\eta \sim 4$) region of the detector. Because the particles in this region are traveling almost parallel to the magnetic field of the detector, enhanced $\phi$ sensitivity is required to accurately measure track curvature. Therefore, the proposed detector will reshape the standard $100 \times 150 \mu$m pixels to be more sensitive in $\phi$, sacrificing precision in $\rho$. A telescope is being developed for the express purpose of characterizing different pixel geometries. The telescope operates by using eight layers of silicon-strip sensors, with the device-under-test placed with four on each side. A charged-particle beam is directed so it passes through both the strip sensors and the device-under-test. Measurements from the telescope are taken to reconstruct individual particle tracks. These tracks are then compared to data collected from the device-under-test to characterize its performance.

## Hardware

### Analog Pipeline Chip (APC-128)

![APC-128 Testboard](image)

- Developed for the tracker of the H1 detector at HERA
- Serializes the analog pulse-heights of 128 channels to dramatically reduce the number of required I/O lines
- Capable of sampling waveform data from a strip sensor at up to 20MHz
- Features a very good signal-to-noise ratio of 40
- Low noise combined with inter-strip charge-sharing gives each layer of the detector a measurement precision of $\approx 1 \mu$m

### Sensor Board

- Features:
  - 8-channel, each with
  - 1-128-channel microstrip sensor
  - 4-APC-128
  - 4-40-Pin Headers

### Data Acquisition (DAQ) Board

- Features:
  - generates the control signals needed by the APC-128
  - 10 ADC channels to read out all APC128s in parallel, minimizing dead time
  - FPGA Board with associated HSB hardware enables high-speed communication with online software
  - Handles external triggering from a variety of sources via an translators receiver card

### DAQ Board

- Configuration shown has alternating 128 channels

### Desktop PC

- Online software organizes the hits into events and stores them to disk
- Since the detector layers can shift in space significantly during operation, alignment must first be done to accurately measure the geometry of the detector
- After alignment, various edge hits can be combined to construct extreme tracks
- The tracks can then be considered for consistency with the data collected in parallel from the device-under-test, and, using the telescope as the ground truth, establish performance characteristics

### References

- [PCB Design Files](https://github.com/cfangmeier/VFPIX-telecope-PCB)
- [Software Repository](https://github.com/cfangmeier/VFPIX-telecope-Code)

### Acknowledgments

Beat Meier & Tilman Rohe - The Paul Scherrer Institute
Frank Meier - Heidelberg University
Aaron Dominguez & Rachel Bartek - Catholic University of America
Brian Farleigh & Bob Kethy - University of Nebraska - Lincoln