

Development of a timing detector for the TOTEM experiment at the LHC

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The upgrade program of the TOTEM experiment foresees the installation of timing detectors inside vertical Roman Pots to allow the reconstruction of the longitudinal vertex position in presence of event pile-up in high β^* dedicated runs. The small available space inside the Roman Pot and the required time precision led to the study of a solution using single crystal CVD diamonds. The sensors are read-out using fast low-noise front-end electronics developed by the TOTEM Collaboration, achieving a signal-to-noise ratio larger than 20 for MIPs. A prototype was designed, manufactured and tested during a test beam campaign, proving a time precision below 100 ps and an efficiency above 99%. The geometry of the detector has been designed to guarantee a uniform occupancy in the expected run conditions keeping, at the same time, the number of channels below ten. In fact, each detector uses four diamond crystals of $4.5 \times 4.5 \text{ mm}^2$: one is segmented in four pixels, another in two, while the remaining pair is metallized with a single electrode. The detectors are read-out using the SAMPIC chip, a fast sampler designed specifically for picosecond timing measurements with high rate capabilities. Four aligned detectors will be installed in each Roman Pot to achieve a final precision below 50 ps. The first set of prototypes was successfully installed and tested in the LHC in November 2015.

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The TOTEM experiment has been designed to measure the total proton-proton cross section and to study elastic and diffractive scattering at the LHC energy. The measurement requires detecting protons at distances as small as 1 mm from the beam centre: TOTEM uses Roman Pots (RP), special beam pipe insertions, to move silicon detectors close to the outgoing beams to detect particles very close to the beam axis. The pile-up suppression capabilities of the TOTEM detectors can be improved using a timing detector. In fact, due to the high rapidity covered by RPs and their distance from the interaction point, the different vertexes cannot be discriminated using a tracking detector; however, measuring the arrival time of the protons, the longitudinal position of the different collisions can be reconstructed, as shown in Fig. 1.

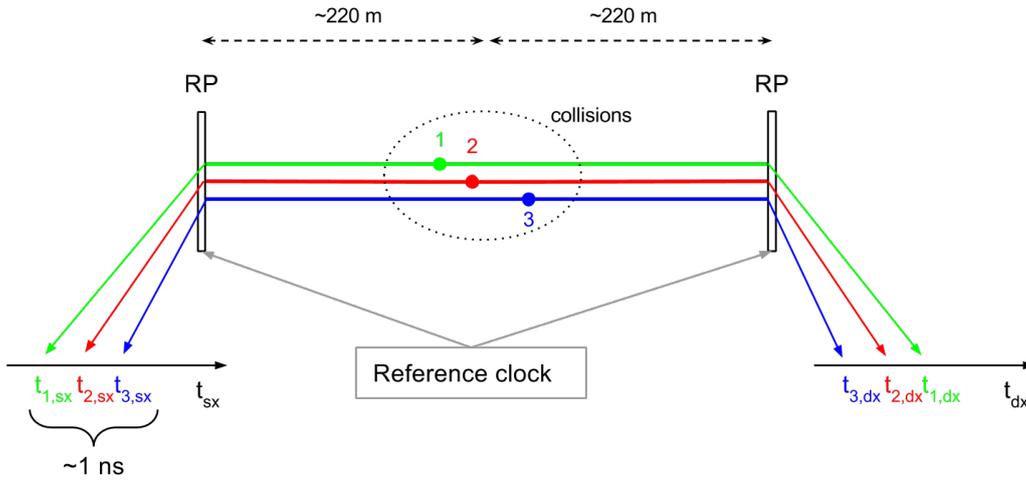


Figure 1: Detecting the arrival time of the protons on the two sides of the interaction point allows the reconstruction of the longitudinal position of the vertex.

1. The timing detector

A survey of the most promising technologies for precise timing showed that a resolution below 50 ps for MIPs is possible with 4 aligned single crystal diamond detectors, with a resolution of 100 ps each. The first part of an extensive beam test campaign was focused on the understanding and the characterization of the technology commercially available [3]; however, the performance and the cost of these solution were not suitable for the TOTEM requirements. Hence, the Collaboration started the development and the optimization of a front-end electronics using discrete components.

To keep relatively small the number of channels, the detector geometry was optimized to reduce the probability that multiple protons hit the same pad. Hence, the geometry of the detector reflects the expected hit distribution, in a way that the most hit region (closest to the beam) is covered by the smallest pads. The capacitance of the sensor, including the diamond itself, the bonding wire and PCB lines, are critical for the time resolution; therefore, following the design of the HADES start detector [4], a single transistor amplifier is placed as close as possible to the active area. Differently, the distance of the following amplifying and shaping stages is not critical, as it is possible to use adapted transmission lines. Due to the different size (hence capacitance) of the pads, the time resolution will worsen for the channels further away from the beam. The output signal

of each channel is digitized using a fast sampling chip and analysed using off-line algorithms. During the beam test campaign, the read-out electronics was optimized using prototype boards with a single diamond crystal. In a later stage, the final board with 4 diamond crystals was tested standalone and, then, installed in a RP prototype in the North Area at CERN, as shown in Fig. 2.

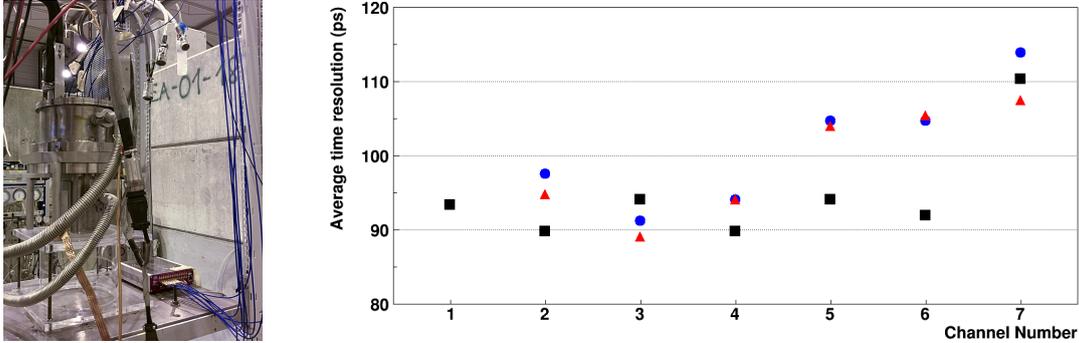


Figure 2: On the left: picture of the experimental setup in the North Area at CERN. On the right: time resolution computed measuring the time difference between two aligned boards. Black squares: time resolution computed using board 2 and 3; blue circles: time resolution computed using board 1 and 3; red triangles: time resolution computed using board 1 and 2 [1].

The optimization was focused on the improvement of the signal-to-noise ratio (SNR) keeping as fast as possible the signal. In fact, a quick rule of thumb to estimate the time precision of a detector is [1]:

$$\sigma \approx \sigma_{\text{noise}} \cdot \frac{\tau}{A} \approx \frac{\tau}{SNR} \quad (1.1)$$

where τ is the rise (fall) time of the output signal if positive (negative), A is the amplitude and σ_{noise} is the RMS of the noise, or equivalently $SNR = A/\sigma_{\text{noise}}$. Moreover, also the efficiency of the detector was measured using a silicon and a GEM tracker.

2. The Sampic chip

The SAMpler for PICosecond time (SAMPIC) chip has been designed by a collaboration including CEA/IRFU/SEDI, Saclay and CNRS/LAL/SERDI, Orsay. The design goal was to have a quick response (like TDCs) and the versatility of a waveform digitizer to perform accurate timing measurements. The chip is able to acquire 64 12-bit samples at 10 GSa/s, with an average rate above 300 kHz. These performance are achieved using a series of 64 capacitors per channel, controlled by delay lines, that continuously sample the input signal; when an acquisition is triggered, the sampling is stopped and the sampled values are digitized using a Wilkinson ADC. The time resolution obtained using smart algorithms to compute the arrival time using the digitized signal, i.e. constant fraction discriminator and fast cross-correlation, has been measured using a signal generator, the results are shown in Fig. 3, and then using silicon and diamond detectors. The SAMPIC chip will be installed on a motherboard developed by the TOTEM Collaboration that will allow the synchronization of the acquired data with the TOTEM trigger and DAQ systems.

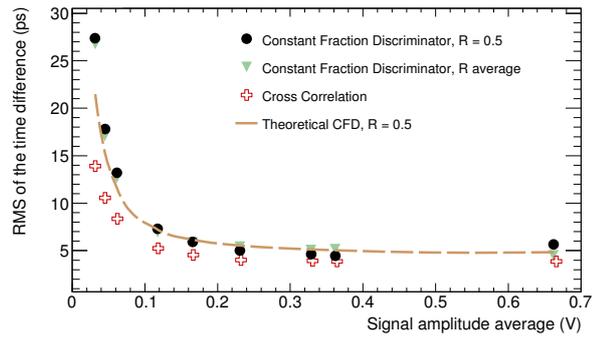
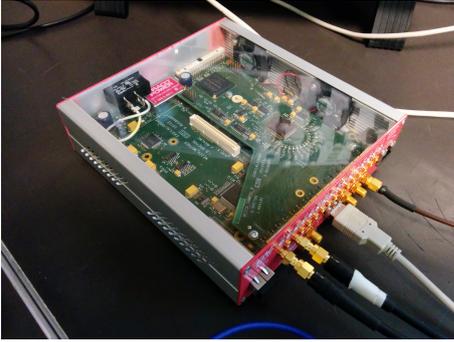


Figure 3: On the left: picture of the SAMPIC chip installed in the development board used for the tests. On the right: RMS of the time difference between two signals generated using a function generator and acquired at 6.4 GSa/s using the SAMPIC evaluation board. The time difference has been computed using three different algorithms and the RMS is shown as a function of the amplitude of the signal [2].

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