PROCEEDINGS OF SCIENCE

ATLAS Trigger and Data Acquisition Upgrades for High Luminosity LHC

William Balunas[*†]
University of Pennsylvania
E-mail: balunas@cern.ch

The ATLAS experiment at CERN is planning a second phase of upgrades to prepare for the High Luminosity LHC, due to start in 2026. In order to deliver an order of magnitude more data than previous runs, 14 TeV protons will collide with an instantaneous luminosity of 7.5×10^{34} $\mathrm{cm}^{-2}\mathrm{s}^{-1}$, resulting in much higher pileup and data rates than the current ATLAS detector was designed to handle. While this extreme scenario is essential to realize the physics program, it is a huge challenge for the detector subsystems, trigger, data acquisition and computing. The detector upgrades themselves also present new requirements and opportunities for the trigger and data acquisition system. Initial upgrade designs for the trigger and data acquisition system are presented, including the real time low latency hardware trigger, hardware-based tracking, the high throughput data acquisition system and the commodity hardware and software-based data handling and event filtering. The motivation, overall architecture and expected performance are explained. Some details of the key components are given. Open issues and plans are discussed.

38th International Conference on High Energy Physics
3-10 August 2016
Chicago, USA

[*]Speaker.
[†]On behalf of the ATLAS Collaboration.

PoS(ICHEP2016)858

1. Introduction

High Luminosity LHC (HL-LHC), scheduled to begin running in 2026, is planned to deliver far more instantaneous luminosity than the existing version of the accelerator (up to 7.5×10^{34} $\text{cm}^{-2}\text{s}^{-1}$, compared to 2016's 1×10^{34} $\text{cm}^{-2}\text{s}^{-1}$). This equates to as many as 200 interactions per bunch crossing (known as pileup), or 5-10 times the current value. As a result, the rates of all current triggers will increase by at least that amount, or in many cases more (as some behave non-linearly).

These amounts of pileup and data rate are far beyond what ATLAS was originally designed for [1], so a major upgrade of the Trigger and Data Acquisition system is necessary. This will include several new components in the hardware trigger and readout, as well as new software-based data handling and event filtering [2].

This is of particular importance for studying processes which rely on triggers whose rates scale strongly with pileup, such as $HH \to bbbb$ and $ZH \to \nu\nu bb$ among others. Many such analyses which are integral to the ATLAS HL-LHC physics program depend on reasonably low trigger thresholds to retain sufficient acceptance for their signals. These upgrades will achieve this goal by increasing the overall rate budget and by improving background rejection with more sophisticated trigger algorithms.

2. System Architecture

The design for the upgraded system (shown in Fig. 1) includes a two-level hardware trigger (described in Section 3), followed by a software-based Event Filter (described in Section 4). Level-0 receives information from the calorimeter and muon systems and runs hardware-based algorithms to reduce the event rate from 40 MHz to 1 MHz. Level-1 adds regional information from the new tracker (ITk), as well as better-granularity readout from the calorimeters. Due to the larger latency allowance relative to Level-0, more complex algorithms can be run here. This will further reduce the event rate to 400 kHz.

The Event Filter consists of a processor farm which makes a final selection in software for an output rate of 10 kHz. Full-detector tracking is available for 100 kHz of events from a hardware co-processor (FTK++). FELIX (Front End Link Exchange) will be the new interface between the subdetector electronics (which use custom optical serial links) and the rest of the DAQ system (which uses a standard multi-gigabit network). The links are bi-directional, allowing for both detector readout and control signals to be exchanged.

3. Level-0 and Level-1 Trigger

The hardware trigger is split into two levels: Level-0 is based heavily on the system which will already be built for an earlier upgrade of ATLAS between LHC Runs 2 and 3 (described in full detail in Ref. [3]), while Level-1 will consist entirely of new hardware.

The Level-0 trigger will run on inputs from the calorimeter and muon systems. For the calorimeter, coarse-grained information is read out and sent to three Feature Extractors, or "FEXes", which each run specialized hardware-level algorithms to find trigger objects, on which the decisions

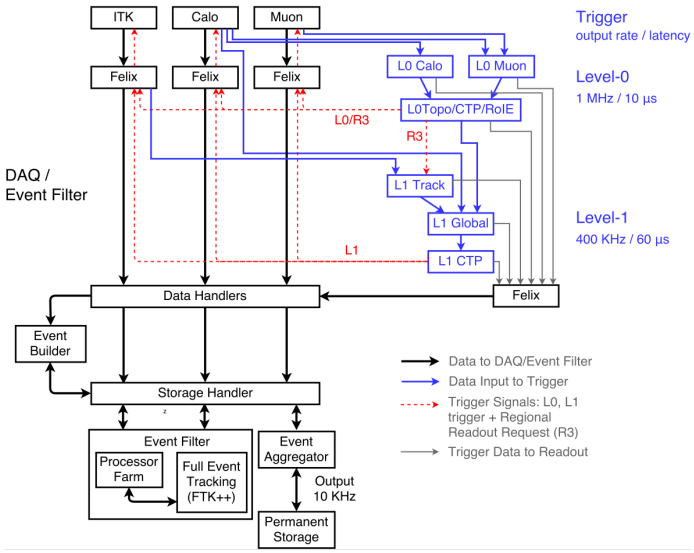

Figure 1: Schematic overview of the upgraded Trigger/DAQ system architecture.

are based. These are the eFEX (which identifies electromagnetic objects), jFEX (which searches for jets and missing energy), and gFEX (which computes global quantities and identifies jets from boosted objects). The Level-0 muon system will consist of the existing RPCs (Resistive Plate Chambers) and TGCs (Thin Gap Chambers), with one additional RPC layer which will be added in the barrel. Additionally, the MDT (Monitored Drift Tube) readout electronics will be completely replaced. This will allow MDT information to be used in the Level-0 decision, which is not possible currently due to readout rate and latency constraints. The Level-0 Central Trigger Processor (CTP) receives objects from these systems to make a final trigger decision. This can include topological relationships between the objects, such as cuts on angles between objects or invariant masses.

The Level-1 trigger adds in finer-grained calorimeter information as well as tracking to the trigger decision. The 60 μs total latency allowance means more sophisticated algorithms can be run at this stage (Figure 2). This will refine the event selection further, to an output rate of 400 kHz. L1Track performs track finding and fitting using low-latency regional tracker readout. The regions of interest are determined by Level-0. The track-finding will use associative-memory chips for pattern recognition and FPGA-based χ^2 fitting. The performance target is to reconstruct tracks down to a p_T of 4 GeV. After tracking is done, that information is combined with full-granularity calorimeter readout by the L1Global system to build refined trigger objects (electrons, jets, etc.). This includes iterative clustering and calibration algorithms which cannot be performed at Level-0. Finally, the Level-1 CTP receives all the trigger objects and results from L1Global, applies any prescales, and makes the final Level-1 accept decision. This output signal can be issued at a fixed latency from the beam crossing if required.

4. Data Acquisition and the Event Filter

After the data is transitioned to a commodity network via the FELIX system, it is reformatted by a PC-based Data Handler system and then buffered in the Storage Handler before being sent to

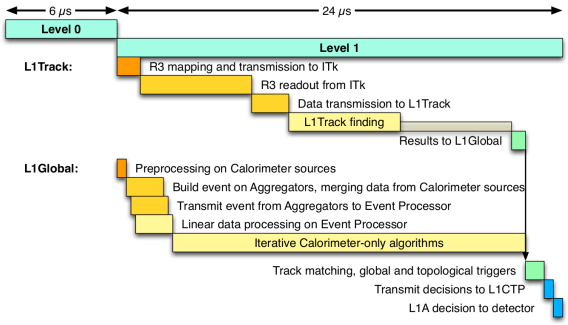

Figure 2: Latency budget for the Level-1 trigger. The design allows for up to 60 μs, including Level-0.

the Event Filter (EF) for the last level of trigger algorithms. The Storage Handler will be capable of buffering sufficient data to allow the EF to continue processing events between fills. This will require approximately 50 PB of storage volume, with a throughput rate of a few TB/s.

The Event Filter makes the final trigger selection using software algorithms that are close to offline reconstruction. This will likely be a heterogeneous system which can use both multi-core CPUs and GPGPUs. Full-detector tracking from FTK++ is used for events where it is available, complemented by near-offline quality EF tracking within regions of interest for all other events. Events which pass this step are written to permanent storage for physics analysis, at a rate of 10 kHz.

FTK++ is the successor to the ATLAS Fast Tracker (FTK). This will perform full-detector tracking down to $p_T > 1$ GeV at 100 kHz. Since the Level-1 output rate is 4 times larger, only certain events are selected for this, such as those passing Level-1 hadronic triggers. The tracker will also be extended to improve its acceptance, potentially out to $|\eta| = 4.0$.

5. Conclusions

The ATLAS Trigger and Data Acquisition system will undergo a significant upgrade for running at HL-LHC, with the goal of maintaining trigger thresholds as close as possible to their current values. It will involve a two-level hardware trigger, where the first level will largely re-use existing hardware and the new second level uses regional readout to allow a high rate of tracking. The output rate of the hardware trigger will be increased to 400 kHz. The data acquisition system will use a new common interface between custom detector serial links and a commodity network. A PC-based Event Filter will run near-offline algorithms to make the final trigger decision. This will be able to function asynchronously from the LHC fill cycle using a large storage capacity.

References

[1] ATLAS Collaboration, *The ATLAS Experiment at the CERN Large Hadron Collider*, JINST **3** (2008) S08003.

[2] ATLAS Collaboration, *ATLAS Phase-II Upgrade Scoping Document*, CERN-LHCC-2015-20, 2015.

[3] ATLAS Collaboration, *Technical Design Report for the Phase-I Upgrade of the ATLAS TDAQ System*, CERN-LHCC-2013-018, 2013.