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The ATLAS Fast Tracker Processing Units - track finding and fitting

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The Fast Tracker is a hardware upgrade to the ATLAS trigger and data-acquisition system, with the goal of providing global track reconstruction by the start of the High Level Trigger starts. The Fast Tracker can process incoming data from the whole inner detector at full first-level trigger rate, up to 100 kHz, using custom electronic boards. At the core of the system is a Processing Unit installed in a VMEbus crate, formed by two sets of boards: the Associative Memory Board and a powerful rear transition module called the Auxiliary card, while the second set is the Second Stage board. The associative memories perform the pattern matching looking for correlations within the incoming data, compatible with track candidates at coarse resolution. The pattern matching task is performed using custom application specific integrated circuits, called associative memory chips. The Auxiliary Card prepares the input and reject bad track candidates obtained from the Associative Memory Board using the full precision and a linearized fit. The track candidates from the Auxiliary Card use only 8 of 12 silicon layers, the track segments are extended to the additional layers by the Second Stage Board. During the first half of 2016, the first Fast Tracker VMEbus Processing Units was installed in the ATLAS cavern.

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1. Introduction

The FastTracKer (FTK)[1] is a Phase-I upgrade for the ATLAS detector[2] trigger system. Its goal is to run full detector tracking for each event passing the Level-1 (L1) trigger, with the output tracks ready for use by the software-based High Level Trigger (HLT). This requires processing an event rate of 100 kHz with a latency of a few tens of μs. The system is expected to operate at pile-up conditions of up to 70 interactions per second. The output of FTK can be useful for improving b-tagging, hadronic τ-tagging and pile-up suppression in the trigger.

FTK accomplishes the hard problem of track finding at high rates by implementing a massively parallel system using a combinations of custom ASICs and high-performance FPGAs. The entire system consists of several boards implemented in a mix of VME and ATCA standards. First a copy of the hits in the ATLAS silicon pixel and strip (SCT) detectors are clustered and sorted into overlapping η-ϕ regions called "towers". Each tower is associated with a Processing Unit (PU). The PU is responsible for the 8-layer pattern recognition using coarse-resolution coordinates called SSIDs and first stage fit to reduce data-flow volume. It consists of the Associative Memory Board and the Auxiliary card. Subsequent boards perform an extrapolation of the track candidates to the remaining 4 detector layers, calculating the helix parameters and formatting the output for the HLT.

This document describes the the Processing Unit in more detail. For more information on the FTK input and output cards, see [3].

2. Hardware and Firmware Implementation

The Processing Unit hardware consists of two boards. The Associative Memory board (AMB) and its powerful Auxiliary card (Aux). They are designed to fit in an extended 9U VME crate. They communicate via user-defined pins in the VME J1/P1 connector and an extra P3 connector. The layout of the two boards is shown in figure 1.

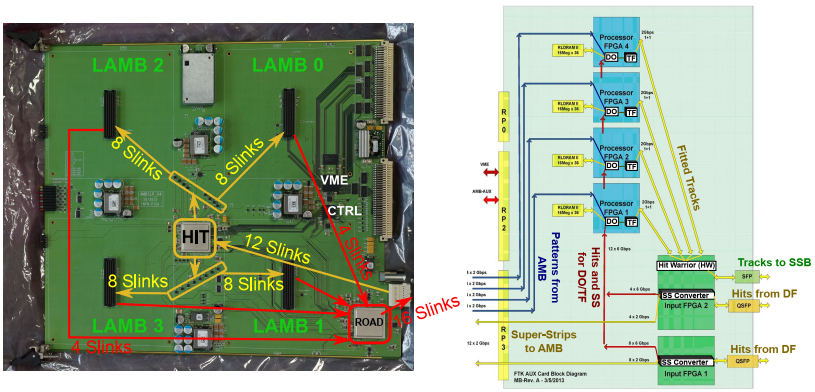

Figure 1: The layout of the AMB (left) and Aux (right). High-speed links and location of FPGAs are shown.

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2.1 Auxiliary Card

The Auxiliary Card contains six Altera Arria V FPGAs. Two of them, named Input 1 and 2 are used to process the input hits. In addition, Input 2 also handles overlap removal and output to the next board. The other four are called Processors and perform the first stage fit.

The input hits are received over two QSFP cables, one cable per Input FPGA, using a modified HOLA S-LINK protocol[4]. The SSIDs are calculated via a look-up table called the SSMap and sent to both the AMB and the nearest Processor. They are then forwarded to all Processors using a daisy-chain implemented using the Reverse Serial Loop-Back feature of the FPGA.

Each Processor fits the output of a single LAMB. First the Data Organizer (DO) uses a database to associate each road with the full-resolution hits, while at the same time preparing it for the next event. Then the Track Fitter (TF) performs a linear fit using pre-loaded constants to calculate the χ^2 and remove track candidates failing a threshold. The TF consists of three fitter types. A nominal fitter handles roads with all 8 layers containing hits, while a majority fitter handles roads with a missing layer. Each processor has 1 nominal, 3 pixel majority and 5 SCT majority fitters.

The final block in the Auxiliary card processing chain, called the Hit Warrior (HW), is responsible for combining tracks from the four Processors and removing duplicates. Tracks are defined as duplicates when they are within the same road and share hits. The combined tracks are sent out over an SFP link, using the modified HOLA S-LINK protocol.

2.2 Associative Memory Board

The Associative Memory Board is responsible for managing the power distribution and control of up to 64 AMChips. They are connected to the board using mezzanine cards called Little Associative Memory Boards (LAMB). Each LAMB carries 16 AMChips. During typical operations, the AMB will consume around 250 W of power.

The data processing is performed using four Xilinx FPGAs; HIT, ROAD, CONTROL and VME. The VME chip is used to handle the VME communication with the AMB and Aux FPGAs. The CONTROL FPGA handles the state-machine controlling event processing. The HIT FPGA forwards the input SSIDs to the AMChips. To reach all 64 AMChips, three levels of fan-out are required. The ROAD FPGA handles the road output of the AMChips, sending them to the Aux.

2.3 Associative Memory Chip

The Associative Memory chip is a custom 65 nm ASIC responsible for matching pre-loaded patterns against hits in the tracking detector. It is based on an array of CAM cells, with functionality to look for correlations in time. A layer block consists of 18 CAM cells, corresponding to an SSID. Three pairs of them are used as ternary bit, allowing for variable width functionality called “Don’t Care”. Eight layer blocks are grouped into a single pattern. At least seven layer matches are

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required for a pattern match. Figure 2 shows a schematic of the pattern matching and read-out functionality.

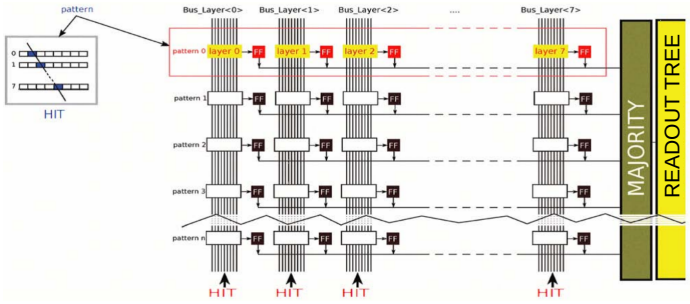

Figure 2: The schematic of the AMChip's pattern matching functionality. Columns correspond to a hit's position in a tracker layer. Rows corresponds to a single pattern.

Each chip contains 128k patterns and runs on a 100 MHz clock. This results in 10^{14} pattern comparisons per second. The patterns take up 70% of the 11 x 15 mm^2 die size.

3. Integration and Status

The core firmware for both the Associative Memory board and the Auxiliary card has been developed. The cards have been tested individually at their home institutions using testvectors from simulated ttbar events. The Aux has also been shown to work with real data from the detector, but without AMB input.

The integration of the two cards has started and is progressing well. The bit-error rate between the two cards less than 10^{-15}. Simulated ttbar testvectors flow continuously up to the Data Organizer in the Aux, with correct patterns being fired by the AMChip. Debugging is on-going to finish the chain.

In terms of availability, all Aux cards required for the initial phase of the installation have been produced. Four AMB boards, with two being the final revision, are available for testing. Fifteen more will be available by the end of summer 2016. They can be fully loaded with AMChip06s, as 2000 have been produced and characterized.

References

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[4] O. Boyle et al, *The SLINK Interface Specification*, March 1997, http://www.cern.ch/HSI/s-link/

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