

ATLAS Tracker and Pixel Operational Experience

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The tracking performance of the ATLAS detector relies critically on the silicon and gaseous tracking subsystems that form the ATLAS Inner Detector. Those subsystems have undergone significant hardware and software upgrades to meet the challenges imposed by the higher collision energy, pile-up and luminosity that are being delivered by the LHC during Run2. The key status and performance metrics of the Pixel Detector and the Semi Conductor Tracker, are summarised, and the operational experience and requirements to ensure optimum data quality and data taking efficiency are described.

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1. Introduction

The Inner Detector (ID) of the ATLAS experiment[1] is responsible for particle tracking in ATLAS and employs three different detector technologies: a silicon Pixel Detector closest to the interaction point, the Semiconductor Tracker (SCT) micro-strip silicon detector, and a Transition Radiation Tracker (TRT). The Pixel Detector was supplemented in 2014 with the Insertable B-Layer (IBL), an extra layer of pixelated silicon installed closest to the interaction point in the space made available by the installation of a smaller beam pipe. The overall ID is 5.6 m long and 2.1 m in diameter, and resides in a 2 T axial magnetic field. The layout of the four detector elements is shown in Figure 1, and the channel counts and detecting element sizes are summarised in Table 1.

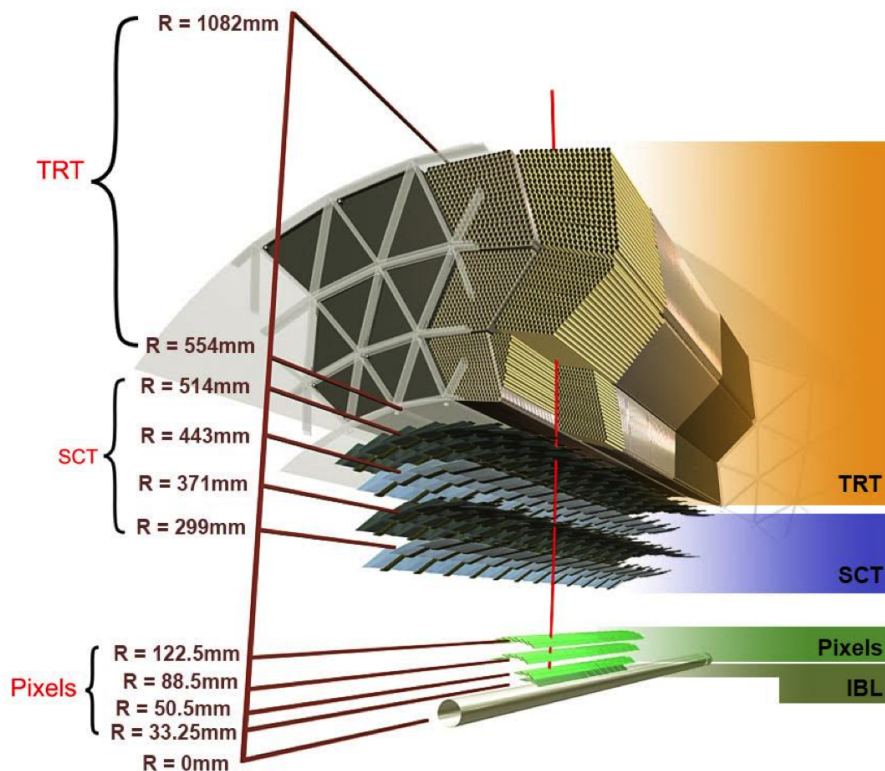


Figure 1: Layout of the central section of the Inner Detector.

The SCT comprises 61 m² of silicon microstrip sensors arranged into 4 concentric cylinders and 9 disks at each end. It is 5.6 m long and extends to 0.7 m in radius at the disks, providing a 4-hit system extending to $|\eta| < 2.5$ for tracks originating from the collision point. The basic detector element is the SCT module, an independently powered and read out detector unit comprising two pairs of sensors glued back to back to a thermally conductive substrate. The cylinders are assembled using 2112 modules with a rectangular shape of size 6×12 cm², but the the two end-caps each use 998 modules of three different wedge shapes to accommodate the more complex geometry. Each side of the module with 768 microstrips is read out by six 128-channel ABCD chips; the signal

	Channels	Element Size	Resolution (μm)
IBL	12×10^6	$50 \mu\text{m} \times 400 \mu\text{m}$	8×40
Pixel	80×10^6	$50 \mu\text{m} \times 500 \mu\text{m}$	10×115
SCT	6.3×10^6	$80 \mu\text{m} \times 12 \text{ cm}$	17×570
TRT	3.5×10^5	4mm	130

Table 1: Channel counts and detecting element size for the ID silicon subsystems.

from each channel is pre-amplified, shaped and then discriminated at 1fC threshold to provide a binary output. Following a level-1 trigger, three bits are read out per channel corresponding to the presence of a hit in the preceding, in-time and following bunch crossings.

The Pixel Detector is 1.4 m long and 0.25 m in radius, comprising 1.7 m^2 of pixelated silicon arranged into 3 concentric cylinders and 3 disks at each end. It provides a 3-hit system extending to $|\eta| < 2.5$. There is one unique module shape of size $62.4 \times 21.6 \text{ mm}^2$, comprising a single $16.4 \times 60.8 \text{ mm}^2$ sensor with 46080 pixels. There are 1744 Pixel modules in total, assembled to 13-module staves in the cylinders and 6-module sectors within the disks. Each module has 16 front-end (FE) chips with event building performed by the Module Control Chip (MCC). Charge measurement is determined using an 8-bit Time over Threshold (ToT) counter.

A schematic of the Data Acquisition (DAQ) hardware and the data connectivity between its components is shown in Figure 2 for both the SCT and Pixel Detector.

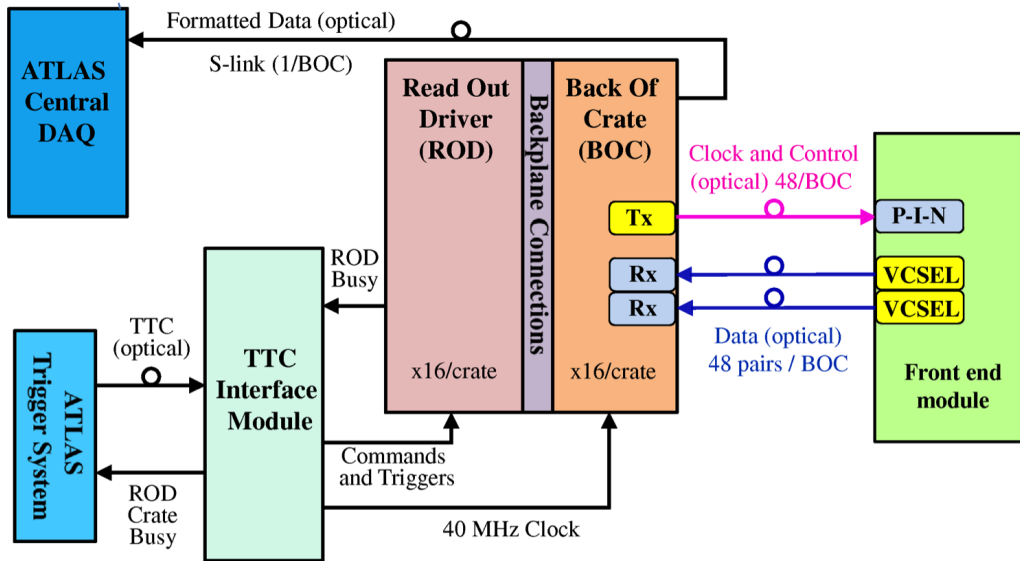


Figure 2: Schematic of the SCT and Pixel DAQ hardware and data connectivity paths. Tx and Rx refer to the off-detector optical transmitters and receivers, respectively.

The Back of Crate card (BOC) is the optical interface between the Readout Driver (ROD) and up to 48 modules. A single optical link broadcasts the trigger, clock and command signals to the module, and two optical links return data from the module, one for each side. The ROD processes

the incoming module data at the level 1 trigger rate and combines those data into a single ROD fragment, which is transmitted via a single fibre (the "S-link") to the ATLAS Central DAQ where it is buffered pending a higher level trigger decision. Each ROD can generate a "busy" signal to inhibit triggers from the ATLAS trigger system, in the case of a processing fault or bandwidth limitation on the ROD.

Optical communication on the control and data streams are implemented by Vertical Cavity Surface-Emitting Laser (VCSEL) arrays and p-i-n diodes. Redundancy can be implemented for the SCT optical links, in the event of fibre breaks, or defective VCSEL or p-i-n diodes. Tx redundancy can be applied so that an SCT module receives the clock and command signals from its neighbouring module. Similarly, Rx redundancy can be applied to transmit 12-chip data from both sides of the module on a single data link, instead of two links of 6-chip data.

Both the SCT and the Pixel Detector need to be operated below 0°C to dissipate the heat from the front-end chips and to minimise the impact of radiation damage to the sensor depletion voltages and leakage currents. Both detectors employ bi-phase evaporative cooling using C₃F₈, using 212 individual cooling loops sourced by a common cooling plant.

2. Operations Overview

The operations roadmap of the Large Hadron Collider (LHC) is summarised by Figure 3. There are three distinct run phases before the LHC and the ATLAS tracking detectors will be significantly upgraded in 2024; Run1 refers to the proton-proton operations at 7 TeV and 8 TeV collision energy with modest luminosity conditions, Run2 marks the transition to operation at 13 TeV and 14 TeV collision energy with LHC exceeding nominal design luminosity, and Run3 anticipates potentially a factor 2 (or higher) increase in design luminosity. Two long shutdowns (LS1 and LS2) separate the LHC Runs, providing opportunities for upgrades and repair work.

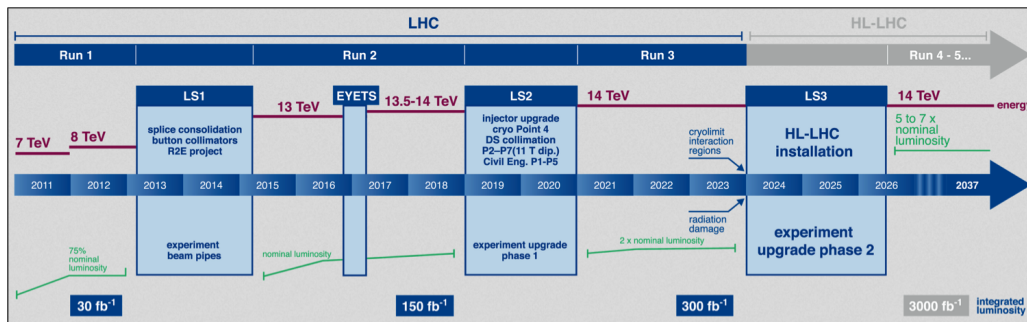


Figure 3: The Large Hadron Collider operations roadmap.

The ATLAS experiment recorded 26.4fb^{-1} of proton-proton collision data in Run1 and 39.9fb^{-1} by the end of 2016 in Run2. There are two potential sources of data-taking inefficiency from the SCT and Pixel Detectors: the time taken to switch on the SCT and Pixel Detector upon the declaration of stable beam conditions by the LHC (referred to as 'warm start'), and a busy from the Data Acquisition System (DAQ) which inhibits ATLAS data-taking due to a DAQ fault. The warm start typically took 60–90 seconds, and the busy fraction typically $\ll 1\%$ during a physics fill of several

hours. Data Quality (DQ) efficiency is the fraction of recorded data that can be used for physics analyses; the two main inefficiency sources are errors from the front-end chips which flag that data fragments from those chips cannot be used for tracking, and the disabling of DAQ components which result in an intolerable fraction of the detector not returning data.

3. Operations Issues

Table 2 summarises the fraction of active readout channels and the luminosity weighted fraction of good quality data for the stated year, ranging from the start of Run 1 and up to the end of 2016 in Run 2. Both systems delivered excellent availability and tracking performance at all times, though subtle variations in Table 2 reflect some of the three main operational issues: deaths in the off-detector optical transmitters, on-detector connectivity breakages in the Pixel Detector services due to cooling cycles, and data processing flaws within the firmware of the RODs, exposed by the increasing trigger rate and occupancy levels.

	Active Fraction (%)		DQ Fraction (%)	
	Pixel	SCT	Pixel	SCT
2010	97.5	99.1	99.9	99.8
2012	95.0	99.0	99.8	99.1
2015	98.0	98.6	93.5	99.4
2016	98.3	98.7	98.9	99.9

Table 2: Status of the SCT and Pixel Detector at the beginning and end of Run1, and during Run2, indicated by the fraction of active channels, and luminosity weighted fraction of good quality data.

During Run1, both systems experienced significant numbers of single-channel deaths within the 12-channel VCSEL arrays of the off-detector TX optical transmitters. The immediate consequence of a TX channel failure was that the module no longer received the clock and command signals, and therefore no longer returned data. VCSEL failures were originally attributed to inadequate electrostatic discharge (ESD) precautions during the assembly of the VCSEL arrays into the TX plug-in, and the entire operational stock of the 12-channel TXs were replaced in 2009 with units manufactured with improved ESD procedures. However channel deaths continued in 2011, attributed to degradation arising from exposure of the VCSELs to humidity. In 2012, new VCSEL arrays were installed; these VCSELs contained a dielectric layer to act as a moisture barrier, and as expected these TXs remain operationally robust.

The impact of VCSEL channel deaths was mitigated for the SCT by applying TX redundancy, whereas for the Pixel Detector a TX channel death was non-recoverable and required a BOC extraction and the replacement of the TX plugin containing the VCSEL array, which was a major intervention with risk of damage to exposed optical fibres. The application of TX redundancy for the SCT detector varied significantly due to the TX channel deaths, reaching up to ~ 240 at its worst in 2011 as shown in Table 3.

The Pixel Detector experienced significant degradation in working channel counts in Run1 due to thermal-cycle induced breakages. The detector was extracted to the surface during LS1

	Number of links	Links using redundancy	
		Run1	Run2
TX	4088	14 (up to 240)	27
RX	8176	132	147

Table 3: Use of optical link redundancy in the SCT at the end of Run1 and at the end of 2016 in Run2.

for the replacement of its Service Quarter Panels (SQPs) which extend the powering, cooling and optical services to the Pixel Detector in the centre of ATLAS. As well as replacing existing faults, the new SQPs supported the relocation of the on-detector opto-transceivers to an accessible area for future access, to make future such repairs possible without re-extraction of the Pixel Detector. Figure 4 shows the category of breakages and the module recovery status in the different Pixel layers following LS1.

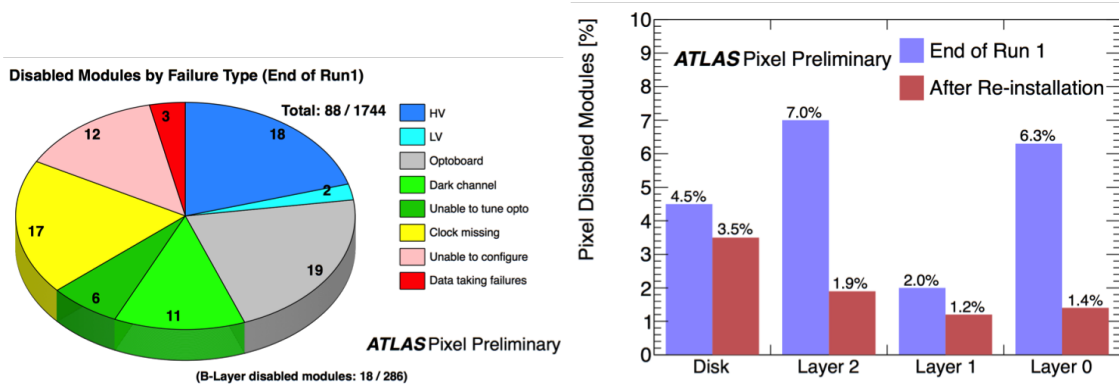


Figure 4: The Run1 disabled module count by failure type in the Pixel Detector (left figure), and the disabled module fraction per Pixel layer following repair during LS1 (right figure) [2].

Late in Run1 and early in Run2, the increasing luminosity and associated pile-up¹ started to impact on the data taking and DQ efficiencies of both the SCT and of the Pixel innermost layer. By the end of 2016 these issues were largely resolved due to firmware improvements and steps to mitigate occupancy, as shown in Figure 5. For the Pixel innermost layer, the analogue threshold used to determine the ToT was raised together with cuts in the ToT itself, while the SCT implemented effective recovery of SEU-induced bit flips in the front-end chip threshold registers to minimise noisy chips, and switched to a data compression mode which vetoes hits registered in the first sampled time bin, corresponding to the previous bunch crossing. Following these steps, optimal data taking efficiencies were achieved even with the high luminosities in 2016.

4. Coping with high luminosity and pile-up

The ATLAS tracking systems were designed to operate at the LHC design luminosity of

¹The term pile-up refers to multiple pp interactions per bunch crossing.

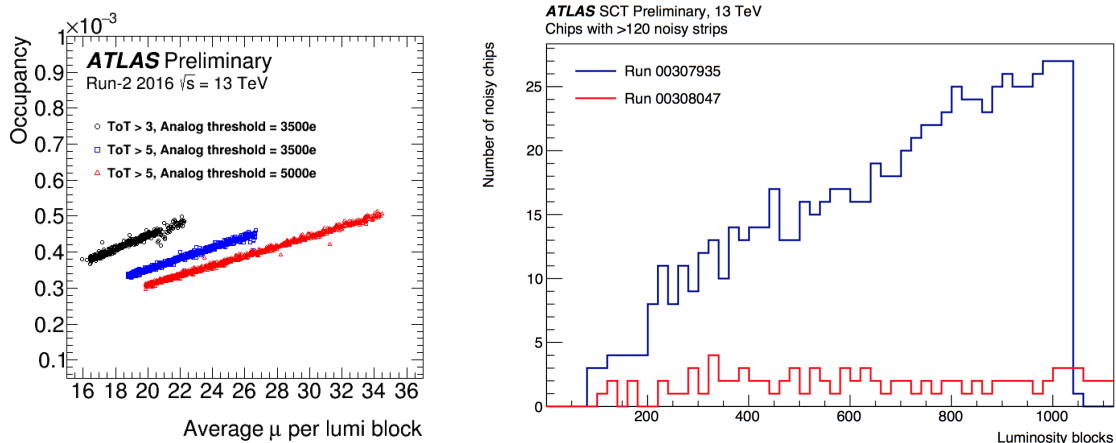


Figure 5: Examples[2] of occupancy mitigation: occupancy vs pile-up (μ) for the innermost Pixel layer with varying threshold and ToT thresholds (left plot) and the impact of Single Event Upset (SEU) recovery on the noisy chip count in the SCT (right plot). Luminosity block refers to a 1-minute time interval.

$1 \times 10^{34} \text{ cm}^{-2}\text{s}^{-1}$ and pile-up of up to 23 interactions per bunch crossing. Both these parameters were routinely exceeded in 2016, with pile-up reaching ~ 50 , and with expectations of up to twice nominal luminosity by the end of Run2. Both the SCT and Pixel systems implemented upgrades to the DAQ during LS1 in preparation for higher occupancy and trigger rate.

There are two potential bottlenecks within the SCT DAQ shown in Figure 2: the optical links which transmit data from the front-end chips at 40Mbps, and the S-links which transmit ROD data fragments containing data for up to 48 modules at 1.28 Gbps. During Run1, the SCT had 90 RODs in 8 ROD crates, with 4–5 empty slots in each crate. An extra 38 RODs and BOCs were installed in the empty slots during LS1 resulting in 38 extra S-links. The incoming front-end data links were redistributed across more RODs reducing the number of modules processed by each ROD from up to 48 to up to 36. Figure 6 shows the maximum sustainable trigger rate as a function of pile-up for both the front-end links and the S-links, with the newly expanded DAQ. The front-end links in magenta indicate those links that use RX-redundancy which transmit data for up to 12 chips instead of the nominal 6 chips. Supercondensed mode for the ROD indicates optimal data compression without inclusion of the 3-bit time bin information per hit.

Figure 7 shows the number of front-end links and S-Links that exceed the bandwidth limitations as a function of pile-up assuming a 100kHz L1 trigger rate. For the S-links the plots also indicate data with the ROD configured in expanded mode, which includes the 3-bit time bin information. The plots indicate that bandwidth limits are exceeded on an increasing number of links from a pile-up of ~ 55 upwards. Those links using RX-redundancy can be recovered to match those that do not use redundancy by disabling a small number of chips ($\sim 0.1\%$ of the total chip count) on each link, with negligible impact on tracking performance.

For the Pixel Detector, the readout links of the middle and outermost barrel layers were expected to exceed bandwidth limitations early in Run2. The extraction of the detector during LS1

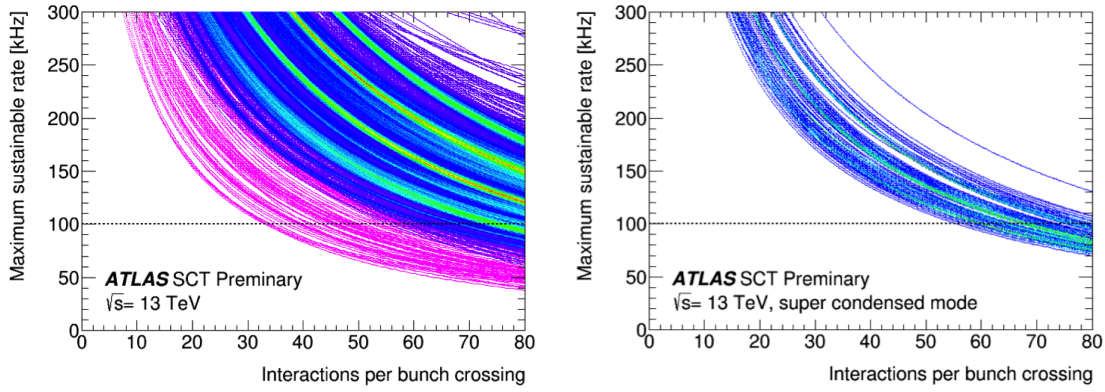


Figure 6: The maximum sustainable trigger rate in kHz as a function of pile-up for each of the 8176 SCT front-end links (left plot) and each of the 128 SCT S-links (right plot) [2].

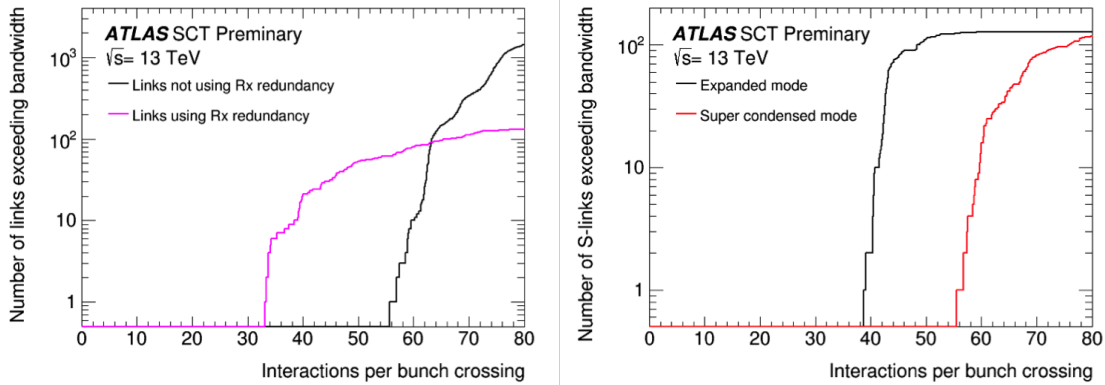


Figure 7: The number of SCT data links which exceed bandwidth limitations at 100kHz trigger rate as a function for pile-up for the front-end links (left plot) and S-links (right plot) [2].

provided the opportunity to install additional data links from the newly installed opto-transceivers and increase clock speed as detailed in Table 4. The Pixel S-Link bandwidth limitation is being improved by a staged replacement during the end of year stops in Run2 of the Pixel RODs and BOCs by the newly developed models for the IBL.

Pixel Layer	Run1	Run2
Disks & Inner Barrel	160 Mbps	160 Mbps
Middle Barrel	80 Mbps	2×80 Mbps
Outer Barrel	40 Mbps	80 Mbps

Table 4: Pixel front-end data link bandwidth in Run1 and Run2.

5. Radiation Damage

The most dominant impact of radiation damage to the SCT and Pixel Detector is the increase

in sensor leakage currents and the initial decrease then subsequent increase of depletion voltage as the silicon bulk passes through type inversion. Operationally, these changes require modifications to the voltage applied to ensure full depletion of the silicon, and modifications to leakage current thresholds (which are set low enough to flag anomalous leakage currents, but high enough to track the increase from radiation damage). The mean leakage currents for the four SCT barrel layers throughout Run1 and up to 2016 in Run2 are shown in Figure 8, with comparisons to model predictions using the Hamburg-Dortmund model[3][4]. The plot shows excellent agreement with model predictions, and strong correlation with fluence and module temperature.

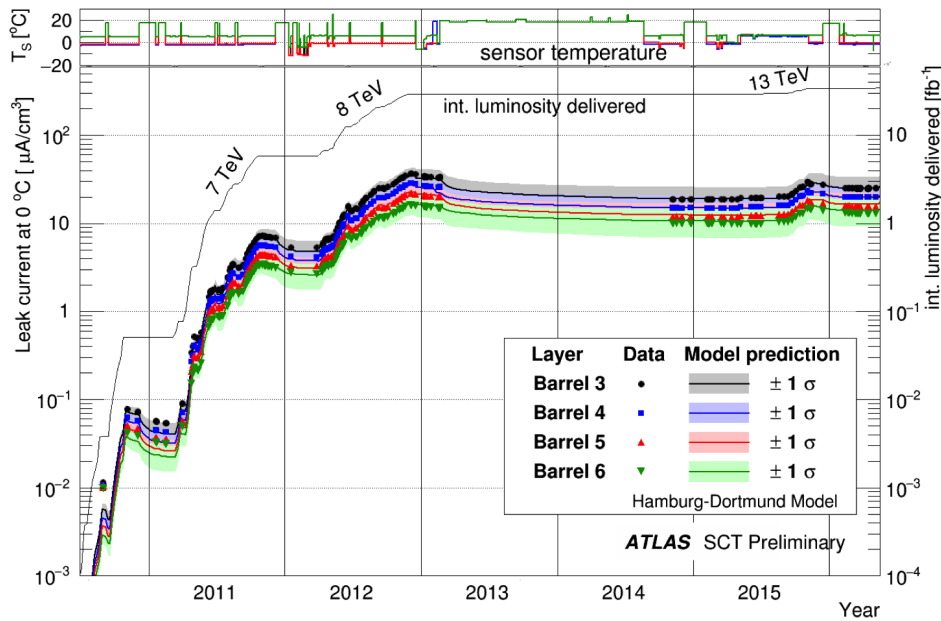


Figure 8: Comparison between data (points) and Hamburg/Dortmund model predictions (lines with uncertainties shown by the coloured bands) of the leakage current per unit volume at 0°C of the four SCT barrel layers [2]. The variations in sensor temperatures are due to cooling stops.

Figure 9 shows the projected long term evolution in leakage currents for the innermost SCT barrel layer, using the same Hamburg-Dortmund model[3][4] and assuming the delivered luminosity projections shown in Figure 3. The plot shows three different scenarios for module temperatures, including raising the silicon to room temperature for the full duration of LS2. The plot indicates that leakage currents will remain acceptable for operation SCT at the end of the SCT lifetime. Similar projections apply for the Pixel Detector.

6. Summary

The SCT and Pixel Detector are now operating in Run2 with luminosities and pile-up which significantly exceed original design goals, and continue to deliver excellent tracking performance and detector acceptance. Both systems successfully upgraded their DAQ systems during LS1 to

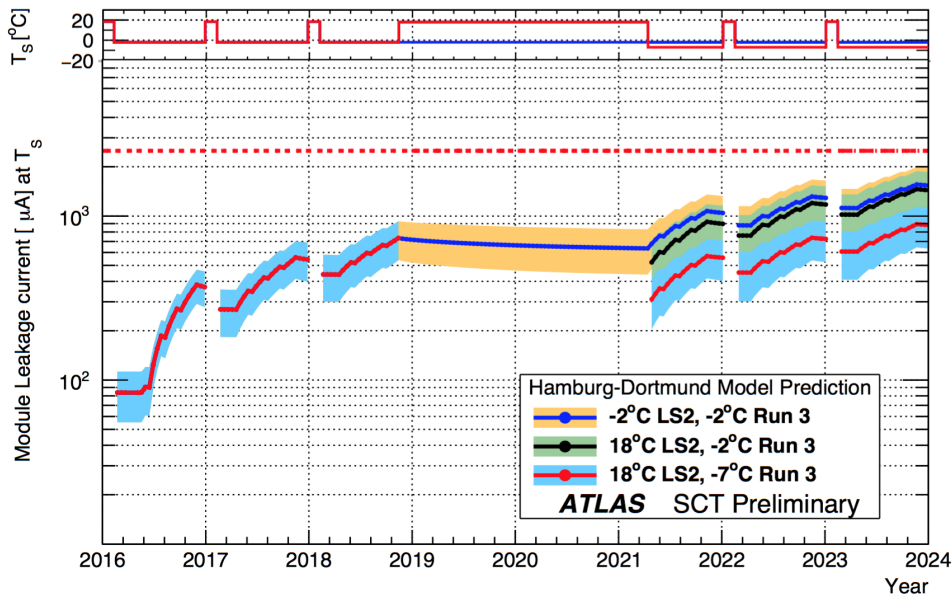


Figure 9: Leakage current projections up to LS3 for the innermost SCT barrel layer, with different temperature scenarios [2]. The horizontal dashed line indicates the conservative current threshold for the onset of thermal-runaway.

address the bandwidth limitations inherent in the Run1 configuration. The dominant operational issues so far have been the single channel deaths of the off-detector TX optical transmitters in Run1, and data processing flaws within the RODs that were exposed by the increasing occupancy and trigger rates. Both issues have been addressed with optimal data taking efficiencies now achieved even at the highest luminosities in 2016. Radiation damage effects closely match expectations, with long term projections indicating that leakage currents will remain within operational limits throughout the anticipated lifetime of the detectors.

References

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