PROCEEDINGS OF SCIENCE

Silicon Vertex Tracker for CLAS12 experiment

Yuri Gotra* **on behalf of the CLAS Collaboration**
Thomas Jefferson National Accelerator Facility, Newport News, VA, USA
E-mail: gotra@jlab.org

The Silicon Vertex Tracker is a central tracker built for the CLAS12 experiment aiming at measuring the momentum and reconstructing the vertices of charged particles emerging from the target. The system is designed to operate at a luminosity of $10^{35} cm^{-2} s^{-1}$ and to have a momentum resolution of 5% for 1 GeV tracks. The tracker is centered inside 5T solenoid magnet and has 33792 channels of Hamamatsu silicon microstrip sensors. To lower the amount of materialal in the tracking volume modules are assembled on barrel structures using unique cantilevered geometry. The sensors have graded angle design to minimize dead areas and a readout pitch of 156 μm. Double sided module hosts three daisy-chained sensors on each side with total strip length of 33 cm. There are 512 channels per module read out by four Fermilab Silicon Strip Readout (FSSR2) chips featuring data driven architecture, mounted on a rigid-flex hybrid. We describe the detector and present performance results from tracker commissioning with cosmic muons.

The 25th International workshop on vertex detectors
September 26-30, 2016
La Biodola, Isola d'Elba, ITALY

*Speaker.

PoS(Vertex 2016)008

1. Introduction

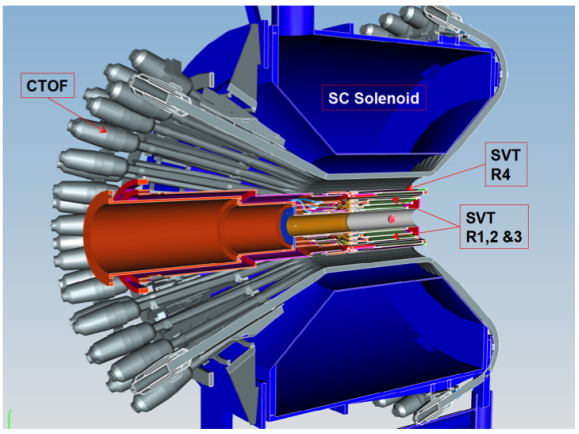

Figure 1: CLAS12 central detector

The Continuous Electron Beam Accelerator Facility's (CEBAF) Large Acceptance Spectrometer (CLAS) at Jefferson Lab is being upgraded for the 12 GeV electron beam to conduct spectroscopic studies of excited baryons and of polarized and unpolarized quark distributions, investigations of the influence of nuclear matter on propagating quarks, and measurements of Generalized Parton Distributions (GPDs) which require tracking of low momentum particles with few percent momentum and about one degree angle resolution at large angles [1]. Deep exclusive reactions, in which an electron scattering results in a meson-baryon final state, provide stringent requirements for the CLAS12 tracking system. The central tracker consists of a solenoid, Central Time-Of-Flight system (CTOF), and Silicon Vertex Tracker (SVT). The SVT is centered inside of the 5 T solenoid magnet.

2. Detector design and simulation

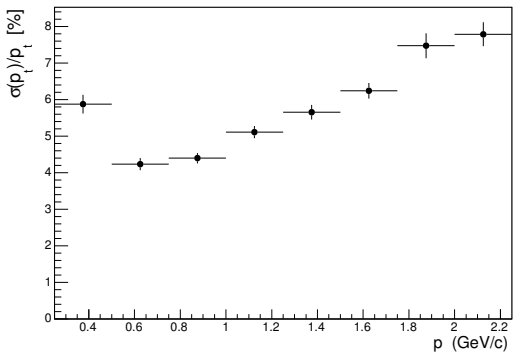

Figure 2: Simulated SVT momentum resolution.

SVT provides standalone tracking capabilities in the central detector region by measuring recoil baryons, large angle pions and kaons with tracking efficiency $\geq$ 90%, momentum resolution $\delta p_T/p_T \leq 5\%$, angular resolution for polar angle $\delta\theta \leq$ 10–20 mrad (within 35°–125°), and azimuthal angle $\delta\phi \leq 5$ mrad (within $\geq$ 90% of 2π). Tracks match up with hits in the CTOF for β vs. p measurement (particle ID). SVT allows reconstructing of detached vertices, e.g. $K_s \to \pi^+\pi^-$, $\Lambda \to \pi^- p$, $\Xi \to \Lambda\pi$ for efficient experimental program in strangeness physics. Results of GEANT simulation of SVT momentum resolution are presented in Fig. 2.

SVT comprises 33792 channels of silicon strip sensors in eight layers (four concentric polygonal regions that have 10, 14, 18, and 24 double sided modules). For 15 years of running the experiment on carbon target the estimated radiation dose for the sensors is 2.5 Mrad [2]. To minimize multiple scattering a unique module design with extra long 33 cm strips has been developed to reduce material budget to about 1.4% of radiation length per region (two silicon planes) for

normal incidence tracks, which is essential for low momentum tracking. All SVT modules are identical and there are no overlaps of adjacent modules. The SVT modules are cantilevered off a water-chilled cold plate, designed to remove the heat generated by the electronics, located only at one end of the module outside of the tracking volume. To facilitate the planned tracker upgrade the outermost SVT region has a separate cold plate and support tube. Both tubes are attached to the insertion cart. The cart hosts all detector services and is movable along the beam axis for easy maintenance.

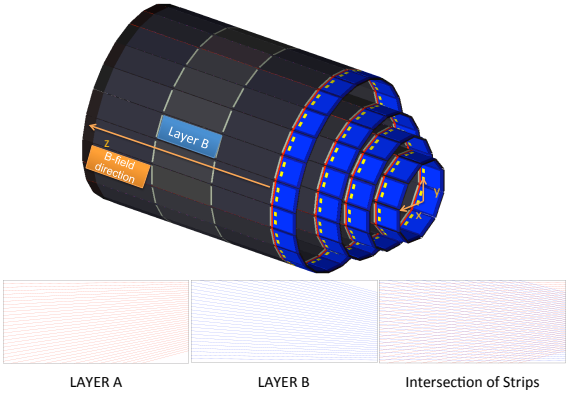

Figure 3: Side view of the SVT detector and strip layout for inner (A) and outer (B) layers.

The modules are mounted between the upstream and the downstream rings. For each region the upstream ring is attached to the cold plate. The cold plate and upstream ring are mounted to a mounting tube. The mounting surfaces of the upstream and downstream rings are machined in a single step to guarantee planarity. The rings of each region are independent from each other to prevent overconstraining the assembly. This design allows an entire region to be removed as a unit, rather than module by module. Downstream rings are made of PolyEther Ether Ketone (PEEK) [3]. The maximum deflection of a module due to gravity is 16 μm. The deflection of the downstream ring is less than 7 μm. The deflection of the entire SVT is 230 μm.

SVT uses single sided 320 μm thick microstrip sensors fabricated by Hamamatsu mounted on each side of the module. All modules have 3 types of sensors: Hybrid, Intermediate, and Far. Sensors are cut from 6 inch wafers, 2 sensors per wafer. All sensors have the same size, 112×42 mm. There are three daisy-chained sensors per layer (six per module). Each layer has 256 strips with linearly varying angles of 0°–3° (constant ϕ pitch of 1/85°) to minimize dead sensor area. First readout strip is parallel to the longitudinal axis of the module; the last readout strip has an angle of 3° with respect to this axis. Fig. 3 shows the side view of the detector and direction of the strips in the inner (A) and outer (B) layers of of the double-sided region. Regions are shifted along the beam axis to ensure angular coverage. Because of the constant ϕ pitch, the lengths of the readout strips of the modules vary from 0.5 cm to 33 cm. At the hybrid side the intermediate strip pitch is 78 μm and the readout pitch is 156 μm The strip-to-pitch ratio is 0.256 for all three types of sensors.

Sensors are mounted on a composite backing structure composed of Rohacell 71 core, bus cable, and carbon fiber (see Fig. 4). The carbon fiber skin is made from K13C2U fibers oriented in a quasi-isotropic (45/-45/0) pattern. It is co-cured with the bus cable, made from a Kapton sheet with 3 μm thick and 0.5 mm wide copper traces; one side provides high voltage to the sensors, a 6×6 mm copper mesh on another side grounds the carbon fiber. The Rohacell core under the hybrid board is replaced by a copper heat sink to remove ∼2 W of heat generated by the ASICs. At the downstream end of the module, the Rohacell core is replaced by a PEEK insert. The module

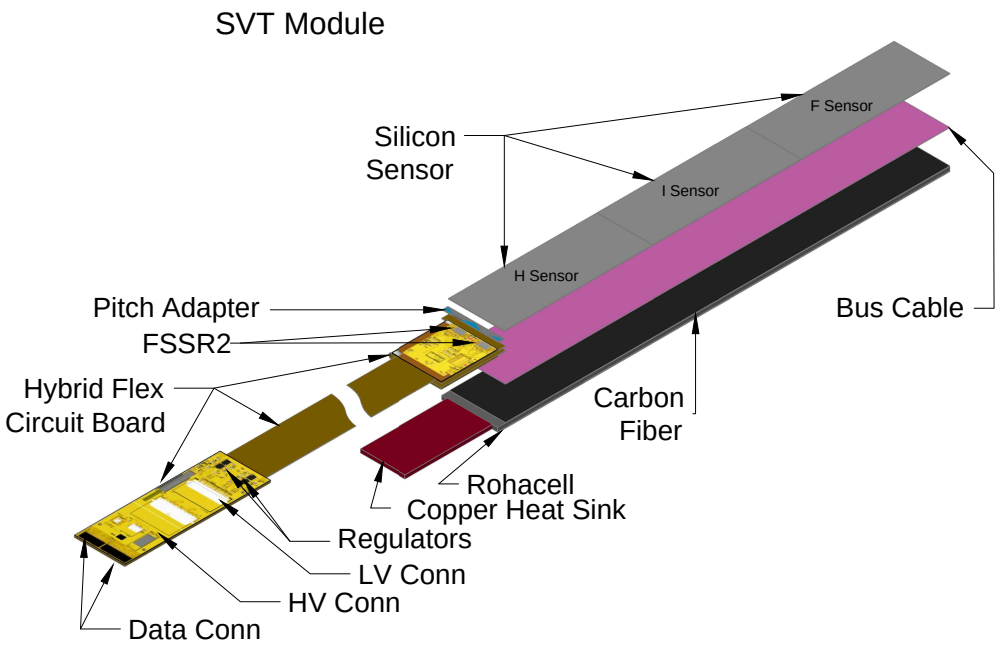

Figure 4: Layout of the SVT module.

has two mounting and two fiducial holes in the copper heat sink and one in the PEEK insert. After module is fabricated, position of these fiducial holes is measured with respect to the fiducial marks etched on the sensor. Sensors are aligned with respect to insert fiducials within few micrometers. Pitch adapter matches the 156 μm sensor readout pitch to the 50 μm FSSR2 bonding pad pitch. There are 512 channels per module read out by FSSR2 chips, mounted on a hybrid.

3. Readout system

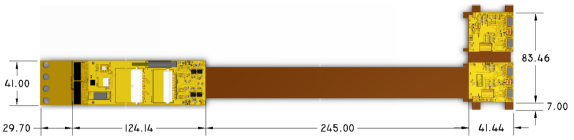

Figure 5: Hybrid Flex Circuit Board (HFCB).

A readout system which instruments both sides of a module with a single rigid-flex Hybrid Flex Circuit Board (HFCB), has been developed by Jefferson Lab (see Fig. 5) and fabricated by Compunetics Inc. The HFCB is located on the upstream end of the module. It hosts four FSSR2 ASICs, two on the top and two on the bottom side. The hybrid areas are connected by a 10 mm-long wing cable. The sensors, the pitch adapters, and the HFCB are glued with Huntsman TDR 1100-11 resin/hardener to both sides of the backing structure. The HFCB is wrapped around the backing structure with a wing cable (Fig. 6).

Data are transferred from the hybrid via the flex cable to the level one connect (L1C) board. The L1C has two high density Nanonics connectors for data and control lines, Molex Micro-Fit

9-pin connector for high voltage (∼85 V) bias to the sensors, and AMP Mini CT 17 pin connector for low voltage (2.5 V) power to the ASICs. There are 12 layers in rigid part and 6 layers in flex part. Control, data, and clock signals do not cross the ground plane splits. Clock signals are located on a separate layer. Guard traces are routed between output, clock, and power lines.

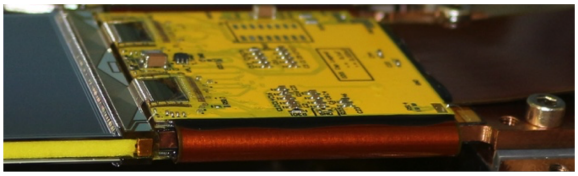

Figure 6: HFCB wrap

Separate planes are provided for analog and digital power. To reduce noise on these planes, regulators and bypass capacitors are added. High voltage filter circuits and the bridging of high and low voltage return lines are located close to the ASICs. Decoupling capacitors for power transmission are placed at transitions between flex and rigid materials. The HFCBs are routed through 10 mm radial slots in the cold plate. There are temperature and humidity sensors on each side of the HFCB for monitoring purposes.

The FSSR2 ASIC has been developed at Fermilab for the BTeV experiment [4]. The chip features a data-driven architecture (self-triggered, time-stamped). Each of the 128 input channels of the FSSR2 ASIC has a preamplifier, a shaper that can adjust the shaping time (50–125 ns), a baseline restorer (BLR), and a 3-bit ADC. The period of the clock called beam crossing oscillator (BCO) sets the data acquisition time. If a hit is detected in one of the channels, the core logic transmits pulse amplitude, channel number, and time stamp information to the data output interface. The data output interface accepts data transmitted by the core, serializes it, and transmits it to the data acquisition system. To send the 24-bit readout words one, two, four, or six Low Voltage Differential Signal (LVDS) serial data lines can be used. Both edges of the 70 MHz readout clock are used to clock data, resulting in a maximum output data rate of 840 Mb/s. The readout clock is independent of the acquisition clock. Power consumption is $\leq$ 4 mW per channel. The FSSR2 is radiation hard up to 5 Mrad.

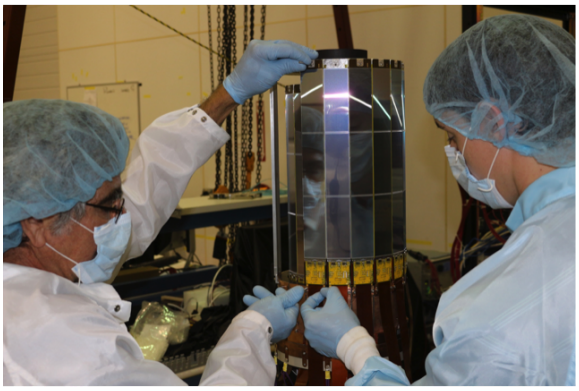

Figure 7: SVT assembly

Each of the four FSSR2 ASICs reads out 128 channels of analog signals, digitizes and transmits them to a VXS-Segment-Collector-Module (VSCM) card developed at Jefferson Lab. The event builder of the VSCM uses the BCO clock timestamp from the data word of each FSSR2 ASIC and matches it to the timestamp of the global system clock, given by the CLAS trigger. The event builder buffers data received from all FSSR2 ASICs for a programmable latency time up to ∼16 μs. The VSCM is set up to extract event data within a programmable lookback window of ∼16 μs relative to the received trigger. The trigger latency is expected to be ∼8 μs.

4. Detector integration and commissioning

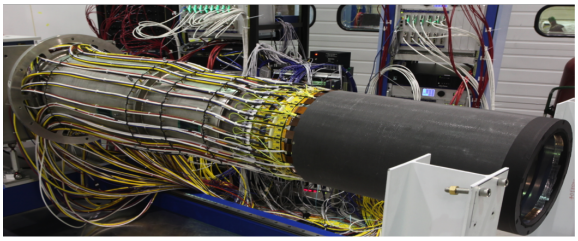

Figure 8: SVT after integration.

SVT modules were assembled at the Fermilab Silicon Detector Facility and tested at the Jefferson Lab. Barrel integration took place at the Jefferson Lab. Regions were assembled in sequence. The assembly was done in a vertical position on a granite table. Modules are mounted on the dowels inserted in the rings by holding the module by the two handling rods which are screwed into the inserts (Fig. 7). There are three fiducial points on each module, two on the upstream copper insert, and one on the downstream PEEK insert. During barrel assembly a survey of fiducial locations have been performed with precision of $\sim$20 μm using a FaroArm Quantum CMM. The shifts of survey positions from ideal geometry were taken into account by the alignment software. After assembling each region functionality of integrated modules was checked. When barrel assembly is complete, it was rotated to a horizontal position using a special fixture.

The mounting tubes of the inner and outer barrel were attached to the detector transportation cart, cable bundles routed along the support tubes and connected to the crates (see Fig. 8). Ambient conditions inside the detector are monitored by temperature and humidity sensors installed inside the downstream rings.

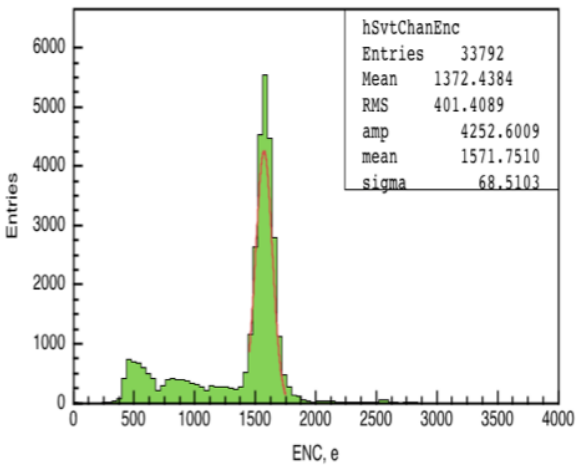

Figure 9: SVT channel noise.

Detector performance was tested by calibration procedures. Noise calibration accounts for the different strip lengths and pitch adapter layouts that affect the input capacitance of the preamplifier. Channel noise has linear dependence on the strip length from 400 electrons for the shortest strips. Defects known before the integration of the system were reestablished. 99.9% of channels are operational after detector integration. Noise behavior is found to be very good and well understood. No significant correlated noise has been observed between the channels of the same chip, between the chips of the same module or between the closely placed modules. Measured average Equivalent Noise Charge (ENC) of the SVT channels (see Fig. 9) is comparable with estimated contributions of different noise sources. The peak is $\sim$1600 electrons, the shoulder on the left side corresponds to the shorter strips. Channel noise allows setting a 3σ threshold at 20 keV level. Noise is found to be stable and the the dependence of the noise on the environmental temperature and humidity is small. Noise performance in the experimental hall was comparable with results

taken in the clean room. Detector response and full readout chain calibration was done with γ and β sources, cosmic muons and using the proton beam. Results of absolute gain calibration with γ source are shown in Fig. 10. Signal peak is in good agreement with expected position. Detector response to Minimum Ionizing Particles was about 24000 electrons which is what is expected for the 320 μm thick sensor.

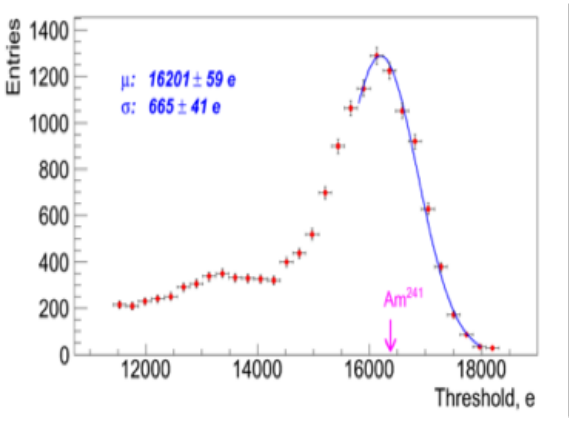

Figure 10: Signal from Am^{241} γ source.

Safe operation of the tracker is ensured by the dedicated monitoring of all important operation parameters including monitoring of low and high voltages and currents, temperatures and dew points. To avoid condensation the detector volume is purged with nitrogen. EPICS based slow control and monitoring system has been developed. Software and hardware interlocks continuously monitor critical system parameters. The performance and stability of the system is tested at various operation temperatures. Sensor leakage currents are below 300 nA with coolant at 7°C.

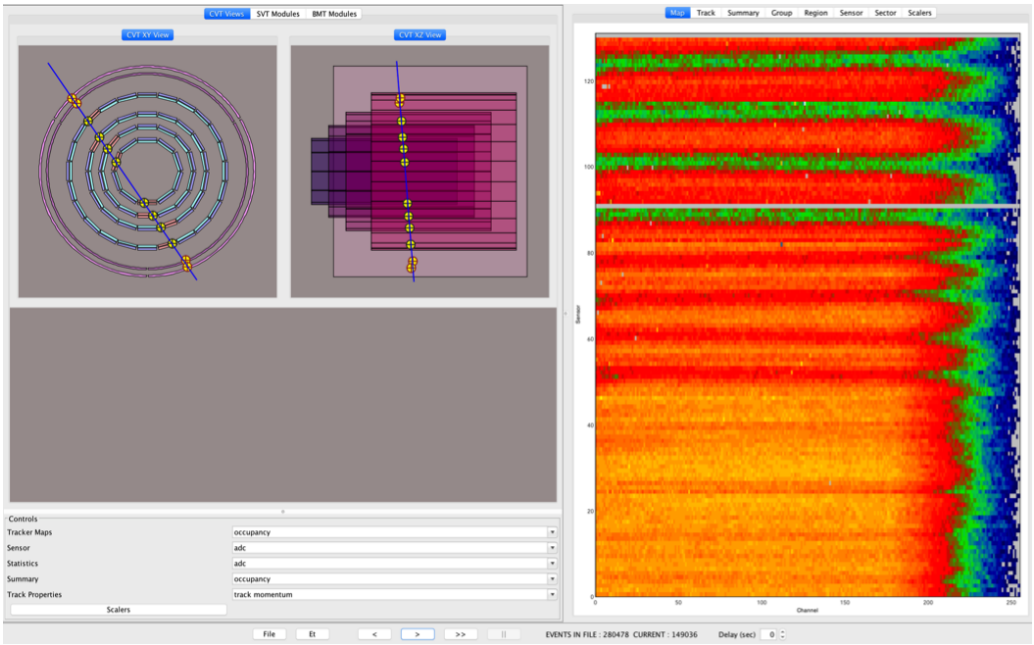

Figure 11: Online monitoring of the SVT

Java based data quality monitoring tools were developed to check the quality of the data both online and offline. Online SVT monitoring interface is shown in Fig. 11. The tools allow the shifter to check the status of the track reconstruction and performance of the individual modules. On the left side of the interface are shown the event display and the histogram selection menus. On the

right side there are canvases for the selected groups of histograms. The hit occupancy canvas is selected.

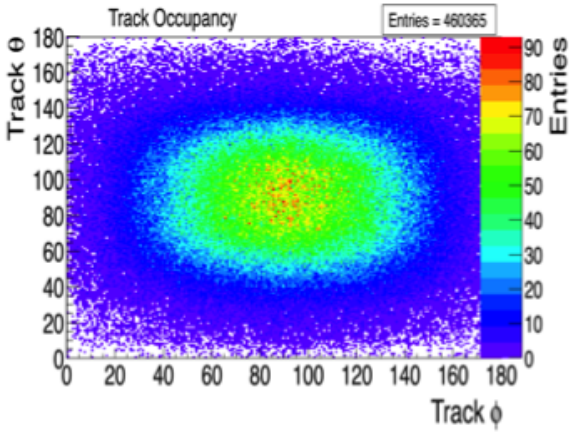

Figure 12: Angular distribution of the cosmic muons reconstructed in the SVT

Cosmic ray tests of the SVT have been used to test track reconstruction routines for the SVT, as well as establish correct readout, good noise performance, and full response for the entire detector. Cosmic data were taken in the standalone mode using the self triggering feature of the readout in coincidence logic. Angular distribution of the cosmic muons reconstructed in the SVT is shown in Fig. 12.

Validation of alignment procedures was performed on Monte Carlo simulation and cosmic data. Detector alignment procedure is using a least squares approach of a Millepede II algorithm [5]. The dependence of the residuals on the track parameters is explicitly taken into account. The alignment code uses the partial derivatives of the distance of closest approach (DOCA) taken with respect to the track parameters and the SVT geometry. This approach accounts for correlated shifts among the geometry parameters. Results of alignment correction for one of the SVT modules are shown in Fig. 13. Only shifts in the sensor plane were taken into account in the alignment procedure for this plot.

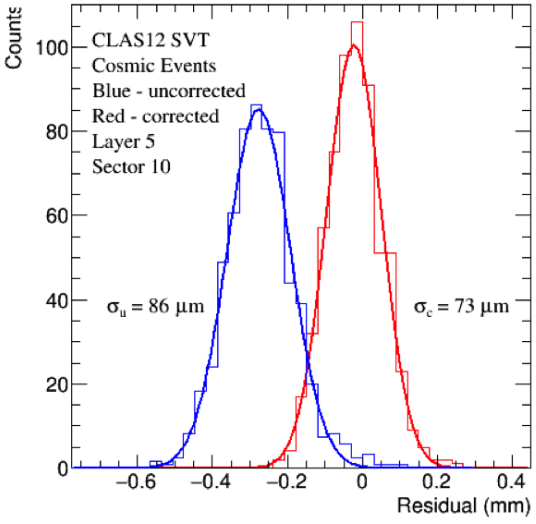

Figure 13: Alignment of the SVT module.

References

[1] CLAS12 Technical Design Report, 2008. URL: https://www.jlab.org/Hall-B/clas12_tdr.pdf

[2] CLAS12 Silicon Vertex Tracker Technical Design Report, 2012. URL: https://www.jlab.org/Hall-B/cvt/svt/doc/TDR4.pdf

[3] M.A. Antonioli et al. "Performance of the CLAS12 Silicon Vertex Tracker modules", Nucl. Instr. and Meth., A732 (2013) 99-102.

[4] R. Yarema, J. Hoff, A. Mekkaoui, M. Manghisoni, V. Re, P.F. Manfredi, L. Ratti and V. Speziali, "Fermilab silicon strip readout chip for BTEV", IEEE Trans. Nucl. Sci. 52(3), 799 (2005).

[5] V. Blobel. "Software alignment for tracking detectors", Nucl. Instr. and Meth., A566 (2006) 5-13.