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# The phase 1 upgrade of the CMS pixel detector

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The CMS collaboration is building a replacement for the pixel detector that will be installed in the extended end of year shutdown 2016-2017. This contribution reviews the motivations for the upgrade, the technological choices made, the status of the construction of this new detector and the plans for installation and commissioning.

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## 1. Introduction

The innermost layers of the current CMS [1] tracker are built out of pixel detectors arranged in three barrel layers (BPIX) and two forward disks in each end cap (FPIX). The pixel detector provides space points that are used as seeds in the track finding and that are crucial for resolving track ambiguities in high occupancy environments like the core of jets and for tagging products of the decay of heavy flavor quarks. The original CMS detector was designed to operate at a maximum instantaneous luminosity of $1 \times 10^{34}\,\mathrm{cm}^{-2}\,\mathrm{s}^{-1}$, a value that the LHC has already exceeded in 2016, with further increases foreseen in the coming years. The limited size of the buffers on the pixel readout chips and the limits in the readout bandwidth introduce a dynamic inefficiency that results in a loss of tracking efficiency and of the rejection power of b-tagging algorithms for events with a large number of collisions per bunch crossing (high pileup). To overcome these limitations the CMS collaboration has started in 2012 the construction of a new pixel detector [2]. The new detector features new digital readout chips with larger buffers and increased data transmission bandwidth to overcome the main limitation of the current detector. Despite the addition of one tracking layer both in the barrel and in the end cap, the total amount of material transversed by tracks is reduced in comparison to the current detector. With the installation of the new detector the tracking efficiency, the b-tagging performance, and the rate of fake tracks are expected to improve even at a luminosity of $2 \times 10^{34}\,\mathrm{cm}^{-2}\,\mathrm{s}^{-1}$ in comparison to the performance of the current detector at the design LHC instantaneous luminosity. Additional benefits arise from a reduction of the radius of the first tracking layer from 4.4 cm to 2.9 cm following the installation of a new beam-pipe with reduced radius during the 2012-2014 shutdown. The addition of one more tracking layer will also compensate for possible losses of efficiency in the silicon strip tracker that may occur as that detector continues to operate until 2023, when the entire tracker is slated for replacement. Most of the services for the upgraded pixel detector (power distribution, readout and control optical fiber plants) are kept from the original detector, in order to reduce the time needed for installation. The addition of one tracking layer and the increase of the outer radius covered by the pixel detector result in a doubling of the total number of channels, from 48 M to 79 M for BPIX, and from 18 M to 45 M for FPIX. A comparison of the geometries of the original detector and of the phase 1 upgrade is shown in Fig. 1. The barrel layers are numbered 1 to 4 starting with the innermost one and similarly the disks are numbered 1 to 3 starting with the one closest to the interaction point.

This review is organized as follows: first the changes in the module construction, including the new readout chips, are discussed. Then the modifications to the mechanical supports are described. These include the use of a new $CO_2$ cooling system and the placement of the electronic readout boards at larger rapidities, that together contribute to an overall reduction of the material in the pixel detector. Then the readout, control, and power distribution chain is reviewed. Finally the construction status and the plans for testing, installation and commissioning are discussed.

## 2. Modules

Like for the original detector the BPIX modules are built out of a $n^+$-in-n sensor that covers an area of $16.2 \times 64.8\,\mathrm{mm}^2$ comprising 66,560 pixels, each with size $100\,\mu\mathrm{m} \times 150\,\mu\mathrm{m}$, read out via sixteen readout chips (ROCs). Each sensor pixel is connected in the bump bonding process



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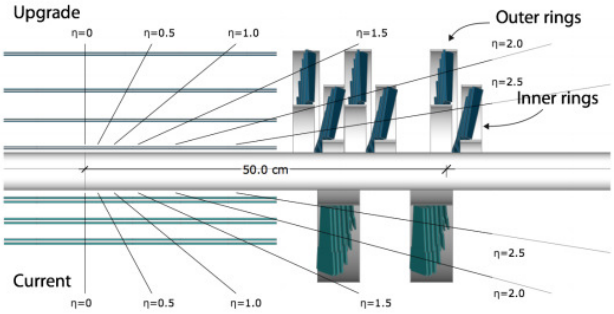


**Figure 1:** Comparison of the azimuthal cutouts of the current (bottom) and upgraded (top) CMS pixel detectors.

to a readout channel on the ROC via a solder bump previously deposited on the ROC surface after metallization of the pads. The solder bumps are then reflown to complete the interconnection of the sensor with the ROCs. While for the original detector the FPIX modules were built in different sizes and were read out with a number of ROCs between 2 and 10, a geometry identical to that of BPIX is now used. Neither the sensor technology nor the fabrication technology for the readout chips (0.25 $\mu$m CMOS) have changed since the original detector, given that both have been demonstrated to be able to sustain the radiation dose that will be collected until 2023. Thin flexible printed circuits (high density interconnects, HDIs) are glued on top of the sensor, and connected via wire bonds to the readout chips (for control and readout purposes) and to the sensor (to provide the bias voltage). Each HDI routes the data from the ROCs to one or two token bit manager (TBM) ASICs that organize the readout and aggregate and format the data in a single output data stream (TBM08 used for layers 3 and 4 of BPIX and all FPIX disks) or two output data streams (TBM09 used for layers 1 and 2 of BPIX, two TBM09 chips are used in layer 1). The data from 4, 8 or 16 ROCs (based on the occupancy of each pixel layer, 4 for BPIX layer 1, 8 for BPIX layer 2, and 16 for the remaining detectors, respectively) is shipped off the module at 320 MBit/s through 4/5 bit encoded data streams. This represents a gain of a factor eight in the data throughput compared to the original detector, where the readout bandwidth was limited to 40 MBit/s. The BPIX and FPIX modules differ mostly for the HDI technology and the cable used for the readout. Different vendors and different types of bump bonding have been used for the construction of the detectors, but similar quality and yields have been obtained. The total number of modules in the new pixel detector is 1,856, of which 1,184 are in BPIX and 672 in FPIX.

The ROCs are based on an evolution of the readout chip used in the current detector [3], using a similar zero-suppressed and column drain architecture in the chip used for layers 2-4 of BPIX and for FPIX, while a completely new readout architecture is used for layer 1 of BPIX that needs to sustain higher readout speeds. The version of the ROC used for layers 2–4 of BPIX and for FPIX comprises 80 rows and 26 double columns. To increase the bandwidth, the 40 MHz analogue readout has been changed to 160 Mbit/s digital readout, requiring the addition of an 8 bit ADC. The data streams from two banks of ROCs are merged in the TBM to achieve the module data transmission rate of 320 MBit/s. The buffer depths of the hit and time-stamp buffers have been increased from 32 to 80 and from 12 to 24, respectively. Furthermore an additional readout buffer



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has been added. The cross-talk inside the ROCs has been reduced and the comparator in each pixel cell improved, leading to a reduction of the threshold from about 3200 electrons to about 2000 electrons. This increases the efficiency and the lifetime of the detector under irradiation, given that clusters with total smaller charge can be reconstructed, and also leads to an improvement of the intrinsic position resolution of each pixel module. This new readout chip has been characterized in beam tests, where it ran stably with a threshold as low as 1800 electrons [5]. The ROC was also tested after irradiation with 23 MeV protons to doses of 0.6 MGy and 1.2 MGy, corresponding to the doses expected in layer 2 and 1 after integrated luminosities of 500 $fb^{-1}$, in excess of the integrated luminosity expected until 2023. Simulation of the readout speed and efficiency measurements in high occupancy environments indicate that the dynamical inefficiency of the ROCs is below 2% for layer 2 of BPIX, but also that this chip would have a too high inefficiency if installed in the innermost layer of BPIX.

The ROC used for layer 1 of BPIX, called PROC600, uses a new readout architecture where clusters of $2 \times 2$ pixels are formed in the double column and transferred in a single step, instead of transferring individual pixels [6]. This new dynamic cluster column drain mechanism, coupled with the increase in the number of double columns that can be simultaneously transferred to the ROC periphery, results in an increase of the maximum rate that can be sustained by the layer 1 BPIX modules with a limited ($< 2\%$) inefficiency to approximately 600 MHz/$cm^2$, compatible with the expected rates in CMS.

## 3. Mechanical supports

The biggest changes in the mechanical support structures for both BPIX and FPIX are the use of a two phase $CO_2$ cooling system and the displacement of the service electronics from inside the volume covered by the silicon strip tracker ($|\eta| < 2.5$) to larger rapidities. The heat removal in a two phase $CO_2$ cooling system is more effective compared to that of a single phase system using $C_6F_{14}$ that was used in the current pixel detector. This allows the use of smaller pipes resulting in a reduction of the overall material. Further material reduction is achieved in FPIX by building the disk supports with carbon based compounds instead of aluminum as in the original detector.

The BPIX modules are connected to the high thermal conductivity support strips in which the cooling pipes are embedded via ceramic supports made of $Si_3N_4$. The support strips are held by end flanges that are built out of a sandwich of carbon fiber and Airex foam, with the exception of the end flange for layer 4 that is built entirely out of carbon fiber. The FPIX modules are mounted on blades built out of thermal pyrolitic graphite (TPG) that are supported by rings built out of graphite with an external carbon fiber reinforcement. The FPIX cooling pipes run inside the graphite rings. Both in the case of BPIX and FPIX simulation and measurements on prototypes indicate a maximum temperature difference between the coolant and the module of at most 10 °C (FPIX) and 12 °C (BPIX). This should ensure that the FPIX and BPIX modules are kept at temperature below -10,°C, when the $CO_2$ cooling plant is operated at a temperature of -23 °C, thus increasing the lifetime of the detector under irradiation.

The BPIX modules with their support strips and the corresponding end flanges form two half shells for each layer. For FPIX the modules mounted on the blades and their suppor rings are organized in sets of three inner and three outer half disks. The BPIX shells and the FPIX disks are



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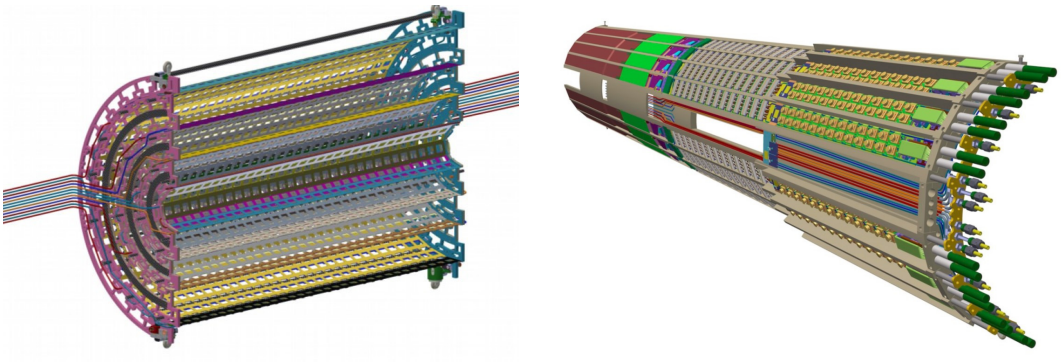

**Figure 2:** Left: CAD model of the BPIX detector support structure, showing four detector layers, supported by end flanges. The cooling pipes are also depicted. Right: CAD model of the BPIX supply tube. The interaction point is to the left. The most important components visible are (left to right): module cables (pink), opto-hybrids (green), and DC-DC converters (green/yellow).

supported by two sets of half cylinder supports, called supply tube in the case of BPIX and service cylinders in the case of FPIX. These supports house the readout, control and powering electronics boards that are cooled by the same $CO_2$ cooling system used for cooling the sensors and the ROCs. For BPIX the supply tubes are made of carbon fiber plates close to the interaction point, IP, and of carbon fiber / Airex foam sandwich further away from the IP. For FPIX the service cylinder are made of a rear part that is made of carbon fiber sheets separated by ribs also made of carbon fiber, while the section closest to the IP, where the FPIX disks are mounted, is made of a corrugated section of thicker carbon fiber. CAD drawings of the BPIX half shells and of one supply tube, and of the FPIX half disks and half cylinder are shown in Figs. 2 and 3, respectively.

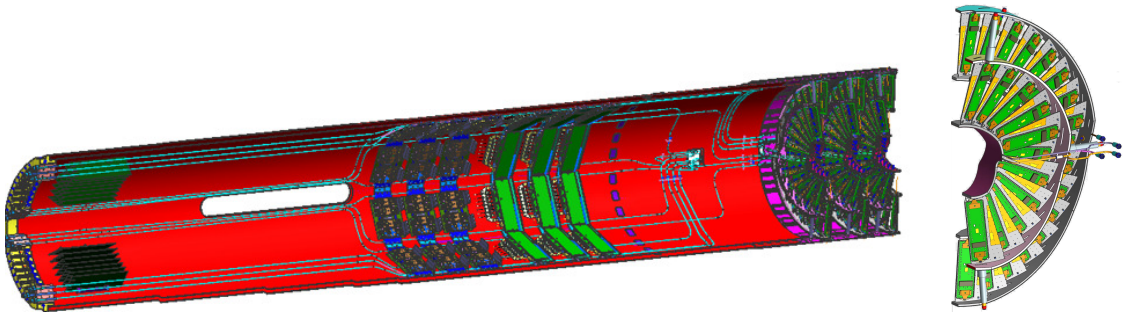

**Figure 3:** Left: CAD model of the FPIX half cylinder with the interaction point on the right. The various components visible are (right to left): the half disks, the port cards (green) with the opto-hybrids attached, the DC-DC converters with their cooling bridges (orange/blue). Also visible is the layout of the cooling lines in the service cylinder. Right: CAD model of one half disk comprising an inner and an outer section with the modules depicted in green.

## 4. Electronics and readout

The readout, control and power systems are mounted in the supply tubes and in the service



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cylinders. While the basic components used by BPIX and FPIX are identical, the implementation in the two systems is entirely different. BPIX uses long flexible printed circuit boards inserted in slots in the supply tube to house all the electronics, while FPIX uses smaller boards that are connected by cables. In both cases the electronics is moved to large rapidities, $|\eta| > 2.5$, to reduce the amount of material seen by the tracker. The control signals (clock, trigger, detector configuration) are transmitted from the electronics cavern via optical fiber and distributed to each individual module. The signals from the modules are converted from electrical to optical using opto-hybrids that are mounted inside the supply tubes and service cylinder. Each individual module is read out via four, two or a single readout fiber for BPIX layer 1, BPIX layer 2, and the remaining detector modules, respectively. The fiber plant used for both the control and the readout of the module will be almost entirely re-used from the current detector, and only the part running from the PP0 bulkhead (just outside the supply tubes / service cylinders on the front face of the end cap calorimeters) to the top of the CMS detector will be replaced during the 2016/2017 shutdown.

The total amount of power required to operate the new pixel detector is significantly increased relative to that used for the current one, because of the increase in the total number of channels (the power requirement of individual channels has remained essentially constant). To avoid increasing the number of power cables entering the pixel detector a DC-DC conversion power system is used [7]. The power supplies of the original detector are being modified to supply a larger voltage (10 V) at a lower current. To obtain the voltages required to operate the module (2.4 V for the analog part of the ROCs, and 3.3-3.5 V to operate the digital part of the ROCs, taking into account the ohmic losses on the modules' cables), DC-DC converters are used inside the supply tubes and service cylinders. The DC-DC modules are a custom development based on the FEAST2 ASIC [8] from CERN, achieving a total efficiency above 80% in the conversion.

The DC-DC converters and the opto-hybrids are cooled by the same pipes used for cooling the modules and provide enough heat to initiate the transition from a fully liquid phase to the two-phase system that is needed for efficient heat removal from the modules.

The back end of the readout and control electronics is based on the use of new $\mu$TCA boards based on the same motherboard design used for the upgrade of the trigger, control and distribution system (TCDS) system, the FC7 board [9]. For the readout boards (FEDs) a new mezzanine is used that can read out 24 channels. For the distribution of the clock, trigger, and detector configuration signals (FEC boards) the same mezzanine card used for the TCDS system is used. New firmware has been developed for both the FED and the FEC boards. A total of 108 FEDs and 20 FECs housed in 12 $\mu$TCA crates are needed to control and read out the upgraded pixel detector. The FED and FEC firmware and the entire readout, control, and power chains are being exercised in system tests based on increasing number of channels, reaching up to a total of 168 channels in the case of the FPIX system test. A smaller system, called pilot system, was installed in CMS at the end of the 2014 shutdown. This system, based on 8 FPIX modules with prototypes of the entire readout chain, has provided [10] invaluable information for the finalization of the boards design and is being used to ensure that the FED and FEC firmware is capable of handling the 100 kHz trigger rate expected during data taking.



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## 5. Construction status

The construction of the barrel and forward part of the phase 1 CMS pixel detector is distributed among multiple institutions in Europe (BPIX) and the US (FPIX). PSI in Switzerland and Fermilab in the US serve as centers where the complete parts of the detectors (the two halves of BPIX and the four half cylinder of FPIX) are assembled and tested prior to their transport to CERN.

At the time of the conference (September 2016) the module construction and qualification [11, 12] for barrel layers 2-4 was complete, with the assembly and testing of additional spare modules for layer 2 still progressing, while the construction of the modules for the innermost barrel layer using the new PROC600 readout chip had just started. The construction and qualification of the modules for the forward disk was almost complete. At the time of the submission of these proceedings (November 2016) the module construction is essentially complete, with just the qualification of the modules for the innermost barrel layer still ongoing.

**Figure 4:** Photo of three FPIX half disks installed in the first complete half cylinder.

The construction of the mechanical supports (disks and half cylinders) for the forward disks was completed in early September, and all the electronics was installed in the service cylinders at the beginning of October. The installation of the modules on the half disks for FPIX was completed at the end of October. Three of the four FPIX half cylinder were fully assembled at Fermilab by installing the half disks inside the half cylinder, performing all the electrical and cooling connections. The three half cylinders were tested at Fermilab (Sect. 6 below), then disassembled removing the disks from the half cylinders, prior to their transport to CERN. For the last one the disks' insertion in the half cylinder will be performed only at CERN. Two complete half cylinders were delivered to CERN and reassembled with all the half disks in mid-October, with a plan for transporting to CERN and reassembling the remaining two half cylinders by the middle of November. A photo of three half disks (split into an inner and an outer part) installed in the first complete half cylinder is shown in Fig. 4.



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At the time of the submission of these proceedings the construction of the shells supporting the BPIX modules is nearing completion and modules have already been installed on three half shells for layers 2-4. The construction of the supply tube mechanical supports is progressing and one of the four supply tubes (two on each side of the BPIX barrel half shell) has been completed with the installation of all the service electronics and is currently under test. It is expected that the installation of the modules on all the half shells for BPIX will be completed by the end of November, and that the first half of the detector (the four half shells for layers 1-4 of the barrel and the two supply tubes on either side of the barrel) will be assembled by the end of November. The second half of the detector will be ready by the end of December. Photos of the first layer 2 half shell with all its modules installed and of the first complete supply tube are shown in Fig. 5.

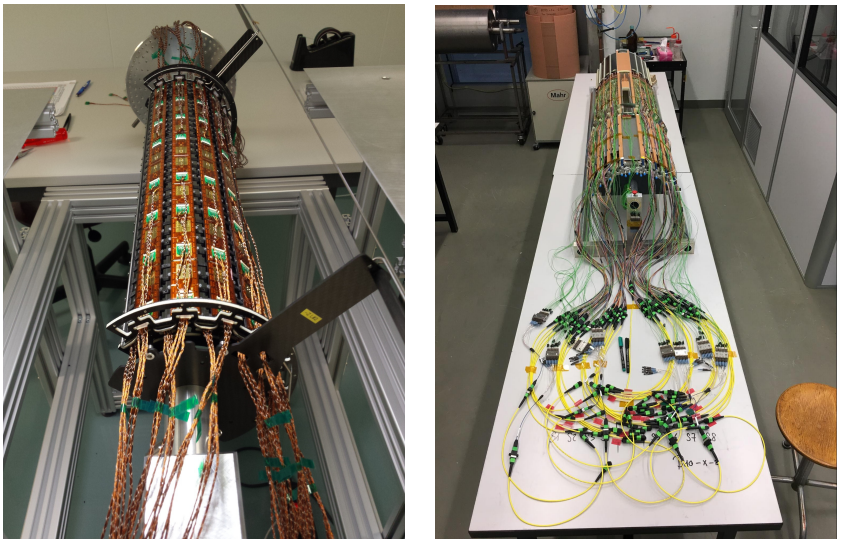

**Figure 5:** Left: Photo of the first complete layer 2 BPIX half shell with all its modules installed and cabled (October 2016). Right: Photo of the first complete BPIX supply tube, with all the readout, control, and power electronics installed (November 2016).

## 6. Testing, installation and commissioning

Different approaches are used for the testing of the complete BPIX and FPIX detectors prior to their installation. Each FPIX half cylinder is tested in conditions as close as possible to those after the installation in CMS, first at Fermilab and then at CERN. After the installation of disks into the half cylinder all electrical, optical, and cooling connections are made, and pressure and leak tests for the cooling systems are performed. At that point the half cylinder is tested with the final $\mu$TCA readout system. First the channel mapping is checked and light levels in the pixel opto-hybrids are established. Then each individual module is timed in, establishing appropriate delays for the readout relative to an external trigger, and phases are set for each individual TBM core. Using the initial calibrations obtained with the digital test boards as starting point, functionality checks are repeated on each module. Then sensor leakage current, pixel by pixel noise and bump bonding quality are checked again to identify modules that may have been damaged during the



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installation of the disks into the half cylinders and / or during the transport to CERN. Damaged modules can be replaced at this point, although the most commonly encountered problem is that of loose connections of cables or of electronic components. All these tests are performed first at room temperature and then with the $CO_2$ cooling temperature set to -20 °C. At Fermilab only one entire half disk was read out, while at CERN enough readout and power channels are available to perform these tests on one entire half cylinder. Sufficient time will be available in December and January to perform full calibrations of the half cylinder at the target operating temperature of -23 °C.

For BPIX the initial tests of the readout chain are performed by moving the connections of a reference set of modules through all the channels of a supply tube, performing a sequence of tests very similar to the one described above for FPIX. The supply tube is first tested at room temperature and then cold. After the connection of the supply tube to a set of half shells the same tests can be performed by reading out only one sector at a time at room temperature, due to the limitations introduced by the available cooling power at PSI and by the number of readout electronic channels. These tests will be repeated, possibly also at the target operating temperature of -23 °C, after the transport of the detector to CERN at the beginning of February 2017.

The current pixel detector will be removed in the middle of January 2017 and in the following weeks part of the services (from the PP0 bulkhead to the top of the detector) will have to be replaced. The original cooling lines will have to be replaced to allow for the transition from $C_6F_{14}$ cooling to $CO_2$ cooling and optical fibers in the same region will also be replaced. The new BPIX and FPIX detectors will be installed at the end of February over a period of two weeks. Initial tests of the detectors will be performed at room temperature and only after the sealing of the water vapor barriers and the closure of the CMS end caps the detector will be operated cold. Full calibrations of the new pixel detector will be performed prior to having circulating beams in the LHC, and cosmic data will also be collected, which could help with the alignment of the forward disks along the beam direction. Once collisions are again established in the LHC, few millions of minimum bias events from the first useful store will be required for establishing an overall timing delay for the trigger, and a similar amount of data from the following store will be needed to perform an initial alignment of the entire pixel detector at a quality level sufficient for using the tracking in the high level trigger. Further refinements of the alignment will require more data and possibly additional cosmic ray data. Overall it is expected that the installation of the new detector will entail only a minimal loss of high quality physics data, which will be compensated with time with all the performance gains compared to the current detector.

## 7. Conclusions

The construction of the phase 1 CMS pixel upgrade is nearing completion and the detector is expected to be ready for installation during the extended end of year shutdown 2016–2017. The new detector will overcome the limitations of the current one at the highest LHC instantaneous luminosities and provide improved tracking performance.

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