PROCEEDINGS OF SCIENCE

The ATLAS tracker Pixel detector for HL-LHC

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The high luminosity upgrade of the LHC (HL-LHC) in 2026 will provide new challenges to the ATLAS tracker. The current Inner Detector will be replaced with an all-silicon tracker which will consist of a five barrel layer Pixel detector surrounded by a four barrel layer Strip detector. The expected dense tracking environment and high radiation levels require the development of higher granularity radiation hard silicon sensors and a new front-end readout chip. The data rates require new technologies for high bandwidth data transmission and handling. The current status of the HL-LHC ATLAS Pixel detector developments as well as the various layout options are presented in this paper.

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1. Introduction

The LHC accelerator at CERN is providing a detailed insight for the study of the fundamental nature of matter at the energy frontier. Since its start-up in 2009, it is delivering collisions at increasing energy and interaction rate, and reached 13 TeV in the pp center of mass energy in 2015 and an instantaneous luminosity of 1.37×10^{34} cm^{-2} s^{-1} in the 2016 data-taking period. The LHC scientific program spans over more than 20 years and, as it is shown in Figure 1, two main long shutdown periods are still foreseen before reaching the ultimate instantaneous luminosity of the High Luminosity LHC (HL-LHC): Long Shutdown 2 (LS2) in 2019/20 and Long Shutdown 3 (LS3) starting at the end of 2023. The accelerator plans require major detector upgrades, referred to as Phase-I and Phase-II, that will take place during these shutdown periods.

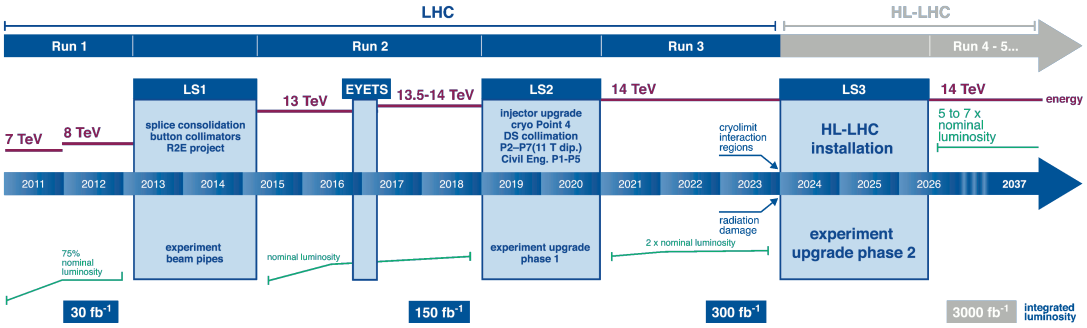

Figure 1: LHC baseline program.

With a nominal (ultimate) luminosity of $\mathscr{L} = 5 \times 10^{34}\text{cm}^{-2}\text{s}^{-1}$ ($\mathscr{L} = 7.5 \times 10^{34}\text{cm}^{-2}\text{s}^{-1}$), an integrated luminosity of 3000 fb^{-1} and an average $\langle\mu\rangle$ =140 (200) inelastic pp collisions per beam-crossing, the HL-LHC will present an extremely challenging environment to the ATLAS experiment, well beyond that for which it was designed. ATLAS has foreseen a staged approach for the upgrades of the calorimeters, muons spectrometer and the trigger and DAQ systems using Phase-I as an intermediate step. The current Inner Detector however will be replaced during LS3 with a completely new all-silicon tracker to maintain similar tracking performance as the current one in a high occupancy environment and to cope with the increase of approximately a factor of ten in the integrated radiation dose with respect to Phase-I [1, 2]. New technologies will be used to ensure that the system can survive this harsh radiation environment, with the radiation level exceeding 2×10^{16} $\text{n}_{\text{eq}}/\text{cm}^2$ and 17 MGy in the innermost pixel region, and also to reduce the scattering material. The new read-out scheme will allow the implementation of a track trigger contributing to the major improvements in the ATLAS online data selection capabilities.

In Section 2 the new ITk Pixel detector is presented, starting from an overview of the ITk layouts currently under study, with special emphasis on the Pixel barrel and forward regions; Section 3 describes the pixel modules and Section 4 illustrates the timeline towards the Technical Design Report and the production and integration of the detector.

2. ITk Layout

The layout of the ITk tracker has evolved from a proof of principle concept [1] to a more

realistic design, taking into consideration tracking performance, cost, ease of construction and installation. It is an all-silicon detector covering a pseudorapidity $|\eta|$ range up to 4, with pixel sensors in the innermost radii, surrounded by a Strip detector extending up to the solenoid inner bore.

The ITk pixel system extends out to a radius of 345 mm, it has five barrel layers arranged in cylinders around the beam axis, three or four sets of rings according to the η coverage and several pixel hits in the forward direction to allow tracking in that region. The total active surface of the Pixel detector is $\sim$14 m^2, i.e. roughly an order of magnitude larger than the current Pixel detector. The innermost part of the Pixel detector is designed to be replaceable (the plan is to replace it at least once during the HL-LHC operation).

The Pixel barrel is followed by two short-strip layers of paired stereo modules then two long-strip layers of paired stereo modules. The outer active radius of the Strip detector is moved as far outside as the technical constraints allow to maximize momentum resolution. The forward regions are covered by six strip discs on each side. The strip system covers $\pm$2.5 units of pseudorapidity.

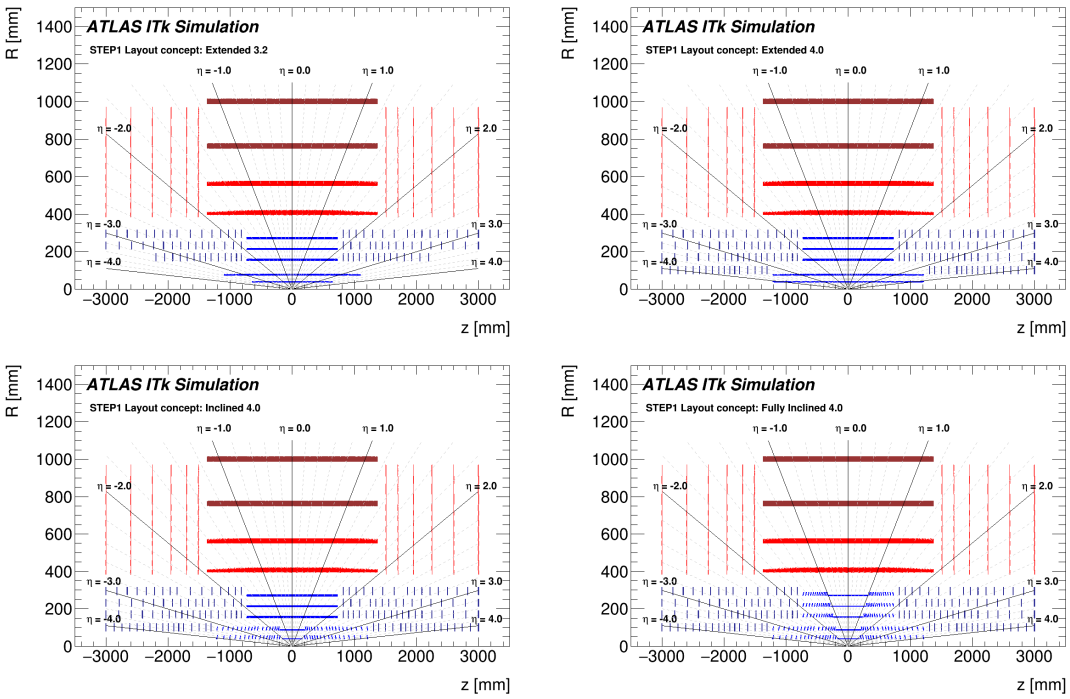

Figure 2: Longitudinal views of the ITk layout options: the horizontal axis is the axis along the beam line with zero being the interaction point; the vertical axis is the radius measured from the interaction point. Top Left: Extended layout at η 3.2; Top Right: Extended layout at η 4.0; Bottom Left: Innermost Inclined layout; Bottom Right: Fully Inclined layout. [3]

The ITk community is currently evaluating four layouts, shown in Figure 2. The radii of each barrel layer and the z positions of the discs in the end-caps were optimised for momentum resolution and track finding efficiency, providing η coverage up to 4.0 (or 3.2) with at least 9 space points. While the strip and the forward pixel regions are the same in all the layouts, different concepts are studied for the barrel part of the Pixel detector: an extended long barrel is compared to a layout in

which sensors are inclined, either in the innermost layers only or in all the layers.

2.1 ITk Pixel Barrel

In the inclined options, either used in the innermost two barrel layers only or in all the barrel layers, particles originating from the interaction point cross the pixel sensors at an angle close to normal, thus minimizing interactions with material. This option can reduce the number of sensors needed, even allowing multiple hits per layer in order to reconstruct the incident angle with precision. However, since for the inclined sensors the support surface is not parallel to the cooling lines, it has been necessary to demonstrate the capability to cool down the detector. Two local support designs have been developed: SLIM, shown in Fig. 3 left, and Alpine. Prototypes have been built and tested. Mechanical and thermal tests have been performed and have demonstrated that there is a viable solution to support the inclined sensors satisying all the requirements.

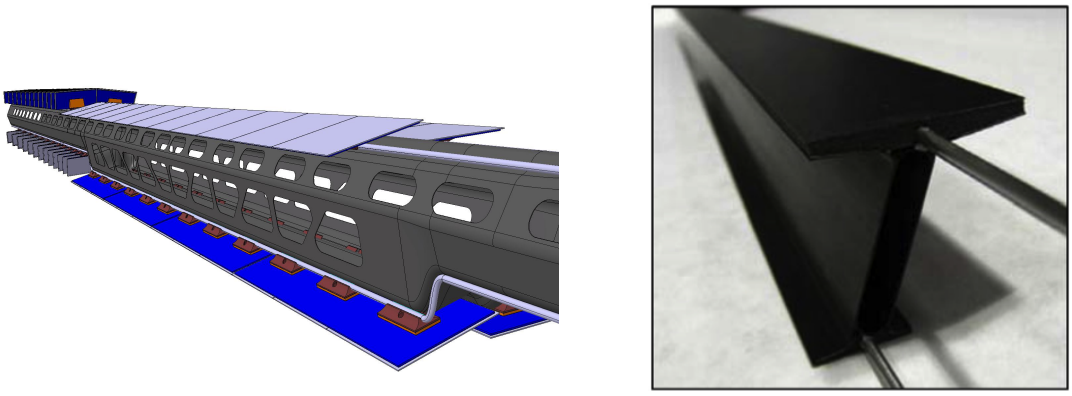

Figure 3: Left: SLIM design for the inclined layout. Right: Pictures of an I-Beam stave: modules are loaded on both sides (top and bottom). [2]

In the extended option, all the sensors are positioned on cylindrical surfaces around the beam axis. This is a "more traditional" approach, although in the innermost barrel layers the supports should be very long, up to 2 meter length. This implies that the cluster size in the forward region is rather large and it may be exploited to reconstruct tracks segments and constrain the track fit. A huge effort is on-going to solve the critical software aspects such as cluster size robustness in presence of broken clusters and optimal use of the long clusters in the track seeding and reconstruction. Two mechanical designs are being developed to support modules of the extended barrel. The first one, so called I-Beam, achieves the low-mass requisite by supporting two layers in a single discrete structure, see Fig. 3 right. Modules are placed on both flanges of the structure. The heat generated by the modules is collected by the flange whose core is low-mass thermally conductive carbon foam. The heat reaches a titanium pipe having a wall thickness of about 120 μm directly bonded to the carbon foam. There the boiling CO_2 removes the heat at low temperature. Although the pipe wall thickness is relatively thin, the titanium density is such that its contribution to the material budget is not negligible. As a consequence, the replacement of titanium with other material has recently been considered. One prototype is the so-called Carbon Stave where the metal pipe is replaced by a carbon pipe braided dry on a mandrel and passed through an impregnating dye.

2.2 ITk Pixel Forward

The Pixel forward local support is developed through a novel approach. Usually the forward region is covered by disc-like structures on which the sensors are arranged in petals at fixed z (as in the current Inner Detector or in the LoI [1]). A ring system is an elegant solution to get more flexibility and to maximise the physics performance. In this approach, modules are placed over narrow round supports, so-called rings. Rings are then assembled in four cylindrical layers. As each ring in a layer can be placed independently from the sensors z position loaded in the other layers, the rings in different layers line up to provide a better coverage up to $\eta = 4$. Figure 4 top shows the ring concept as implemented in the ITk forward region.

Each ring is built out of two half-rings, for ease of construction. The half-ring, see Fig. 4 bottom, is a sandwich of carbon laminates where the core is carbon foam. In its neutral plane a titanium cooling pipe and the service bus tape are placed. The heat generated by the modules is taken away by the CO_2 evaporative system. The bus tape distributes the electrical services to the modules which are alternatively bonded to the two carbon face-plates allowing an adequate sensor overlap.

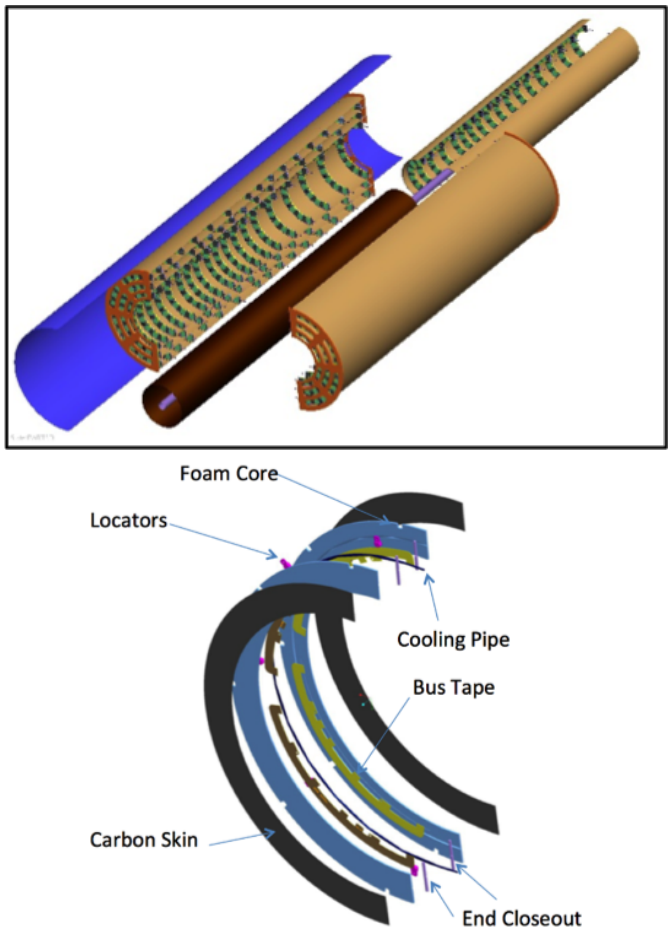

Figure 4: Top: Ring endcap concept: modules (shown in green) are mounted on half-rings which are in turn mounted inside cylindrical layers (light brown). Bottom: Exploded view of the ring mechanical assembly. [2]

3. Modules

The basic electrical unit of the Pixel detector is a module. The baseline module concept for the ITk Pixel detector is the well proven hybrid pixel detector which uses a sensor and the read-out chip bump bonded to each other. Other concepts like monolithic CMOS pixel detectors are being investigated especially for the outer layers.

There will be few types of modules:1-chip or 2-chip-modules for the innermost layers and quad-modules for the outer barrel and the forward regions. 3D and planar sensors are considered for the inner layers, while the use of planar technology is planned for quad-modules in the other parts of the detector. The pixel cell size is not yet decided, it could be 25×100 μm^2 or 50×50 μm^2, both compatible with the 50×50 μm^2 electronics cell. Finally, sensor thicknesses will be a compromise between charge collection, material budget and cost, and could be different in the different parts of the detector.

The read-out will match the requirements of the ATLAS trigger which will be finalized in the coming months. Two hardware triggers levels are currently under consideration: L0 at a rate of 2-4 MHz with 2 μs latency and L1 at a rate of 0.6 MHz that will use also a track trigger input, with a total latency of 25 μs. The outer part of the Pixel detector should be readable at the L0 rate in order to be used by the track trigger; the innermost part should use L0 as a fast clear and then send out data at 600 kHz.

The electrical data transmission system for the Pixel detector runs from the front-end read-out chip to the optical transceiver box outside the ITk volume, approximately seven metres away. The point-to-point data links must operate at speeds up to 5 Gb/s for the inner barrel layers and 2.5 Gb/s for the outer barrel layers and forward regions.

3.1 Read-out electronics

To allow operation in such a harsh radiation environment new front-end electronics is under development within the RD53 collaboration who is developing the pixel read-out chip technology for both ATLAS and CMS usage at the HL-LHC [4]. This is a critical path item for both experiments. RD53-A is a first large format 2 cm^2 chip, to demonstrate that the design requirements are met and to allow the experiments to test sensors with the final pixel size. The submission of this chip is planned for the end of March 2017 and its delivery for the end of June 2017. In the meantime, two small 64x64 pixel matrix prototypes have already been designed: FE65-P2 (received on Dec 2015) and CHIPIX65 (submitted in July 2016). Significant testing of the RD53-A chip and hybrid modules built with RD53-A chips will take place in 2017/18. After this first phase of RD53-A tests, the ATLAS design team will directly proceed to the design of the final pixel read-out chip relying heavily on RD53-A and its initial test results, and using the tools, basic blocks, and design environment provided by RD53.

3.2 Sensors

A new generation of planar sensors is under development for the HL-LHC trackers. The main challenges to face are to obtain a low cost per unit area for the outer radii; to reduce the material budget, to be rad-hard and minimize the thermal runaway in the inner radii. The R&D program has already achieved several results. The n-in-p (rather than the traditional n-in-n) technology allows

for cost reduction thanks to the single side processing and the less complex handling and testing. The reduced thickness in the range of 100-150 μm (with respect to the 200 μm for the sensors used in IBL and 250 μm in the three outer ATLAS pixel layers) achieves a better radiation hardness and material reduction. Prototypes from different vendors, such as Cis, Advacam, MPG-HLL, FBK, Hamamatsu, have been produced and studied.

Preliminary results show good hit efficiencies up to the physical perimeter of the devices obtained with 100-150 μm thin active edge sensors. A hit efficiency up to 97 % with FE-I4 modules has been reached in test beam measurements with 100 μm thin sensors at a bias voltage of 350 V for a fluence of $5 \times 10^{15} n_{eq}/cm^2$. Comparing this performance with those of thicker sensors, as shown in Fig. 5 left, it is evident that 100 μm thin sensors can provide the same tracking efficiency than thicker sensors but at lower bias voltages. Based on this result, the power dissipation has been estimated to be in the range of 25-45 mW/cm^2 at a temperature of -25°C at a fluence of 10^{16} n_{eq}/cm^2 (see Fig. 5 right).

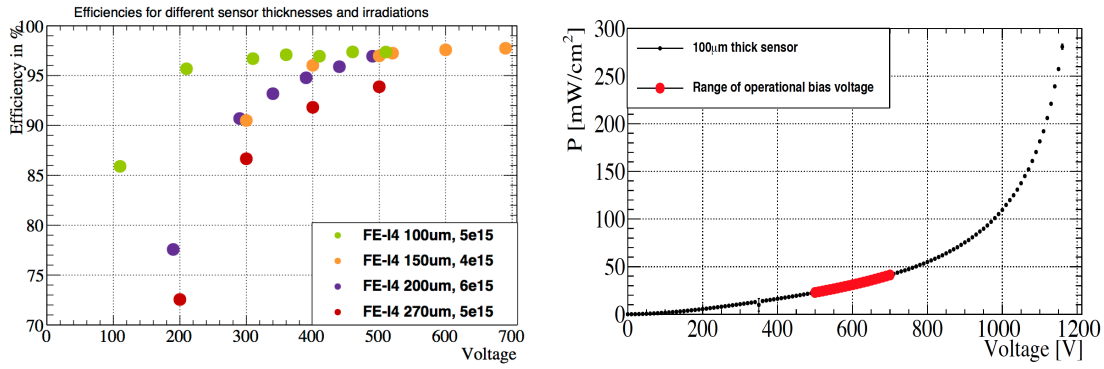

Figure 5: Left: Comparison of hit efficiencies obtained with planar pixel sensors of different thickness interconnected to FE-I4 chips after a fluence of approximately 5×10^{15} n_{eq}/cm^2 . Right: Power dissipation estimated for 100 μm thin sensors at a temperature of -25°C irradiated to a fluence of 10^{16} n_{eq}/cm^2 . [5]

3D silicon detectors are candidates to be used in the innermost layer(s) of the Pixel barrel system and some of the inner end-cap rings due to their excellent radiation hardness at low operational voltages. 3D silicon detectors have recently undergone a rapid development from R&D to industrialisation with their first operation in the IBL. IBL-generation 3D pixel detectors coupled to FE-I4 pixel electronics have been found to have hit efficiencies in test beam measurements larger than 97% at 170 V after irradiation to 10^{16} n_{eq}/cm^2 for normally incident minimum ionizing particles with a power dissipation of 15 mW/cm^2 at a temperature of -25°C [6], see Fig. 6 left. For the HL-LHC the main challenges are the design of small cells and thinner substrate; the production rate and yield should be regarded as critical issues. Progress has been made in the 3D R&D programme: the production process is now single sided thus simplifying the production steps; columns diameter as small as 5-8 μm have been produced in sensor with 50×50 μm^2 and 25×100 μm^2 pixel cells (see noise measurements in Fig. 6 right); 50-200 μm thin sensors have been produced with the use of support wafers. Several vendors are producing prototypes and are now designing sensors compatible with the RD53-A chip.

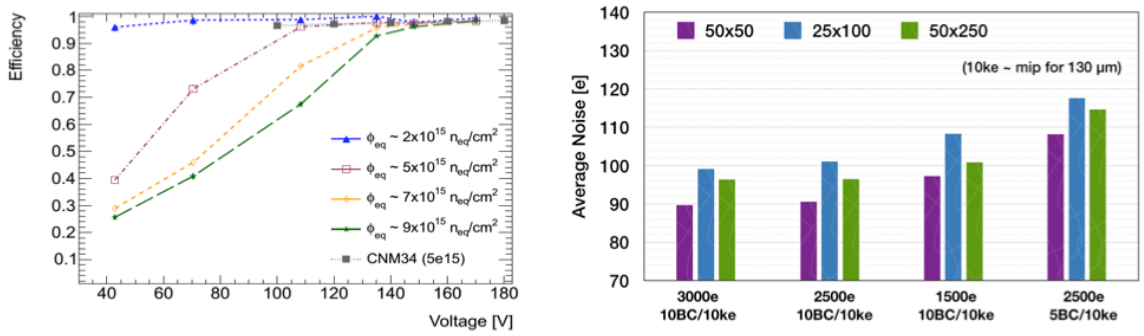

Figure 6: Left: Hit efficiency as a function of bias voltage for different fluence regions on a non-uniformly irradiated 3D FE-I4 detector [6]. Right: Comparison of mean noise on FBK devices, equipped with FE-I4 read-out chips, for different sensor cell dimensions and four threshold and time over threshold tuning configurations.

3.3 Interconnections

A key step in the fabrication of the hybrid pixel assembly is the flip-chip bump bonding process. There are two major challenges in this process. The first one is the requirement to produce very thin pixel assemblies, targeting 100-150 μm for the inner layers. The second challenge is the production rate and volume required for the substantially enlarged Pixel system. Additional requirements include: read-out wafer sizes of 12" and a five-fold increase in bump density due to the pixel pitch of 50 μm in both directions.

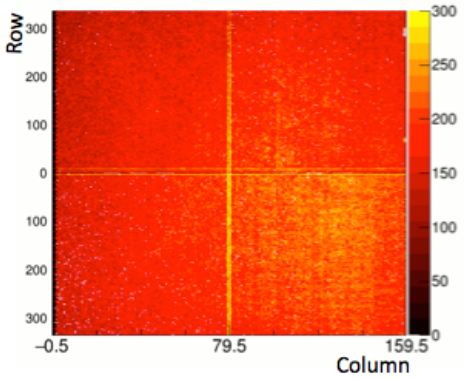

Figure 7: The response to Am-241 gamma radiation of a thin chip FE-I4 based Quad module produced at HPK (150 μm thick sensor and read-out chip) [2]. The plot shows the number of hits recorded per pixel.

Different processes have been investigated to enable thin devices flip-chip. The first is a low temperature flip-chip process using indium bumps, used with good results in terms of bump density and substrate thicknesses at Selex and HPK. Figure 7 shows an example of a source hit map on a quad-module flip-chipped with In bumps at HPK. The second process developed at IZM, and used for the IBL, employs a temporary glass carrier wafer bonded to the backside of the thinned read-out chip wafer. The wafer including carrier is diced and the chip-carrier packages are used for flip-chip

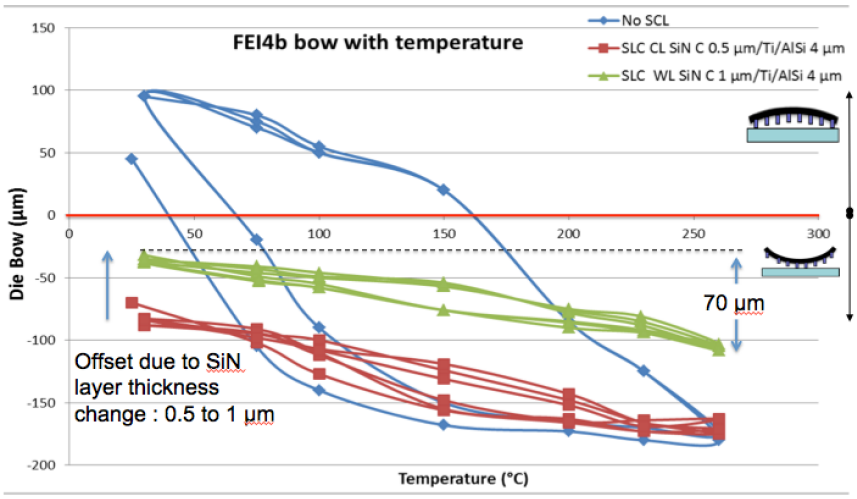

Figure 8: Wafer bow versus temperature with or without a Stress Compensation Layer (SCL) [7].

to prevent the chips from bowing during the solder reflow process. The glass carrier is removed from chip backside after the flip-chip process by laser exposure. Another method uses a dielectric and metal layer deposited on the backside of the read-out chip wafer to balance the bow induced from the front-side stack (CEA Leti/Advacam [7]), as shown in Figure 8. This layer is not removed after flip-chip.

In 2017/2018 several vendors will be qualified, investigating also the possibility to decouple the bump deposition from the flip-chip that can be partially done in-house. While preparing for the Technical Design Report, other cost saving solutions and possible production bottlenecks are explored. Alternative solutions are for instance Through Silicon Vias, chip to wafer bonding or the use of hybrid pixels with passive or active CMOS sensors or fully monolithic detectors [8].

4. Conclusions

The Pixel detector production schedule, shown in Figure 9, is determined by two parameters: the availability of module components, fixing the start of the pre-production phase, and the start of ITk integration at CERN, when all the modules must be ready. It is then conservatively assumed that the total time available for module production and loading is 30 months, from Q2 2020 to Q4 2022, while all the modules, tested, qualified and mounted on the local supports must be available at CERN by the end of 2022, in order to allow for the ITk installation in the ATLAS cavern for mid-2025.

One of the crucial module components still missing precise fabrication plans is the new read-out chip: the schedule assumes that two submissions of the ATLAS chip may be needed to achieve the requested functionalities. The Pixel Technical Design Report foreseen in late 2017 will not contain a complete baseline design for the different module flavours that will be used in the detector: the final decision on some aspects of the implementation will be postponed until the beginning of the pre-production, around Q1 2019.

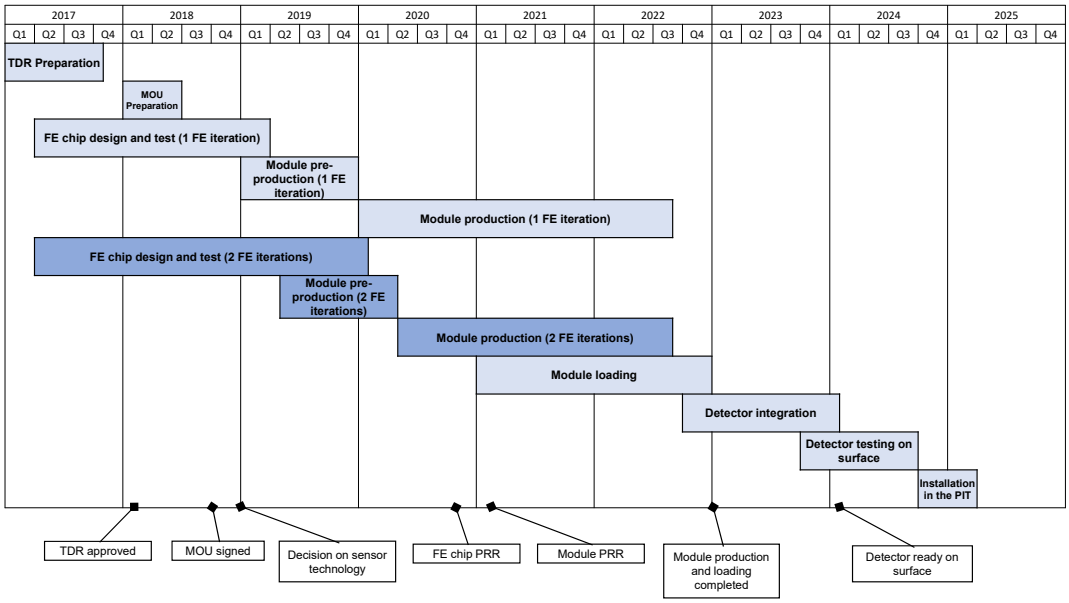

Figure 9: Schematic timeline of the Pixel detector production [2].

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