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The ATLAS tracker strip detector for HL-LHC

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As part of the ATLAS upgrades for the High-Luminosity LHC (HL-LHC) the current ATLAS Inner Detector (ID) will be replaced by a new Inner Tracker (ITk). The ITk will consist of two main components: a semi-conductor pixel detector at the innermost radii, and a silicon strip detector covering larger radii out as far as the ATLAS solenoid magnet including the volume currently occupied by the ATLAS Transition Radiation Tracker (TRT). The primary challenges faced by the ITk are the higher planned read out rate of ATLAS, the higher density of charged particles in HL-LHC conditions, and the corresponding high radiation doses that the detector and electronics will receive. The ATLAS collaboration is currently working on designing and testing all aspects of the sensors, readout, mechanics, cooling and integration to meet these goals and a technical design report (TDR) is being prepared. This report is an overview of the ITk strip detector, highlighting the current status and the road ahead.

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1. Introduction

1.1 ATLAS Inner Detector at the HL-LHC

The current Inner Detector (ID) of the ATLAS experiment [1] was designed for running at LHC conditions for up to ten years. It will not be able to withstand the higher particle density environment or higher total dose that will be delivered at the High-Luminosity LHC (HL-LHC) [2]. Whereas during 2016 data taking the LHC provided up to 50 collisions per bunch crossing, the HL-LHC is expected to provide as many as 200. The LHC plans to deliver a total integrated luminosity of 300 fb^{-1} whereas the HL-LHC plans to deliver 3000 fb^{-1}. Extracting meaningful physics in this environment requires a new radiation hard inner detector with high granularity. The new detector must also be equipped to deal with updated ATLAS Trigger, Timing and Control (TTC) requirements. Currently the first level trigger at ATLAS runs at up to 100 kHz whereas for the HL-LHC the first level trigger rate will be 1 MHz or higher.

The current ID consists of three main subsystems: a silicon pixel detector at the smallest radii, a silicon strip detector (SCT) at larger radii, and a Transition Radiation Tracker (TRT) based on straw tube technology extending to the edge of the ID volume at a radius of 1 m. The entire ID will be replaced by the Inner Tracker (ITk) [3, 4, 5], which will consist of an inner pixel detector surounded by a silicon strip detector extending out to the largest radii. The design of the ITk strip detector and component testing is currently underway, with a module pre-production stage set to begin in 2018.

2. Design

The ITk strip detector design is at a mature stage with the technical design report (TDR) set to be released later this year. Several aspects of the design are covered briefly in this section. To allow for good physics reach at the HL-LHC the ITk is being designed to achieve high-granularity with high bandwidth readout while maintaining a low material budget, mechanical stability, and radiation hardness.

2.1 Layout

The ITk layout seeks to provide a sufficient number of space points with high granularity throughout the entire ID volume, extending to 1 m in radius (R) and ± 3 m along the beam (z). All space points will be provided by silicon based tracking technology. The ITk pixel detector will cover the innermost regions. The ITk strip detector will cover the region extending from the edge of the pixel detector to the outermost reaches of the ID volume.

The precise layout of the ITk is now converging towards an optimal design, with several possibilites being considered. The layouts under consideration differ only in the design of the ITk pixel detector and will not be discussed further here.

The ITk strip detector consists of 4 barrel layers extending to $z = \pm 1400$ mm and 12 endcap disks (6 on each side) extending from the edge of the barrel to $z = \pm 3000$ mm (see Fig. 1). The innermost barrel layers will be populated with short strip segments (24.1 mm) to increase granularity at small radius as compared to the long strip segments (48.2 mm) in the outer barrel

layers. Similarly, in the end-caps each disk will contain shorter strips at smaller radii for increased granularity with longer strips at larger radii.

Simulations of collisions in the ATLAS detector have been performed to assess both the performance of the ITk layout and the radiation doses and particle fluxes through the detector. The highest expected fluence in the strip detector over the HL-LHC lifetime is 8.2×10^{14} n_{eq}/cm^2 and the highest expected total ionising dose (TID) is 33.6 MRad without applying any safety factors.

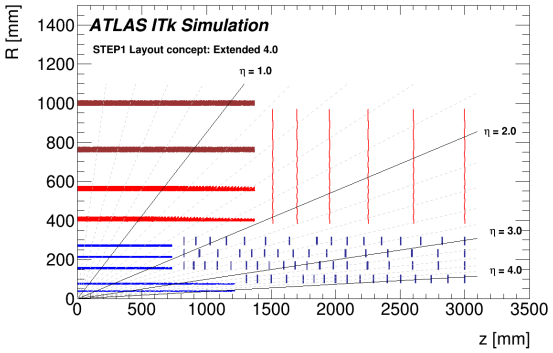

Figure 1: The layout of the ITk detector. Here only one quarter segment is shown. The horizontal axis, z, is the axis along the beam line with zero being the interaction point. The vertical axis, R, extends outward perpendicular to the beam pipe and the origin of co-ordinates is taken to be the center of the detector. [6]

2.2 Staves and petals

The barrel layers (end-cap disks) are formed from independent substructure units called staves (petals). Each substructure unit provides mechanical support, cooling, power and data transmission to strip modules (see Figs. 2,3). Strip modules are mounted on either side of the substructure unit with the strips on opposite sides at a small stereo angle to provide space points to be used for tracking.

Staves (petals) are populated with 14 (9) strip modules on each side. Each module sensor is glued to a thin bus tape. The bus tape itself consists of copper lines for power and communications sandwiched between layers of polyimide. The bus tape is co-cured to the carbon fibre frame which provides mechanical stability for the substructure. The carbon fibre frame is filled with a carbon honeycomb foam for rigidity. Titanium tubes with a 2.5 mm outer diameter deliver the flow of evaporative CO_2 which provides cooling for the detector (see Fig. 4).

The cooling, power and data transmission are all connected to each substructure at one end only. For staves these services are connected at the large |z| side of the substructure, whereas for petals the services are routed to the large radius side of the substructure. The cooling tubes contain a U-shaped bend at the small z (small radius) side of the stave (petal) such that the inlet and outlet from the substructures are at the same end. To electrically isolate the cooling pipes from the off-detector cooling system a small ceramic section of tube is used near the connection of the cooling pipes to the substructure. Electrical power and signals are received by the substructure at a designated site known as the End Of Substructure Cards (EoS).

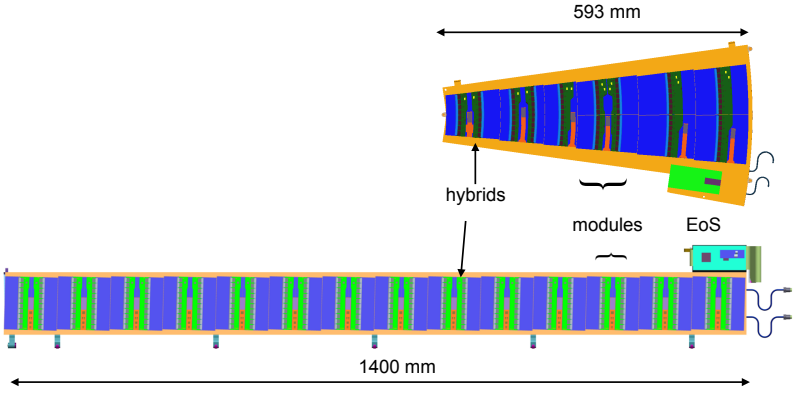

Figure 2: Petal (top) and stave (bottom) structures showing the placement of modules, the End of Substructure Cards (EoS) and the cooling pipe connections.

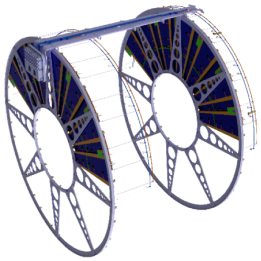

Figure 3: Partially populated end-cap disks showing the overlapping tiling of the petals on the disk. Services are routed to each of the petals via the service tray. Barrel services will be routed via similar trays overtop of the end-cap services.

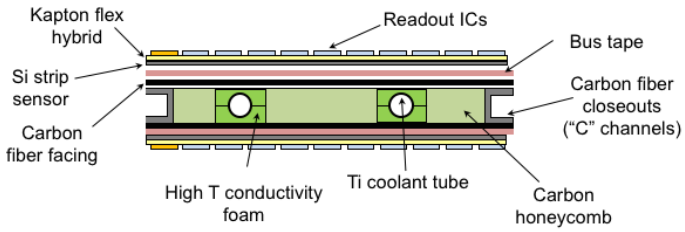

Figure 4: Schematic (not to scale) showing the internal structure of a stave core.

2.3 Electronics architecture

Signals will be transmitted between the substructure units and the off-detector electronics via optical fibres attached to the End of Substructure Cards (EoS). The serialization/deserialization required for data being transmitted and received on the bus tape will be performed by the low power GigaBitTranceiver (lpGBTx). The high speed optical transmission and reception between the substructure and the off detector electronics is performed by the Versatile Link+ (VTRx+) fibre optic driver. These projects [7, 8]are being developed at CERN to deal with the large radiation doses and high data rate conditions prevailing at the HL-LHC.

Signals will be carried between the modules and the EoS along multi-drop copper traces in the bus tape. The bus tape also carries lines for the high-voltage power required to bias the sensor, the low voltage power required for the module electronics, and I^2C signals for slow control.

Although the ITk strip detector will consume much less power per channel than the SCT there are many more total channels and total power consumption will increase. To deal with space and material constraints power will be transmitted to the each module at 11 V where it will be converted to the necessary operating voltage using a custom DC-DC converter built around the upFEAST chip [9].

Each module contains a power board on which the DC-DC converter sits. High voltage biasing of the sensor is controlled via a high-voltage multiplexer (HV Mux) [10]. A custom ASIC called the Autonomous Monitor Chip (AMAC) will monitor powering and environmental conditions. Based on the measured conditions the AMAC will control both the high and low voltage power so that they can be controlled independently of each other and independently on each module. The AMAC can be programmed and monitored via I^2C links on the bus tapes.

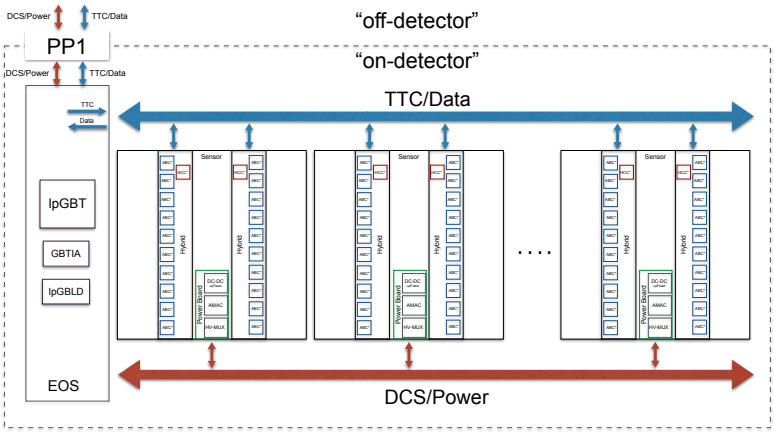

Figure 5: Schematic of the power and electronics architecture. The Timing, Trigger, and Control (TTC), Detector Control Signals (DCS), and power are carried between the modules and the End of Substructure (Eos) card via custom bus tapes. Optical links are used for communication lines between the EoS and the off-detector readout.

2.4 Modules

Modules are formed by gluing a power board and one or more readout boards (hybrids) on to a silicon strip sensor. Each hybrid contains between 7 and 12 read out chips (ABCs) and one or two control chips (HCCs) which manages communication between the ABCs and the EoS (see Fig. 6). The power boards are as described in Sec. 2.3. Several slightly different module designs exist to accommodate varying strip lengths as well as petal geometry.

2.5 Sensors

The strip sensors are AC coupled with n-type implants in a p-type silicon float zone (n^+-in-p FZ) and therefore collect electrons. This choice of sensor avoids type inversion due to radiation,

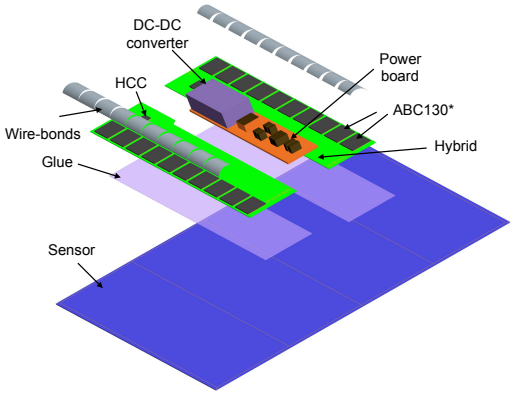

Figure 6: Exploded view of a barrel module.

maintains better charge collection at end of lifetime doses as compared to the p-in-n technology used in the SCT, and is lower cost than n^+-in-n. The nominal sensor bias voltage will be 500 V with the possibility of increasing the bias to 700 V to address changes in performance due to radiation exposure. Tests indicate a total drop in collected charge of a factor of $\sim$2 at end of lifetime doses [11].

Sensors are fabricated out of 6 inch wafers with a thickness between 300 and 320 microns and with strip lengths that vary from 19 to 60.1 mm according to module placement to accommodate for varying particle fluxes. Strip pitches are 75.5 microns in the barrel and vary between 69 and 84 microns in the end-cap.

Sensors in the barrel are rectangular and strips run parallel to the edge of the sensors. Strips will be placed at a 26 mrad angle with respect to the z direction giving a total stereo angle of 52 mrad. The stereo angle is achieved by rotating the sensor as it is placed on to the substructure. In the end-cap sensors have a nearly trapezoidal geometry but with curved edges along the top and bottom such that each sensor forms one section of a ring. Six rings of increasing radius cover the end-cap. The strips are rotated 20 mrad within each sensor to acheive a total stereo angle of 40 mrad with no rotation of the module.

Quality assurance (QA) tests have been performed on a batch of 100 Hamamatsu sensors showing average 51 micron bow centre to corner and 99.97% good strips. The breakdown voltages of the sensors were tested by applying a bias voltage up to 1 kV. Breakdown was observed in only 1 of the 100 sensors. [13].

2.6 ASICs

The front-end readout is implemented by a custom ASIC designed in 130 nm CMOS technology and fabricated by Global Foundries. Each chip measures 7.9$\times$6.8 mm, has 256 front-end channels, and draws $\sim$100 mW of power in baseline operating conditions. Each chip can be considered in two main sections. The analog front-end of the chip performs binary readout of the strips including signal amplification and discrimination. The digital functionality of the chip decodes signals, buffers events, and contains configuration registers. Enclosed layout transistors (ELTs) are used in the analog portion of the chip to ensure good performance stability. Additionally, front-end

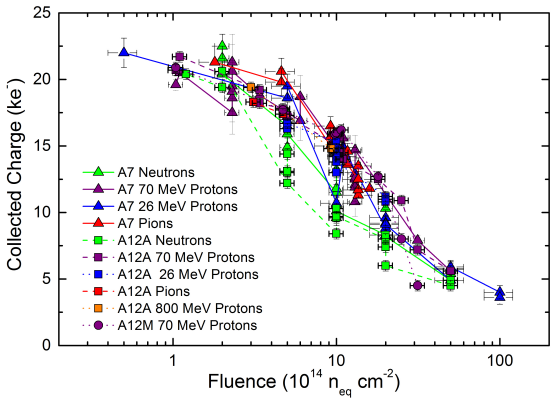

Figure 7: Signal charge collected from minimum ionising particles (MIPs) passing through sensors biased to 500 V after irradiation with various particle types [11].

parameters can be tuned to ensure consistent performance throughout the lifetime of the chip as well as between chips and across channels within a single chip.

Configuration registers are triplicated to protect against single event upsets (SEUs). If any of the three triplicated registers reads a different value from the other two it will be changed on the next clock cycle to match the consensus. For debugging purposes a read-only register on the chip sets a flag when such a triplication correction occurs.

The design of the ABC is ongoing. The current version of the chip is the ABC130. The final design of the chip, called the ABCStar, is expected to be submitted in mid-2017. The ABCStar is so named for its star-network readout scheme, where each ABC has a dedicated transmission line to the HCCStar. In the current scheme chips are read out in a daisy chain (see Fig. 8). This change allows for higher bandwidth between the ABCs and HCC. Other improvements to the chip, including front end noise reduction, and changes to pad placements, communication protocols and readout logic, are also being made.

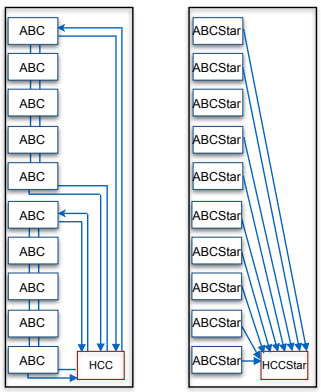

Figure 8: The ABCStar signal routing (right) as compared to the old daisy-chain readout (left).

3. Testing and production

3.1 ASIC testing

The ABC130 has undergone tests to ensure its ability to deal with both the high flux rates and the large dose it will have accumulated by its end of life.

Single event effect (SEE) tests were performed at the CHARM facility at CERN supplying 24 GeV protons. Chips were placed directly in the path of the beam which delivered spills containing nearly 3 $\times 10^9$ protons/cm^2/spill every O(5s). Before each spill the chip was configured to a known state. After each spill the chip was read out and compared to the configured state. Tens of thousands of spills were analyzed for bit flips and functional errors. Measurements showed bit flip cross sections in the data pipeline of 1×10^{-13} cm^2. Triplication of registers was found to decrease the rate of bit flips by a factor of 50 in most registers. Functional errors including duplicated and missing packets were also analyzed. Based on comparisons with current SCT operations and FLUKA [14] simulations the measured cross sections and functional error rates are expected to be well within acceptable limits. Over the course of the test the chips accumulated a total dose of $\sim$6 MRad. Error rates as a function of total ionising dose were examined but no evidence for such a dependence was found.

Total ionising dose (TID) tests have also been performed on the chip under a variety of conditions. Initial tests showed a large increase in the current drawn by the digital portion of the chip around a TID of 1 MRad. The current then slowly returns to its nominal value with increasing dose. This 'TID bump' has been observed in 130 nm CMOS transistors previously by F. Faccio et. al. [17, 18], as well as in the ATLAS Insertable B-Layer (IBL) [19].

Initial tests were done at very high dose rate (2.2 MRad/h) and ambient temperature. Subsequent tests have been performed to understand the characteristics of this current increase, particularly its dependence on dose rate and temperature. These tests have confirmed the increase in current is correlated with dose rate and anti-correlated with temperature as predicted by an empirical model [20]. Tests have been performed at dose rates and temperatures compatible with HL-LHC expectations and show an increase of order 50% in the digital current for the chips in areas of the detector which will receive the highest dose rate. Considerations for cooling and powering requirements have been adjusted to take into account the increased power consumption of the chips at the TID bump.

Although the analog transistors are protected from the increased leakage current at the TID bump by the the use of the enclosed layout technique, the front-end characterestics are still liable to be affected by radiation damage. The effect of TID on the gain and noise was measured. The gain was found to decrease by up to 10% in relevant conditions with some recovery with increasing TID. The noise showed an increase of up to 25% with no recovery at high dose. It is believed that this noise increase is related to a few transistors in the ABC130 front-end which do not use the enclosed layout, and is being addressed for the ABCStar.

3.2 Test beams

Test beams have been performed at the DESY-II and CERN SPS test beam facilities to understand strip module performance. Test beams have evolved from testing single chips attached to

mini-sensors (1 cm^2) to the testing of fully populated hybrids with 10 ABCs and 1 HCC attached to long and short strip modules. The most recent test beam campaign, at the CERN SPS, included a complete module which had previously undergone irradiation up to 8×10^{14} n_{eq}/cm^2 [21].

To study charge collection efficiency 200 thousand triggers of test beam data were taken for various sensor biases, hit thresholds and sensor positions. Hit efficiencies for each setting are extracted, from which charge collection and noise properties can be studied. Using the 1.5-2 μm tracking resolutions from the test-beam telescopes, hit efficiencies and cluster size are also studied as function of the hit position within the strip. Hit efficiencies and noise occupancy requirements are met over a wide range of thresholds (0.5-2 fC) for unirradiated modules. For irradiated modules a narrow range of thresholds around 0.7 fC meet the requirements. However, it has since been found that the front-end settings used for those measurements were suboptimal and that lower input noise can be acheived with updated settings. The range of thresholds for which noise and efficiency requirements are met after irradiation is also expected to be widened with production modules due to several changes in the module and environment. In particular, production sensors will have larger substrate resistance and will benefit from annealing periods. In addition, the ABCStar front-end will be more robust against radiation damage. Increasing sensor bias voltage is also found to increase the range of thresholds which meet specification.

3.3 Production

The large number of components required for the final detector, which includes 17,888 modules, presents a challenge for production. A distributed production model is being used to meet this challenge. Sites will specialize in producing one or more components which will then be shipped to other sites for further integration. Several steps of the build process will take place at multiple sites to allow for high throughput and to add redundancy for sites experiencing downtime. For example, 15 sites will be involved in module assembly. The final barrel assembly and integration will take place at CERN. Each end-cap will be assembled at a different location, one at DESY in Hamburg and the other at NIKHEF and then they will be shipped to CERN.

Sites are gaining experience with currently available components and standardized requirements for production sites are being specified including quality control testing. A travelling module has been shipped to sites across Europe and North America to ensure reproducability of test results across sites and safety of components in transit.

A production database is being implemented to contain serial numbers and information for all parts. Part information will include items such as assembly and production sites, pictures for visual inspection, and the results of mechanical or electrical tests performed on the item. The database API will be acessible via HTTPS.

4. Conclusions

The ATLAS ITk strip detector is a large area (165 m^2) silicon strip detector designed to provide high-granularity, high data-rate readout while maintaining radiation hardness and a low material budget. A modular design approach where small, largely independent building blocks form larger and larger structures has been employed. Testing of relevant componenents is underway and challenges are being addressed. A distributed production model will be used to meet the large volume

requirements and the long times associated with some assembly steps. Final commissioning and installation is set to take place at CERN to begin operating the ITk at the start up of the HL-LHC.

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